First Announcement

2003 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference — September 16-18, 2003

Short Course — September 19, 2003

Place — Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel)

Paper Deadline — May 8, 2003

On-line submission through the conference website will be available for the 2003 conference. Details of the submission procedure will be announced in the final announcement as well as on the website by the end of March 2003.

Late News Paper Deadline — July 25, 2003

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THE JAPAN SOCIETY OF APPLIED PHYSICS
Technical Cosponsored by
IEEE Electron Devices Society
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ssdm 2003

Web Site : http://www.intergroup.co.jp/ssdm

The 2003 International Conference on Solid State Devices and Materials (SSDM 2003) will be held on September 16-18, 2003 at the Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel). Since 1969, the conference has provided good opportunity to discuss key aspects of solid state devices and materials. For the 2003 conference, fourteen program sub-committees have been organized for covering circuits and system areas as well as device and material areas. In addition, one-day short courses are scheduled after the conference, which offer tutorial lectures on important areas.

LOCATION

The Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel) is the perfect place for business, and a pleasant sanctuary in the heart of the city. The Tokyo Metropolitan Government Building and other skyscrapers tower upwards. JR or subway lines are within easy access, 5 minutes by walking from West Exit, Shinjuku Station.

URL: http://www.keioplaza.com/index.html

CONFERENCE LANGUAGE

The official language of the conference is English.

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging to discuss problems to be solved in these fields, new findings and new phenomena and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate the mutual understanding among people in the fields of devices and material and those in the fields of circuit, system and packaging. For the 2003 conference, fourteen program subcommittees have been organized in order to bring higher quality paper selection and strengthening into specific technology areas. The scope of each subcommittee is listed below.

CORE AREAS

[1] Advanced Silicon Circuits and Systems

(Chair, T. Kuroda, Keio Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems, are solicited in the subject areas including, but not limited to, the following: (1) Advanced digital, analog, mixed-signal, and memory, (2) Wireless, wireline, and optical communications, (3) Imagers, displays, and MEMS, (4) Low power technologies and power aware systems, (5) High speed circuits and systems, (6) Technologies for systems on a chip, (7) New concept and technologies; based on nanoelectronics, quantum mechanics, 3D-electronics,

ferroelectrics, photonics, and organic electronics; using neural network, fuzzy logic, and multi-valued logic; and for bio-medical and microfluidic applications.

[2] Advanced Silicon Devices and Device Physics

(Chair, T. Mogami, NEC)

The scope of this subcommittee covers all aspects of advanced silicon devices and device technologies for circuit applications. Papers are solicited in the following areas: (1) Sub-100nm silicon CMOS devices and their integration technologies including logic, memory and merged logic/memory LSIs, (2) Post-CMOS silicon device structure including vertical device and strained-silicon channel device, (3) New concepts, theories and breakthroughs in silicon-related devices, passive device and other functional devices, (4) Physics and reliability for advanced processes/devices including simulation and modeling and (5) Manufacturing and yield issue.

[3] Silicon Process / Materials Technologies

(Chair, N. Kobayashi, Selete)

The session consists of advanced process and materials technologies for Si ULSI applications. Strongly encouraged are the topics of material innovations to improve device performance, manufacturability, and cost-efficiency. Papers are solicited in, but not limited to, the following areas: (1) Novel materials technologies such as high-k and ultra-low-k process to break through the scaling limitations of Logic, Memory and New-concept devices (2) Key process technologies to integrate sub-90nm Si ULSIs such as gate oxide integrity, ultra-shallow junction and Cu/low-k processes (3) Critical reliability issues related with advanced FEOL and BEOL processes including packaging.

[4] New Materials and Characterization

(Chair, S. Takagi, Toshiba)

Introduction and utilization of new materials are expected as a key concept for further evolution and functionarization of Si-based logic and memory LSIs. Also, novel characterization techniques are indispensable in realizing these advance devices. Papers are solicited in the following areas (but not limited to these subjects): (1) Characterization and processing of group-IV semiconductors, high-k and low-k dielectrics and other new materials, including diamond, silicides (germanides), nano-tubes, fullerence and any other materials applicable to Si-based LSIs, (2) Physics and chemistry of surface and interface phenomena (including oxidation and nitridation), (3) Reliability physics and failure analysis of gate oxides and interconnect systems, (4) New characterization method for devices and materials including in-situ monitoring and nanometer-scale characterization. Submission of papers at a germinal stage is also encouraged.

[5] Compound Semiconductor Materials and Devices

(Chair, N. Kobayashi, NTT)

Compound semiconductors are the key materials supporting the highly information oriented society.
III-V, II-VI and wide-gap GaN and ZnO, and magnetic semiconductors are included as the materials.
Compound Semiconductor Materials and Devices covers the following areas (but not limited):
(1) Growth and characterization,
(2) Heterostructures and superlattices,
(3) Optical devices (LEDs, LDs and detectors) and electron devices (HFETs and HBTs), their device processing and reliability.

[6] Optoelectronic Devices and Photonic Crystal Devices

(Chair, O. Wada, Kobe Univ.)

Towards ubiquitous communication and computing, optoelectronic devices are expected to explore novel functions and enhance performance by utilizing novel device physics and developing advanced fabrication techniques. The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices, which includes (1) laser diodes, LEDs, photodetectors, SOAs, and OEICs, (2) photonic crystal materials and novel functional devices, (3) optical switches, modulators, and MEMS, (4) optical wavelength converters, nonlinear optical devices, and all-optical switches, (5) waveguide components, PLCs and integrated photonic circuts, (6) material and device processing and characterization techniques, (7) hybrid and monolithic integration, packaging and moduling, and (8) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices.

[7] Novel Devices, Physics, and Fabrication

(Chair, K. Ishibashi, RIKEN)

The aim of this subcommittee is to explore novel devices and physics, mainly in nanoscale, with inorganic and molecular materials. Papers are solicited in the following areas, but not limited to: (1) quantum phenomena in nanoscale, (2) quantum dots and single electron devices, (3) solid state quantum computing, (4) spintronics, (5) new nanoscale materials such as carbon nanotubes, (6) molecular electronics, (7) other novel devices such as small superconducting device and resonant tunneling device. (8) nanofabrication, nanomechanics and characterization techniques in nanoscale.

[8] Quantum Nanostructure Devices and Physics

(Chair, Y. Hirayama, NTT)

The field covers recent progress in physics, fabrication, characterization and device applications of nanostructures.
The main topics includes (1) growth and processing of quantum dots and nanostructures. (2) transport/optical

properties and THz/Femto-second dynamics (3) nanometer-scale characterization such as SPM and SNOM (4) nano electronic/optical devices (5) novel nanostructures and nanomaterials such as photonic crystals, magnetic materials and organic semiconductors. (6) spin and carrier control in quantum nanostructures.

[9] Silicon-on-Insulator Technologies

(Chair, A. Ogura, NEC)

SOI technology today is rushing onto the commercial market while still being considered as a basic structure for achieving the ultimate Si devices. Moreover, new structures based on SOI are also appearing such as partial SOI, SON (Si on nothing), SGOI (SiGe on insulator) and SSOI (strained-Si on insulator). This subcommittee covers the whole field of SOI and SOI-related new technologies in a wide range of interests from circuit design to material issues. The topics will include, but not be limited to: (1) SOI Circuit Technology and LSI Applications (High Speed, Low Power Consumption, RF, Analog/Linear, etc.), (2) New Structure Devices (Double, Triple, Quadruple Gate, FINFET, Vertical Channel, Quantum, Strained Channel, Multi-Layer Devices, etc.), (3) Process Issues for Device Manufacturing (Isolation, Silicidation, Metal Gate, Plasma Damage, etc.), (4) Physics and Modeling of SOI Device/Process and Circuits (floating-body effect, self-heating, etc.), (5) SOI Materials Characterization and Manufacturing, and (6) Reliability Issues (Hot Carrier Injection, GOI, Radiation Effects, ESD, etc.).

STRATEGIC AREAS

[10] Non-Volatile Memory Technologies

(Chair, K. Takasaki, Fujitsu Lab.)

"Non-volatile Memories" session solicits all NV memory (Flash, FeRAM, EPROM, EEPROM, Anti-fuse, MRAM & others) technology related papers. Topics relating to NV devices include cell device physics & characterization, processing & materials, tunnel dielectrics, ferroelectric materials, reliability, failure analysis, quality assurance & testing, modeling & simulation, integrated circuits, new concept technologies, and new applications & systems (solid state disks, memory cards, programmable logic,—).

[11] SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

(Chair, T. Enoki, NTT)

Compound-semiconductor devices are playing important roles in wireless and optical communications systems. Future communications systems definitely require devices and circuits that dissipate lower energy, operate at higher bit rates or frequencies, have lower noise, generate higher signal power, and are more compact. This session covers advanced device and IC technologies that meet these challenges through the use of SiGe, GaAs-based, InP-based, and N-based materials (but not limited). Monolithic ICs or multi-chip modules integrating optical and electrical devices will also be discussed. Papers demonstrating breakthroughs and novel concepts, discussing on potentials and limitations, and addressing issues in these technologies are strongly solicited for this session.

[12] System-Level Integration and Packaging Technologies

(Chair, K. Takahashi, ASET)

The scope of this subcommittee involves all features of advanced packaging technologies and system-level integration technologies based on packaging technology. Papers are solicited in, but not limited to, the following areas: (1) Advanced packaging technologies including chip size package (CSP), wafer-level package, stacked package, (2) Three-dimensional (3D) integration technology including wafer stacking and chip stacking, (3) System integration technologies including SiP (system-in-package), SoP (system-on-package), opto-electronics integration and MEMS, (4) Design and CAD technologies for the advanced packaging and system integration including interface design, EMI and EMC management and ultra-high speed data transfer technologies, (5) Testing technologies for the system integration including burn-in, known good die (KDG) and design for test (DFT), (6) Modeling and simulation of thermal, mechanical and electrical performance of advanced packaging and system integration.

[13] Organic Semiconductor Devices and Materials

(Chair, M. Iwamoto, Tokyo Institute of Technology)

Electronic and Optical processes in organic materials and device application in the following fields (but not limited): (1) Organic transistors, diodes and circuits (2) Organic light emitting devices (3) Organic photodetectors and photovoltaic devices (4) Chemical sensors and gas sensors (5) Fabrication and characterization of organic thin films (6) Electrical and Optical properties of organic thin film and materials (7) Organic-inorganic hybrid systems (8) Interfacial phenomena, LC devices, etc.

[14] Micro-Nano Electromechanical Devices for Bio- and Chemical Applications

(Chair, Y. Miyahara, National Institute for Materials Science)

Micro/nano electromechanical devices (M/NEMS) are now widely applied to biochemical, medical and environmental fields and a new research field called μ-TAS or Lab. on a Chip is expanding and being established. Fusion of microelectronic devices with materials and methods in the chemical, biological, and mediacl fields is expected to open up new scientific and business fields. Papers are solicited in the

following areas (but not limited): (1) Micro/nano electronic mechanical system (M/NEMS) for RF, optical, power and others, (2) μ-TAS and Lab on a chip, (3) Various Bio-chips for DNA, healthcare and proteins, (4) Fabrication technologies and (5) New integrated micro/nano systems for biochemical and medical applications.

SUBMISSION OF PAPERS

The submission method will be changed to on-line submission through the conference website. Details will be announced in the final announcement as well as on the website by the end of March 2003.

Paper Deadline is May 8, 2003.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed without opportunity for further change in the extended abstracts, which will be distributed on the opening day of the Conference.

Authors of papers accepted for SSDM 2003 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics. The special issue will be published in 2004.

AGREEMENT NOT TO PRE-PUBLISH ABSTRUCTS

Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by automatic withdrawal of the paper by the conference committee.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include a plenary session along with technical sessions comprised of invited and contributed papers for oral or poster presentation.

RUMP SESSIONS

Two rump sessions are planned to be held on September 17 (Wednesday). The detail of the rump sessions will be announced in the final announcement.

SHORT COURSES

One-day short courses are scheduled after the conference, i.e., September 19 (Friday) which offer tutorial lectures on important topics.

FINANCIAL SUPPORT

Limited financial support for presentations by students and by researchers from newly industrializing countries is available. People who are interested in the support should directly contact to the Steering Committee, *c/o Inter Group Corp., e-mail: ssdm@intergroup.co.jp.*

FINAL ANNOUNCEMENT

The Final Announcement and call for papers with complete instructions will appear in the end of March, 2003.

ADDITIONAL INFORMATION

Students' contribution is encouraged. We are pleased to discount the student registration fee (5,000 yen).
We are planning to adopt Poster Sessions.

ORGANIZING COMMITTEE

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