Call for Paper Final Announcement

2003 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference—September 16-18, 2003

Short Course—September 19, 2003

Place—Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel)

Paper Deadline—May 8, 2003

Online submission through the conference website is now available.

Late News Paper Deadline—July 25, 2003

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THE JAPAN SOCIETY OF APPLIED PHYSICS
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IEEE Electron Devices Society
in cooperation with
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ssdm 2003

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Call for Papers
Final Announcement

2003 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: September 16-18, 2003
Short Course (in Japanese): September 19, 2003

The 2003 International Conference on Solid State Devices and Materials (SSDM 2003) will be held from September 16 to September 18, 2003 at the Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid state devices and materials. For the 2003 conference, 14 program subcommittees have been organized covering circuits and systems, as well as devices and materials. One-day short courses are also scheduled for after the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM 2003 is available online at:

http://www. intergroup.co.jp/ssdm

PLENARY SESSIONS

Plenary Speakers:

"Research and Development Strategy for Creation of Corporate Value"

T. Ikoma (Hitotsubashi Univ., Japan)

"The Role and Strategy of IMEC as a European Player in a Globalized Research Era" (tentative)

G.J. Declerck (IMEC, Belgium)

"Progress and Perspective of Nanostructure Devices for Ubiquitous Information Network"

Y. Arakawa (Univ. of Tokyo, Japan)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging to discuss problems to be solved in these fields, new findings and new phenomena and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate the mutual understanding among people in the fields of devices and material and those in the fields of circuit, system and packaging. For the 2003 conference, fourteen program subcommittees have been organized in order to bring higher quality paper selection and strengthening into specific technology areas. The scope of each subcommittee is listed below.

CORE AREAS

[1] Advanced Silicon Circuits and Systems

(Chair, T. Kuroda, Keio Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems, are solicited in the subject areas including, but not limited to, the following: (1) Advanced digital, analog, mixed-signal, and memory, (2) Wireless, wireline, and optical communications, (3) Imagers, displays, and MEMS, (4) Low power technologies and power aware systems, (5) High speed circuits and systems, (6) Technologies for systems on a chip, (7) New concept and technologies; based on nanoelectronics, quantum mechanics, 3D-electronics, ferroelectrics, and photonics; using neural network, fuzzy logic, and multi-valued logic; and for bio-medical and microfluidic applications.

Invited speaker:
"Silicon Integration of UWB: Choices and Challenges"
S. Narendra (Intel, USA)

[2] Advanced Silicon Devices and Device Physics
(Chair, T. Mogami, NEC)

The scope of this subcommittee covers all aspects of advanced silicon devices and device technologies for circuit applications. Papers are solicited in the following areas: (1) Sub-100nm silicon CMOS devices and their integration technologies including logic, memory and merged logic/memory LSIs, (2) Post-CMOS silicon device structure including vertical device and strained-silicon channel device, (3) New concepts, theories and breakthroughs in silicon-related devices, passive device and other functional devices, (4) Physics and reliability for advanced processes/devices including simulation and modeling and (5) Manufacturing and yield issue.

Invited speakers:
"Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation"
J. Kedzierski (IBM, USA)
"Integration Issues of HfO_2-Al_2O_3 Laminate for Gate and Capacitor Dielectric"
H.K. Kang (Samsung, Korea)
"Searching for serendipitous gate dielectric, high-k or silicon oxynitride"
M. Hiratani (Hitachi, Japan)

[3] Silicon Process / Materials Technologies
(Chair, N. Kobayashi, Selete)

The session consists of advanced process and materials technologies for Si ULSI applications. Strongly encouraged are the topics of material innovations to improve device performance, manufacturability, and cost-efficiency. Papers are solicited in, but not limited to, the following areas: (1) Novel materials technologies such as high-k and ultra-low-k process to break through the scaling limitations of Logic, Memory and New-concept devices (2) Key process technologies to integrate sub-90nm Si ULSIs such as gate oxide integrity, ultra-shallow junction and Cu/low-k processes (3) Critical reliability issues related with advanced FEOL and BEOL processes including packaging.

Invited speakers:
"Stress Migration Phenomena of Copper Interconnects" (tentative)
T. Oshima (Hitachi, Japan)
"Recent material and process development for FeRAM applications" (tentative)
Y. Horii (Fujitsu, Japan)
"Mobility in high-k dielectric based field effect transistors"
L. Ragnarsson (IMEC, Belgium)

[4] New Materials and Characterization

(Chair, S. Takagi, Toshiba)

Introduction and utilization of new materials are expected as a key concept for further evolution and functionarization of Si-based logic and memory LSIs. Also, novel characterization techniques are indispensable in realizing these advance devices. Papers are solicited in the following areas (but not limited to these subjects): (1) Characterization and processing of group-IV semiconductors, high-k and low-k dielectrics and other new materials, including diamond, silicides (germanides), nano-tubes, fullerence and any other materials applicable to Si-based LSIs, (2) Physics and chemistry of surface and interface phenomena (including oxidation and nitridation), (3) Reliability physics and failure analysis of gate oxides and interconnect systems, (4) New characterization method for devices and materials including in-situ monitoring and nanometer-scale characterization. Submission of papers at a germinal stage is also encouraged.

Invited speakers:
"SiGe in Advanced CMOS devices - unique material equally helpful when present or absent"
T. Skotnicki (ST Microelectronics, France)
"Dual Gate Electrodes Materials for Advanced Silicon CMOS Devices"
V. Misra (North Carolina State Univ., USA)
"Nanoelectronics: carbon nanotubes and molecular devices"
H.-S.P. Wong (IBM, USA)

[5] Compound Semiconductor Materials and Devices

(Chair, N. Kobayashi, NTT)

Compound semiconductors are the key materials supporting the highly information oriented society. This

area deals with III-V, II-VI compound semiconductors including wide gap GaN and ZnO, and magnetic semiconductors.
The materials also includes other compound semiconductors such as SiC, $FeSi_2$ and so on. Compound Semiconductor Materials and Devices besides covers the following areas (but not limited): (1) Growth and characterization, (2) Heterostructures and superlattices, (3) Optical devices (LEDs, LDs and detectors) and electron devices (HFETs and HBTs), their device processing and reliability.

Invited speakers:
"High efficiency large area GaN-based light emitting diodes"
J.-I. Chyi (National Central Univ., Taiwan)
"MOVPE Growth of InN and its Optical Characteristics"
T. Matsuoka (NTT, Japan)
"Ultrahigh Performance InP HEMTs"
S. Endou (Fujitsu, Japan)
"Optical and Electrical Control of Ferromagnetism in II-VI Quantum Wells"
T. Dietl (Polish Academy of Sciences, Poland)
"Type-II InAs-based quantum cascade lasers"
K. Ootani (Tohoku Univ., Japan)

[6] Optoelectronic Devices and Photonic Crystal Devices
(Chair, O. Wada, Kobe Univ.)
Towards ubiquitous communication and computing, optoelectronic devices are expected to explore novel functions and enhance performance by utilizing novel device physics and developing advanced fabrication techniques. The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices, which includes (1) laser diodes, LEDs, photodetectors, SOAs, and OEICs, (2) photonic crystal materials and novel functional devices, (3) optical switches, modulators, and MEMS, (4) optical wavelength converters, nonlinear optical devices, and all-optical switches, (5) waveguide components, PLCs and integrated photonic circuts, (6) material and device processing and characterization techniques, (7) hybrid and monolithic integration, packaging and moduling, and (8) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices.

Invited speakers:
"SOA-based functional devices for future optical networks"
M.L. Nielsen (Technical Univ. of Denmark, Denmark)
"3D Photonic Crystal as a Novel Dielectric Material"
S. Kawakami (Tohoku Univ., Japan)
"Semiconductor 2D photonic crystal devices"
T. Baba (Yokohama Natl. Univ., Japan)
"Monolithic PD-EAM Optical Gates for Ultrafast Signal Processing"
S. Kodama (NTT, Japan)
"1.3μm GaInNAs(Sb) VCSELs"
A. Kasukawa (The Furukawa Electric, Japan)
"Advances in widely tunable optical transmitters"
L.A. Coldren (Agility Communications, USA)

[7] Novel Devices, Physics, and Fabrication
(Chair, K. Ishibashi, RIKEN)

The aim of this subcommittee is to explore novel devices and physics, mainly in nanoscale, with inorganic and molecular materials. Papers are solicited in the following areas, but not limited to: (1) quantum phenomena in nanoscale, (2) quantum dots and single electron devices, (3) solid state quantum computing, (4) spintronics, (5) new nanoscale materials such as carbon nanotubes, (6) molecular electronics, (7) other novel devices such as small superconducting device and resonant tunneling device. (8) nanofabrication, nanomechanics and characterization techniques in nanoscale.

Invited speakers:
"Quantum Oscillations in Two Coupled Charge Qubits"
Y. Pashkin (NEC, Japan)
"Carbon Nanotube SPM Probe Fabricated by NanoEngineering"
S. Akita (Osaka Pref. Univ., Japan)
"Nanoimprint Lithography—An Enabling Engine to Nanotechnology"
S.Y. Chou (Princeton Univ., USA)

[8] Quantum Nanostructure Devices and Physics
(Chair, Y. Hirayama, NTT)

The field covers recent progress in physics, fabrication, characterization and device applications of nanostructures. The main topics includes (1) growth and processing of quantum dots and nanostructures. (2) transport/optical

properties and THz/Femto-second dynamics (3) nanometer-scale characterization such as SPM and SNOM (4) nano electronic/optical devices (5) novel nanostructures and nanomaterials such as photonic crystals and magnetic nanostructures. (6) spin and carrier control in quantum nanostructures.

Invited speakers:
"Electronic and photonic devices via one-dimensional stacking of quantum structures"
L. Samuelson (Lund Univ., Sweden)
"Nuclear spin dependent transport in quantum dots"
K. Ono (Univ. of Tokyo, Japan)
"A Light Emitting Diode for Single Photons"
A. Shields (Toshiba Cambridge, UK)
"Control of ferromagnetic order in selectively p-doped GaMnAs-based heterostructures"
M. Tanaka (Univ. of Tokyo, Japan)

[9] Silicon-on-Insulator Technologies

(Chair, A. Ogura, NEC)

SOI technology today is rushing onto the commercial market while still being considered as a basic structure for achieving the ultimate Si devices. Moreover, new structures based on SOI are also appearing such as partial SOI, SON (Si on nothing), SGOI (SiGe on insulator) and SSOI (strained-Si on insulator). This subcommittee covers the whole field of SOI and SOI-related new technologies in a wide range of interests from circuit design to material issues. The topics will include, but not be limited to: (1) SOI Circuit Technology and LSI Applications (High Speed, Low Power Consumption, RF, Analog/Linear, etc.), (2) New Structure Devices (Double, Triple, Quadruple Gate, FINFET, Vertical Channel, Quantum, Strained Channel, Multi-Layer Devices, etc.), (3) Process Issues for Device Manufacturing (Isolation, Silicidation, Metal Gate, Plasma Damage, etc.), (4) Physics and Modeling of SOI Device/Process and Circuits (floating-body effect, self-heating, etc.), (5) SOI Materials Characterization and Manufacturing, and (6) Reliability Issues (Hot Carrier Injection, GOI, Radiation Effects, ESD, etc.).

Invited speakers:
"FinFET Promise and Challenges"
T.-J. King (Univ. of California, USA)

"Strained-Si on SOI MOSFETs"

J.J. Welser (IBM, USA)

"Quality comparison of commercial silicon-on-insulator wafers by photoluminescence"

M. Tajima (Inst. of Space and Astronautical Science, Japan)

"Ultralow-power CMOS/SOI Circuit Technology for Ubiquitous Communications"

Y. Kado (NTT, Japan)

STRATEGIC AREAS

[10] Non-Volatile Memory Technologies

(Chair, K. Takasaki, Fujitsu Lab.)

"Non-volatile Memories" session solicits all NV memory (Flash, FeRAM, EPROM, EEPROM, Anti-fuse, MRAM & others) technology related papers. Topics relating to NV devices include cell device physics & characterization, processing & materials, tunnel dielectrics, ferroelectric materials, reliability, failure analysis, quality assurance & testing, modeling & simulation, integrated circuits, new concept technologies, and new applications & systems (solid state disks, memory cards, programmable logic,-).

Invited speakers:

"Floating gate type nonvolatile memory reliability issues"

G. Tempel (Infineon, Germany)

"Current FeRAM technology developments and scaling towards 3-D capacitor cells"

D. Wouters (IMEC, Belgium)

"32Mb Chain FeRAM-An Overview"

D. Takashima (Toshiba, Japan)

"Prospect of Emerging Memories"

H. Jeong (Samsung, Korea)

[11] SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

(Chair, T. Enoki, NTT)

Compound-semiconductor devices are playing important roles in wireless and optical communications systems. Future communications systems definitely require devices and circuits that dissipate lower energy, operate at higher bit rates or frequencies, have lower noise, generate higher signal power, and are more compact. This session covers advanced device and IC technologies that meet these challenges through the use of SiGe, GaAs-based, InP-

based, and N-based materials (but not limited). Monolithic ICs or multi-chip modules integrating optical and electrical devices will also be discussed. Papers demonstrating breakthroughs and novel concepts, discussing on potentials and limitations, and addressing issues in these technologies are strongly solicited for this session.

Invited speakers:
"High-Performance, Low-Cost SiGe:C BiCMOS Technology"
B. Tillack (IHP, Germany)
"High-speed III-V HEMT and HBT devices and circuits for ETDM transmission beyond 80 Gbit/s"
R. Quay (Fraunhofer IAF, Germany)
"GaN-based microwave power devices: A survey on the activities in Europe"
J. Wuerfl (Ferdinand-Braun-Institut fuer Hoechstfreguenztechnik, Germany)
"Development of AlGaN/GaN power HFET for the application of an inverter circuit"
S. Yoshida (The Furukawa Electric, Japan)

[12] System-Level Integration and Packaging Technologies

(Chair, K. Takahashi, ASET)

The scope of this subcommittee involves all features of advanced packaging technologies and system-level integration technologies based on packaging technology. Papers are solicited in, but not limited to, the following areas: (1) Advanced packaging technologies including chip size package (CSP), wafer-level package, stacked package, (2) Three-dimensional (3D) integration technology including wafer stacking and chip stacking, (3) System integration technologies including SiP (system-in-package), SoP (system-on-package), opto-electronics integration and MEMS, (4) Design and CAD technologies for the advanced packaging and system integration including interface design, EMI and EMC management and ultra-high speed data transfer technologies, (5) Testing technologies for the system integration including burn-in, known good die (KDG) and design for test (DFT), (6) Modeling and simulation of thermal, mechanical and electrical performance of advanced packaging and system integration.

Invited speakers:
"3D System Integration by Chip-to-Wafer Stacking Technologies"
P. Ramm (Fraunhofer IZM, Germany)
"AC Coupled Interconnect for high density high bandwidth packaging"
P.D. Franzon (North Carolina State Univ., USA)
"System Packaging and Embedded WLP Technologies for Mobile Products"
T. Wakabayashi (Casio, Japan)
"Design, Manufacuturing and Infrastructure for All-in-One SiP Solution"
T. Fujitsu (J-SiP Walton, Japan)

[13] Organic Semiconductor Devices and Materials

(Chair, M. Iwamoto, Tokyo Institute of Technology)

Electronic and Optical processes in organic materials and device application in the following fields (but not limited): (1) Organic transistors, diodes and circuits (2) Organic light emitting devices (3) Organic photodetectors and photovoltaic devices (4) Chemical sensors and gas sensors (5) Fabrication and characterization of organic thin films (6) Electrical and Optical properties of organic thin film and materials (7) Organic-inorganic hybrid systems (8) Interfacial phenomena, LC devices, etc.

Invited speakers:
"Potential Profile and Opto-Electronic Properties at Nano-interface of Conducting Polymer and Metals"
K. Kaneto (Kyushu Institute of Technology, Japan)
"Semiconductor materials design for low-cost plastic thin film transistors"
B. Ong (Xerox, Canada)

[14] Micro-Nano Electromechanical Devices for Bio- and Chemical Applications

(Chair, Y. Miyahara, National Institute for Materials Science)

Micro/nano electromechanical devices (M/NEMS) are now widely applied to biochemical, medical and environmental fields and a new research field called μ-TAS or Lab. on a Chip is expanding and being established. Fusion of microelectronic devices with materials and methods in the chemical, biological, and mediacl fields is expected to open up new scientific and business fields. Papers are solicited in the following areas

(but not limited): (1) Micro/nano electronic mechanical system (M/NEMS) for RF, optical, power and others, (2) μ-TAS and Lab on a chip, (3) Various Bio-chips for DNA, healthcare and proteins, (4) Fabrication technologies and (5) New integrated micro/nano systems for biochemical and medical applications.

Invited speakers:
"Development of an integrated a-Si:H photodiode detector and its evaluation for chemical and biochemical microfluidic analysis"
T. Kamei (Univ. of California, USA)
"DNA chips and their medical applications"
P. Fortina (Thomas Jefferson Univ., USA)

RUMP SESSIONS

The following two Rump Sessions are planned for September 17 (Wednesday).
"What is a guiding principle for CMOS device evolution under 10nm regime and beyond?" (tentative)
Organizer: S. Takagi (Toshiba, MIRAI-ASET)
"What paradigm can nanoelectronic devices bring about?"
Organizer: J. Sone (NEC)
Details on the rump sessions will be announced in the Advance Program.

SHORT COURSES

Two short courses will be held on September 19 (Friday). All lectures are given in Japanese.
"Combined System LSI Pioneering Ubiquitous Society"
Organizer: T. Mogami (NEC)
In the IT society, where network development eliminates information restrictions on time and space, more convenience is pursued for social life. A ubiquitous society is suggested as one of ultimate aspects of the IT society. A variety of new services are suggested in a ubiquitous society that provides an environment connecting every user with anyone or anything, at any time or any place. On the other hand, combined system LSI assumes an extremely important position in realizing a ubiquitous society. In this short course I will lecture on the various types of combined system LSI devices necessary for its realization from an application viewpoint while reviewing what a ubiquitous society is. The course is also expected to be a compass, not only for young researchers or graduate students, but also for front-line

researchers, in considering new diversification of semiconductor technology including future system LSI.

"Broadband Information Society Developed by Innovative Nitride Semiconductors"

Organizer: M. Mizuta (NEC)

The incoming ubiquitous society necessitates a network environment for which customers can reach or store necessary information without regard to whatever technology they are using. An extremely important breakthrough in implementing such a society is to construct a broadband network, either wired or wireless, and a network environment consisting of inexpensive terminals that provide a variety of access. This short course focuses on nitride semiconductor devices that are expected to serve as a driving force for implementing such a future broadband & ubiquitous society. Starting with the description of material properties, front-line engineers give easy-to-understand explanations to you from such application viewpoints as cellular phones, wireless access and storage.

SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference Web site: http://www.intergroup.co.jp/ssdm.

Please note that submissions by post will NOT be accepted.

Deadline for Submission is May 8, 2003.

The two-page paper must be prepared in English in 8.5-×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. The second page should be used to indicate figures, tables and photographs. Detailed format information will be posted on the conference Web site. The paper should report original, previously unpublished work, including specific results.

Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed without opportunity for further revision in the extended abstracts, which will be distributed to conference participants on the opening day of the conference.

Authors of papers accepted for presentation at SSDM 2003 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2004.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract for review to the committee, the author(s) agrees that the work will not be published prior to the presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted to the conference Web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

Late News Paper Deadline is July 25, 2003.

Notices of acceptance will be e-mailed by mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include a plenary session, along with technical sessions comprising solicited papers and those submitted for oral or poster presentation.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for outstanding an contribution to the field of solid

state devices and materials, among papers presented prior to 1997.

SSDM Paper Award
Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award
Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter.

BANQUET

A buffet dinner will be held on the evening of September 16. Additional tickets may be purchased at the registration desk for ¥7,000 each.

REGISTRATION

Participants may register for the conference at the Web site beginning in June.

The registration and banquet fees are:

	Registration Fee		Short Courses (in Japanese)	Banquet
	On or before August 1	After August 1		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Guest(s)				¥4,000/person

VISA REQUIREMENT

All foreign participants must have a valid passport. Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese embassy or consulate as soon as possible.

LOCATION

The Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel) is the perfect place for business, and a pleasant sanctuary in the heart of the city. The Tokyo Metropolitan

Government Building and other skyscrapers tower upwards. JR (Japan Railway) lines and subway lines are within easy walking distance, approximately five minutes from the West Exit of Shinjuku Station.
Keio Plaza Inter-Continental Tokyo Web site: http://www.keioplaza.com/index.html

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT) has been appointed as the official travel agent for the conference and will handle accommodations.

Kinki Nippon Tourist Co., Ltd.
Event, Convention and Congress Department
6F, Kyodo Bldg., 2-2 Kanda-Jimbocho,
Chiyoda-ku, Tokyo 101-0051 JAPAN
Phone:+81-3-3263-5581, Fax:+81-3-3263-5961
E-mail:SSDM2003@knt-tokyo.gr.jp

HOTEL ACCOMMODATIONS

<Available on the nights of September 15(in) - 19(out)>

#	Hotel Name	Single W/bath	Twin W/bath	Location	Grade
①	*Keio Plaza Inter-Continental Tokyo*	¥19,100	¥25,400	Shinjuku Station (walk 5 min)	Deluxe
②	*Hotel SunRoute Tokyo*	¥11,860	¥16,170	Shinjuku Station (walk 3 min)	Superior
③	*Shinjyuku Washington Hotel*	¥12,700	¥15,750	Shinjuku Station (walk 7 min)	Superior

*All room rates include breakfast, service charge and consumption tax.

APPLICATION AND PAYMENT OF DEPOSIT

1. Participants wishing to make reservations for accommodations should submit your reservation form by the "Online Reservation button" after June 1, 2003. Then your application form is transmitted to KNT. Reservation will close at August 15, 2003. Reservation

should be proceeded on first come first served basis. Applications for hotel reservations should be accompanied by a deposit of 10,000yen. Please pay for the balance at the hotel.

2. Payments must be made by either one of the following;
   a. Credit cards (Visa, MasterCard, American Express, JCB) Please fill in the Credit Card Authorization in the application form.
   b. Bank transfer; Please remit the deposit plus a handling charge to the following account.

Name of bank: **Sumitomo Mitsui Banking Corp., Chuo Branch** Name of Account: **Kinki Nippon Tourist Co., Ltd.** Account Number: **1855682**

NOTE: Personal checks are not acceptable. We would appreciate your kindly sending us a photo-copy of the bank's receipt for your remittance.

CANCELLATION

In case of changes or cancellations, please inform KNT by FAX or E-mail. KNT accepts only written notification. The following cancellation fees apply according to the date of your notification.

5 to 2 days prior to the first night	¥1,000
1 day prior to the first night	50% of daily room charge
the first night or no notice given	100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

The temperature in Tokyo during the period of the conference ranges between 18˚C and 24˚C .

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The

frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

ORGANIZING COMMITTEE

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K. Tsutsui (Tokyo Inst. of Technol.)

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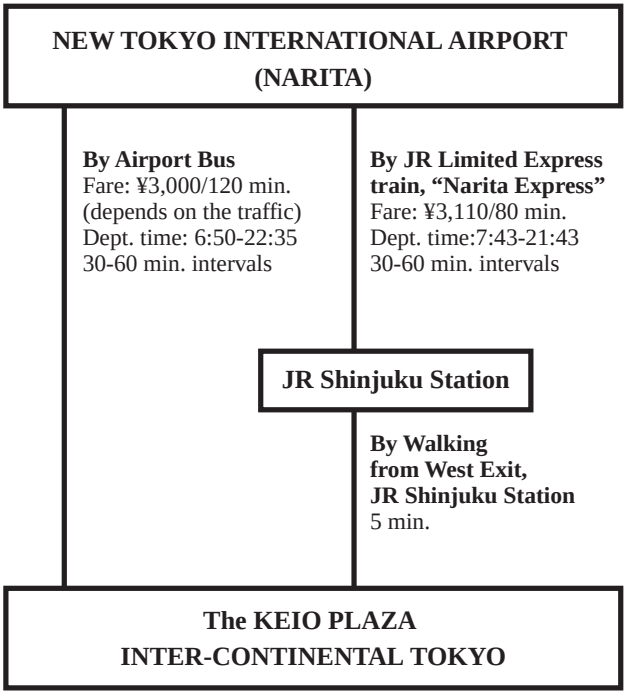

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