Wednesday, September 17

Room A

A-3: Advanced Silicon Devices and Device Physics
-High-k Technology I-
(9:00-10:30)
Chairs: M. Ogawa (Kobe Univ.)
T. Mogami (NEC)

9:00 A-3-1 (Invited)
Integration Issues of HfO_2-Al_2O_3 Laminate for Gate and Capacitor Dielectric
J.-H. Lee[1], *[1]Samsung Electronics Co., Ltd., Korea*

9:30 A-3-2
Influence of Carrier Velocity Related Parameters on the Propagation Delay Time of CMIS Inverters with High-k Gate Dielectrics
M. Ono[1] and A.Nishiyama[1], *[1]Toshiba Corporation, Japan*

9:50 A-3-3
A HfAlOx Gate Dielectric FET Technology Compatible with a Conventional Poly-Si Gate CMOS Process
H. Ohji[1], A. Mutoh[1], K. Torii[1], R. Mitsuhashi[1], A. Horiuchi[1], T. Maeda[1], H. Itoh[1], T. Kawahara[1], K. Hayashi[1], T. Sasaki[1], N. Kasai[1], H. Kitajima[1], M. Yasuhira[1], and T. Arikado[1], *[1]SELETE, Japan*

10:10 A-3-4
A Novel Approach for Determination of Tunneling Mass, m_{eff}-Conduction Band Offset Enegy, E_B Products for Advanced Gate Dielectrics
C.L. Hinkle[1], C. Fulton[1], R.J. Nemanich[1] and G. Lucovsky[1], *[1]North Carolina State Univ., USA*

Room B

B-3: Non-Volatile Memory Technologies
-Non-Volatile Memory III-
(9:00-10:20)
Chairs: K. Takasaki (Fujitsu Labs.)
H. Takada (Mitsubishi Electric)

9:00 B-3-1 (Invited)
Floating gate type nonvolatile memory reliability issues
G. Tempel[1], *[1]Infineon Technologies, Germany*

9:30 B-3-2 (Invited)
The Prospect of New Emerging Memories
H. Jeong[1] and K. Kim[1], *[1]Samsung Electronics, Korea*

10:00 B-3-3
Proposal of New Non-Volatile Memory with Magnetic Nano-Dots
T. Sakaguchi[1], M. Kobayashi[1], M. Takata[2], H. Choi[1], Y.G. Hong[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ. and [2]Asahi Glass Co.*

Room C

C-3: Silicon Process / Materials Technologies
-Memory Technology-
(9:00-10:30)
Chais: T. Kobayashi (Sony)
I. Asano (Elpida)

9:00 C-3-1 (Invited)
0.18 μm Embedded FRAM Fabrication Process and its Consistency with Conventional Logic LSI Process
Y. Horii and T. Eshita[1], *[1]Fujitsu Limited, Japan*

9:30 C-3-2
W-Polymetal Gate with Low W/Poly-Si Interface Resistance for High-Speed/High-Density Embedded Memory
T. Yamashita[1], Y. Nishida[1], K. Hayashi[1], T. Eimori[1], M. Inuishi[1] and Y. Ohji[1], *[1]Renesas Technology Corp., Japan*

9:50 C-3-3
Silicon Selective Epitaxial Growth for Self-Aligned Cell Contact Featuring High Performance Sub-100nm DRAM Cell Transistors
T. Kim[1], Y.P. Kim[1], B.C. Lee[1], S. Choi[1], U.I. Chung[1] and J.T. Moon[1], *[1]Samsung Electronics, Korea*

10:10 C-3-4
Optimum $TiSi_2$ Ohmic Contact Process for Sub-100nm Devices
H.S. Park[1], J.M. Lee[1], S.W. Lee[1], J.H. Park[1], K.J. Moon[1], S.B. Kang[1], G.H. Choi[1], U.I. Chung[1] and J.T. Moon[1], *[1]Samsung Electronics, Korea*

Break

Room D

D-3: Silicon-on-Insulator Technologies
-SOI Novel Devices-
(9:00-10:30)
Chairs: A. Ogura (NEC)
T. Nakai (SUMCO)

9:00 D-3-1 (Invited)
Strained Si MOSFETs on SiGe-on-Insulator (SGOI) for High Performance CMOS Technology
K. Rim[1], B.H. Lee[1], A. Mocuta[1], K. Jenkins[1], S. Bedell[1], H. Chen[1], D. Sadana[1], M. Gribelyuk[1], J. Ott[1], K. Chan[1], L. Shi[1], J. Chu[1], D. Boyd[1], P. Mooney[1], P. O'Neil[1], E. Leobandung[1], and J.J. Welser[1], *[1]SRDC, IBM, USA*

9:30 D-3-2
Fabrication of Ultra-Thin Strained Ge-on-Insulator Substrate by Ge-Condensation Technique
S. Nakaharai[1], T. Tezuka[1], N. Sugiyama[1], Y. Moriyama[1] and S. Takagi[1], *[1]MIRAI ASET, Japan*

9:50 D-3-3
Impact Ionization in Uniaxially Strained-Si MOSFET
N. Watanabe[1], Y. Maeda[1], M. Nishisaka[1] and T. Asano[1], *[1]CMS, Kyushu Inst. of Technology, Japan*

10:10 D-3-4
Quantum Confinement Effect of Ultrathin-SOI on double-gate-nMOSFETs
H. Watanabe[1], K. Uchida[1] and A. Kinoshita[1], *[1]Toshiba Corp., Japan*

Room E

E-3:Quantum Nanostructure Devices and Physics
-Characterization and Nanoprobing-
(9:00-10:15)
Chairs: H. Akinaga (AIST)
M. Sugawara (Univ. of Tokyo)

9:00 E-3-1
Optical characteristics of InAs/GaAs double quantum dots grown by MBE with Indium-Flush method
S. Yamauchi[1,2], K. Komori[1,2], T. Sugaya[1,2] and K. Goshima[1,2], *[1]AIST and [2]CREST-JST, Japan*

9:15 E-3-2
Molecular States of Coupled Zero-Dimensional Structures Imaged Using Low-Temperature Scanning Tunneling Spectroscopy
K. Kanisawa[1], S. Perraud[1,2], H. Yamaguchi[1] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs, [2]ESPCI and [3]CREST-JST, Japan*

9:30 E-3-3
Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by AFM/Kelvin Probe Technique
Y. Darma[1], K. Takeuchi[1] and S. Miyazaki[1], *[1]Hiroshima Univ., Japan*

9:45 E-3-4
Magneto-luminescence of Interdiffused Self-Assembled Quantum Dots
S. Awirothananon[1,2], W. Sheng[1], A. Babinski[3], S. Studenikin[1], S. Raymond[1], P. Hawrylak[1], A. Sachrajda[1], M. Potemski[3], G. Ortner[4] and M. Bayer[4], *[1]National Research Council of Canada, [2]The Univ. of Ottawa, Canada, [3]MPI/FKF and CNRS, France and [4]Universitat Dortmund, Germany*

Room F

F-3:Compound Semiconductor Materials and Devices
-Novel Compound Semiconductors Devices-
(9:00-10:15)
Chairs: K. Akimoto (Tsukuba Univ.)
N. Kobayashi (The Univ. of Electro-Communications)

9:00 F-3-1 (Invited)
Optical and Electrical Control of Ferromagnetism in II-VI Quantum Wells
T. Dietl[1], *[1]Inst. of Physics, Polish Academy of Science, Poland*

9:30 F-3-2 (Invited)
Type-II InAs-based Quantum Cascade Lasers
K. Ohtani[1] and H. Ohno[1], *[1]RIEC, Tohoku Univ., Japan*

10:00 F-3-3
Fabrication of GaN/Alumina/GaN Structure to Reduce Dislocations in GaN
M. Hiroki[1], K. Kumakura[1], T. Makimoto[1], N. Kobayashi[2] and T. Kobayashi[1], *[1]NTT Corporation and [2]Univ. of Electro Communications, Japan*

Room G

G-3:Advanced Silicon Circuits and Systems
-Circuit Techniques for Emerging Technologies-
(9:00-10:30)
Chairs: K. Kotani (Tohoku Univ.)
M. Takamiya (NEC)

9:00 G-3-1 (Invited)
The challenge of analog mix-mode integrated circuit design for brain computer interface
Z. Wang[1], C. Zhang[1], and D. Li[1], *[1]Tsinghua Univ., P.R. China*

9:30 G-3-2
The Vision Chip with Electrical Fovea Motion
Y. Nakagawa[1], J. Deguchi[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ., Japan*

9:50 G-3-3
A Periodic Comparator Operating at 80GHz Based on Single-Flux-Quantum Technology with High Temperature Superconductor
H. Sugiyama[1,2], H. Wakana[2], S. Adachi[2], Y. Tarutani[2] and K. Tanabe[2], *[1]Toshiba Corporation and [2]Superconductivity Research Lab, Japan*

10:10 G-3-4
Ultra Small Random Number Generating Circuits With A Novel Noise Source Device
S. Yasuda[1], H. Satake[1], H. Nozaki[1], T. Tanamoto[1], R. Ohba[1], K. Uchida[1], A. Kinoshita[1] and S. Fujita[1], *[1]Toshiba Corporation, Japan*

Break

Break

Room A	Room B	Room C
A-4: Optoelectronic Devices and Photonic Crystal Devices -VCSELs and Visible Lasers- (10:45-12:00) Chairs: T. Matsuo (NTT) L.A. Coldren (Agility Communications)	**B-4: Non-Volatile Memory Technologies** -Non-Volatile Memory IV- (10:45-12:05) Chairs: K. Yoshikawa (Toshiba) T. Kobayashi (Hitachi)	**C-4: Silicon Process / Materials Technologies** -DRAM- (10:45-12:05) Chais: M. Okuyama (Osaka Univ.) K. Hieda (Toshiba)
10:45 A-4-1 (Invited) 1300nm-Range GaInNAsSb VCSELs A. Kasukawa[1], H. Shimizu[1], C. Setiagung[1], M. Ariga[1], Y. Ikenaga[1], K. Kumada[1], T. Hama and N. Iwai[1], *[1]The Furukawa Electric Co., Ltd., Yokohama R&D Labs, Japan*	**10:45 B-4-1** A 0.18-μm Embedded MNOS-Type Non-volatile Memory for High-Frequency and Low-Voltage Operation N. Matsuzaki[1], T. Ishimaru[1], Y. Okuyama[1], T. Mine[1], H. Kume[1], T. Hashimoto[2], Y. Kanamaru[2], T. Sakai[2], Y. Kawashima[2] and F. Ito[2], *[1]Hitachi, Ltd. and [2]Renesas Technology Corp., Japan*	**10:45 C-4-1** Pt/BST/Pt Capacitor Technology for 0.15μm Embedded DRAM Y. Tsunemine[1], T. Okudaira[1], K. Kashihara[1], A. Yutani[1], H. Shinkawata[1], M. K. Mazumder[1], M. Yoneda[1], Y. Okuno[2], A. Tsuzumitani[2] and Y. Mori[2], *[1]Mitsubishi Electric Corp. and [2]Matsushita Electronics Corp., Japan*
11:15 A-4-2 Improvement of High-Speed Oxide-Confined Vertical-Cavity Surface-Emitting Lasers H.-C. Yu[1,2], S.-J. Chang[1], Y.-K. Su[1], C.-P. Sung[2], H.-P. Yang[2], C.-Y. Huang[2,3], Y.-W. Lin[2], J.-M. Wang[2], F.-I. Lai[4] and H.-C. Kuo[4], *[1]National Cheng Kung Univ., [2]Industrial Technology Research Inst., [3]National Tsing Hua Univ. and [4]National Chiao Tung Univ., Taiwan*	**11:05 B-4-2** 70 nm SONOS Nonvolatile Memory Devices using FN Programming and Hot Hole Erase Method S.D. Chae[1], C.J. Lee[2], J.H. Kim[1], S.K. Sung[2], J.S. Sim[2], M.K. Kim[1], S.W. Yoon[1], B.-G. Park[2], J.W. Lee and C.W. Kim[1], *[1]Samsung and [2]Seoul National Univ., Korea*	**11:05 C-4-2** Low Resistive Contacts of TiN-Barrier and Ru-Electrode Using PCM Sputtering for MIM-Ta_2O_5 Capacitors in Giga-Bit DRAMs Y. Nakamura[1], T. Kawagoe[1], H. Sakuma[1], H. Yamaguchi[1], I. Asano[1], M. Horikawa[1], K. Kuroki[1], K. Tanaka[1], Y. Ueda[1] and H. Goto[1], *[1]Elpida Memory, Inc., Japan*
11:30 A-4-3 High-Power 200-mW 660-nm AlGaInP Laser Diodes with a Low Operating Current R. Hiroyama[1], D. Inoue[1], S. Kameyama[1], A. Tajiri[1], M. Shono[1], M. Sawada[2] and A. Ibaraki[1], *[1]Sanyo electric Co., Ltd. and [2]Tottori Sanyo electric Co., Ltd., Japan*	**11:25 B-4-3** Excellent Electrical Characteristics of SONOS-type Flash Memory with High-k; Dielectric as Trapping Layer and Blocking Layer M. Cho[1], S. Choi[1], H. Hwang[1] and J.W. Kim[2], *[1]Kwangju Inst. of Science and Technology and [2]Samsung Advanced Inst. of Technology, Korea*	**11:25 C-4-3** A Noble SiON/AlO Structure at High-k/poly-Si Interface for Storage Capacitors of High Density DRAMs O. Tonomura[1] and H. Miki[1], *[1]Hitachi, Ltd., Japan*

Room D	Room E	Room F	Room G
	10:00 E-3-5 Optical Time-of-Flight Study of Lateral Exciton Transport in a Strained $Si_{1-x}Ge_x$/Si Multiple Quantum Well K. Sawada[1], N. Yasuhara[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo, Graduate School of Arts and Sciences and [2]PRESTO, JST, Japan*		
	Break		
D-4: Silicon-on-Insulator Technologies -SOI Device Physics- (10:45-12:05) Chairs: O. Nishio (Sharp) T-J. King (UCB)	**E-4: Quantum Nanostructure Devices and Physics** -Spin-related Phenomena- (10:45-12:15) Chairs: A. Takeuchi (Waseda Univ.) T. Dietl (Polish Academy of Science)	**F-4: Compound Semiconductor Materials and Devices** -Optical Devices- (10:45-12:15) Chaisr: T. Matsuoka (NTT) M. Ikeda (Sony)	**G-4: System-Level Integration and Packaging Technologies** -System-Level Integration and Packaging Technologies I- (10:45-11:45) Chairs: K. Fujimoto (Osaka Univ.) M. Kada (Sharp)
10:45 D-4-1 Variable Body Effect Factor FD SOI MOSFET for Ultra-Low Power VTCMOS Applications T. Ohtou[1], T. Nagumo[1] and T. Hiramoto[1], *[1]Univ. of Tokyo, Japan*	**10:45 E-4-1 (Invited)** Control of ferromagnetic order in selectively p-doped GaMnAs-based heterostructures M. Tanaka[1,2], and A. M. Nazmul[1,2], *[1]Univ. of Tokyo, Department of Electronic Engineering, [2]PRESTO-JST, Japan*	**10:45 F-4-1 (Invited)** Developments of High Efficiency In GaN-Based Light-Emitting Diodes J.-I. Chyi[1], C.-C. Pan[1], C.-M. Lee[1], W.-J. Hsu[1], and C.-S. Fang[1], *[1]National Central Univ., Taiwan*	**10:45 G-4-1 (Invited)** 3D System Integration by Chip-to-Wafer Stacking Technologies P. Ramm[1], A. Klumpp[1], R. Merkel[1], J. Weber[1], R. Wieland[1], G. Elst[2] *[1]Fraunhofer Inst., Germany*
11:05 D-4-2 Novel SOI MOSFET with Buried Back-Gate H. Oh[1], H. Choi[1], T. Sakaguchi[1], J. C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ., Japan*	**11:15 E-4-2** Effect of Internal Exchange Coupling on the Curie Temperature in $Ga_{1-x}Mn_xAs$ Trilayer Structures S. Yuldashev[1], Y. Kim[1], N. Kim[1], H. Im[1], T. W. Kang[1], S. Lee[2], Y. Sasaki[3], X. Liu[3] and J. Furdyna[3], *[1]Dongguk Univ., Korea, [2]Korea Univ., Korea and [3]Univ. of Notre Dame, USA*	**11:15 F-4-2** InGaN-based horizontal cavity surface emitting laser diode with selectively grown cavity and outer micromirrors T. Akasaka[1], T. Nishida[1], T. Makimoto[1] and N. Kobayashi[1], *[1]NTT Basic Research Labs, NTT Corporation, Japan*	**11:15 G-4-2** Micro Cu Bump Interconnection on 3D Chip Stacking Technology K. Tanida[1], M. Umemoto[1], N. Tanaka[1], Y. Tomita[1] and K. Takahashi[1], *[1]ASET, Japan*
11:25 D-4-3 Modeling of Fully-depleted SOI Device Variation H. Komatsubara[1], K. Kishiro[1], Y. Kawai[2], N. Miura[1] and K. Fukuda[1], *[1]Oki Electric Industry Co., Ltd. and [2]Miyagi Oki Electric Industry Co., Ltd., Japan*	**11:30 E-4-3** Magnetic Properties of Submicron-sized *p*-$In_{0.97}Mn_{0.03}As$ Ferromagnetic Semiconductor Y. Sekine[1], J. Nitta[1,2], T. Koga[1,3], A. Oiwa[3,4], S. Yanagi[4], T. Slupinski[5] and H. Munekata[4], *[1]NTT [2]CREST [3]PRESTO-JST [4]Tokyo Inst. of Technology, Japan and [5]Warsaw Univesity, Poland*	**11:30 F-4-3** Sub-mW Operation of 308 nm Deep UV LED using quaternary InAlGaN H. Hirayama[1] and Y. Aoyagi[2], *[1]RIKEN and [2]Tokyo Inst. of Technology, Japan*	**11:30 G-4-3** Copper Electrodeposition of High-Aspect-Ratio Vias for Three Dimensional Packaging K. Kondo[1], T. Yonezawa[1], M. Tomisaka[2], H. Yonemura[2], M. Hoshino[2], Y. Taguchi[2] and K. Takahashi[2], *[1]Okayama Univ. and [2]ASET, Japan*

Room A

11:45 A-4-4
High power and high temperature operation of 660 nm AlGaInP laser diodes for DVD-R/RW
Y. Yoshida, H. Nishiguchi, M. Sasaki, S. Abe, A. Ohno, K. Ono, M. Takemi, J. Horie, T. Yagi and E. Omura, [1]*Mitsubishi Electric Corporation, Japan*

Room B

11:45 B-4-4
Data retention improvement of MONOS memories by using silicon-tetrachloride-based silicon nitride with ultra-low Si-H bond density
K. Nomoto[1], G. Asayama[1] and T. Kobayashi[1], [1]*Sony Corporation , Japan*

Room C

11:45 C-4-4
A Highly Reliable TiN/Al_2O_3/TiN MIM Technology for Embedded DRAMs
L.-L. Chao[1], C.D. Wu[1], H.L. Lin[1], Y.L. Tu[1], K.Y. Lin[1], C.Y. Yu[1], C.Y. Chen[1], F.J. Shiu[1], C.T. Ho[1], C.S. Tsai[1], S.-G Wuu and C. Wang[1], [1]*Taiwan Semiconductor Manufacturing Company, Ltd, Taiwan*

Lunch

13:00-15:00 Poster Session (Ohgi)

Room D

11:45 D-4-4
Temperature Dependence of Threshold Voltage and Hot Carrier Degradation of Dynamic Threshold SOI-pMOSFET
Y.-J. Lee[1], T.-S. Chao[1, 2], C.-Y. Huang[1], H.-C. Lin[2] and T.-Y. Huang[1], [1]*National Chiao Tung Univ., Taiwan and* [2]*National Nano Device Labs., Taiwan*

Room E

11:45 E-4-4
Analysis and Control of Rashba Spin-Spliting in One-Dimensional Conductors at Narrow-Gap Single Heterojunctions
T. Kakegawa[1], T. Kita[2], T. Sato[1], M. Akabori[1] and S. Yamada[1], [1]*CNMT, JAIST and* [2]*RIEC, Tohoku Univ., Japan*

12:00 E-4-5
Au/GaAs magnetoresistive-switch-effect devices fabricated by wet etching
Z.G. Sun[1], M. Mizuguchi[1] and H. Akinaga[1], [1]*SYNAF, AIST, Japan*

Room F

11:45 F-4-4
Low Temperature p-GaN rough layer on $In_{0.23}Ga_{0.77}N$/GaN MQW LEDs
L.W. Wu[1], S.J. Chang[1], Y.K. Su[1], W.C. Lai[1,2] and J.K. Sheu[3], [1]*National Cheng Kung Univ.,* [2]*South Epitaxy Corporation and* [3]*National Central Univ., Taiwan*

12:00 F-4-5
Improvement of AlGaInP MQW Light Emitting Diodes by Modification of Ohmic Contact Layer
H.-C. Wang[1], Y.-K. Su[1], C.-L. Lin[1], S.-M. Chen[2] and W.-L. Li[2], [1]*Inst. of Microelectronics and Department of Electrical Engineering and* [2]*Epitech Technology Corporation, Taiwan*

Room G

Lunch

13:00-15:00 Poster Session (Ohgi)

Room A

A-5: Optoelectronic Devices and Photonic Crystal Devices
-Optoelectronic Integrated Devices-
(15:15-16:45)
Chairs: T. Nishimura
(Mitsubishi Electric)
S. Lee
(KIST)

15:15 A-5-1 (Invited)
Monolithic PD-EAM Optical Gates for Ultrafast Signal Processing
S. Kodama[1], T. Yoshimatsu[1] and H. Ito[1], *[1]NTT Corporation, Japan*

15:45 A-5-2
InP-based OEIC Photoreceivers Using Shared Layer Integration Technology of Heterojunction Bipolar Transistors and Refracting-Facet Photodiodes
B. Lee[1], Y. Song[1] and K. Yang[1], *[1]KAIST, Korea*

16:00 A-5-3
Solid-State Optical Routing Device Utilizing Minority Carrier Drift
H. Tsukamoto[1], T.D. Boone[1] and J.M. Woodall[1], *[1]Yale Univ., USA*

16:15 A-5-4
Analysis of AlGaAs/GaAs Heterojunction Photodetector with a Two-Dimensional Channel Modulated by Gate Voltage
H. Song and H. Kim, *Korea Electronics Technology Inst., Korea*

Room B

B-5: Organic Semiconductor Devices and Materials
-Preparation and Characterization-
(15:15-16:30)
Chairs: F. Kaneko
(Niigata Univ.)
O. Sugihara
(Tohoku Univ.)

15:15 B-5-1
Controlling the Morphology of Nanostructured Poly(fluoreneethynylene) Film by a Simple Method
K. Tada[1] and M. Onoda[1], *[1]Himeji Inst. of Technol, Japan*

15:30 B-5-2
Anomalous Growth Temperature Dependence of the Surface Roughness of Pentacene Thin Films
M. Tejima[1], T. Komoda[1], K. Kita[1], K. Kyuno[1] and A. Toriumi[1], *[1]The Univ. of Tokyo, Japan*

15:45 B-5-3
Fabrication and Photoelectrochemical Properties of Polythiophene-Porphyrin Composite Films
T. Akiyama[1], K. Kakutani[1] and S. Yamada[1], *[1]Kyushu Univ., Japan*

16:00 B-5-4
High Resolution Pattern Recording on Photosensitive Urethane-Urea Copolymer Film Surface by Laser Irradiation through Photo-mask
Y. Che[1], O. Sugihara[1], N. Okamoto[1], M. Tomiki[1], M. Tsuchimori[2] and O. Watanabe[2], *[1]Shizuoka Univ. and [2]Toyota Central Research and Development Labs Inc., Japan*

Room C

C-5: Silicon Process / Materials Technologies
-Interconnect-
(15:15-16:45)
Chais: N. Kobayashi
(Selete)
T. Nakamura
(Fujitsu Labs.)

15:15 C-5-1 (Invited)
Stress Migration Phenomena of Cu interconnects
T. Oshima[1], K. Ishikawa[1], T. Saito[1], H. Aoki[1] and K. Hinode[1], *[1]Hitachi, Ltd., Japan*

15:45 C-5-2
Mechanical property control of Low-k Dielectrics for Diminishing CMP-related Defects in Cu-damascene Interconnects
K. Hijioka[1], F. Ito[1], M. Tagami[1], H. Ohtake[1], T. Takeuchi[1], S. Saitoh[1] and Y. Hayashi[1], *[1]NEC Corporation, Japan*

16:05 C-5-3
The Delamination Mechanism of Porous Low-k Film during the Cu-CMP Process
S. Kondo[1], T. Nasuno[1], S. Ogawa[1], S. Tokitou[1], B. U. Yoon[1], A. Namiki[2], Y. Sone[2], K. Misawa[1], T. Yoshie[1], K. Yoneda[1], M. Shimada[1], S. Sone[1], H.J. Shin[1], N. Ohashi[1], I. Matsumoto[1] and N. Kobayashi[1], *[1]SELETE and [2]Novellus Systems Japan, Inc., Japan*

16:25 C-5-4
In-situ Measurement of Friction Force during Cu Chemical Mechanical Polishing
H. Matsuo[1], A. Ishikawa[1] and T. Kikkawa[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC, AIST and [3]RCNS, Hiroshima Univ., Japan*

Room D

D-5: Silicon-on-Insulator Technologies
-Fin FET Technologies-
(15:15-16:45)
Chairs: H. Matsuhashi
(Oki Electric)
K. Rim
(IBM)

15:15 D-5-1 (Invited)
FinFET Promise and Challenges
T.-J. King[1], *[1]Univ. of California, USA*

15:45 D-5-2
High-Aspect Ratio Gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation of Silicon Gate
A. Katakami[1], K. Kobayashi[2] and H. Sunami[2], *[1]Fujitsu Labs Limited and [2]Hiroshima Univ., Japan*

16:05 D-5-3
An Experimental Study of The Cross-Sectional Channel Shape Dependence of Short-Channel Effects in Fin-Type Double-Gate MOSFETs
Y. Liu[1], K. Ishii[1], M. Masahara[1], T. Tsutsumi[2], H. Takashima[1] and E. Suzuki[1], *[1]AIST and [2]Meiji Univ., Japan*

16:25 D-5-4
P-channel Vertical Double-Gate MOSFET Fabrication by Ion-Bombardment-Retarded Etching
M. Masahara[1], T. Matsukawa[1], S. Hosokawa[1], K. Ishii[1], Y. Liu[1], H. Tanoue[1], K. Sakamoto[1], H. Yamauchi[1], S. Kanemaru[1] and E. Suzuki[1], *[1]AIST, Japan*

Room E

E-5:Quantum Nanostructure Devices and Physics
-Single Electron Transport-
(15:15-16:30)
Chairs: Y. Ohno
(Tohoku Univ.)
A. Shields
(Toshiba Cambridge)

15:15 E-5-1 (Invited)
Nuclear spin dependent transport in quantum dots
K. Ono[1], and S. Tarucha[1,2,3], *[1]Univ. of Tokyo, [2]NTT Basic Research Labs, [3]ERATO-JST, Japan*

15:45 E-5-2
Single Electron Transport through Single InAs Quantum Dots Probed by Nanogap Electrodes
M. Jung[1] and K. Hirakawa[1,2], *[1]Univ. of Tokyo and [2]CREST-JST, Japan*

16:00 E-5-3
Investigation of Electron Transition Energy for Vertically Coupled InAs/GaAs Semiconductor Quantum Dots and Rings
Y. Li[1,2] and H.-M. Lu[3], *[1]National Nano Device Labs, [2]National Chiao Tung University and [3]Univ. of Illinois at Chicago, USA*

16:15 E-5-4
1-bit BDD full adder circuit using single electron transistors by selective area metalorganic vapor phase epitaxy
Y. Miyoshi[1], F. Nakajima[2], J. Motohisa[1] and T. Fukui[1], *[1]Hokkaido Univ. and [2]NTT, Japan*

Room F

F-5:Micro-Nano Electromechanical Devices for Bio- and Chemical Applications
-Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - I-
(15:15-16:45)
Chaisr: Y. Miyahara
(NIMS)
M. Kamahori
(Hitachi)

15:15 F-5-1 (Invited)
DNA Chips and Their Medical Applications
P. Fortina[1], L.J. Kricka[2], and S. Surrey[1], *[1]Thomas Jefferson Univ., USA [2]Hospital of the Univ. of Pennsylvania*

15:45 F-5-2
Bioluminometry by CMOS-based active pixel photodiode array with accurate background noise compensation
Y. Yazawa[1], M. Kamahori[1] and H. Kambara[1], *[1]Hitachi, Ltd., Japan*

16:00 F-5-3
Detection of DNA Molecules Using Insulated Gate Field Effect Transistor and Intercalator
T. Sakata[1], H. Otsuka[1] and Y. Miyahara[1], *[1]Biomaterials Research Center, National Inst. for Materials Science, Japan*

16:15 F-5-4
Electrostatic Immobilization of Biomolecules using Nano-Electrode Array
T. Yamamoto[1] and T. Fujii[1], *[1]The Univ. of Tokyo, Japan*

Room G

G-5:System-Level Integration and Packaging Technologies
-System-Level Integration and Packaging Technologies II-
(15:15-16:45)
Chairs: K. Takahashi
(ASET.)
M. Kimura
(Mitsubishi Electric)

15:15 G-5-1 (Invited)
Design, Manufacturing and Infrastracture for All-in-One SiP Solution
T. Fujitsu[1], *[1]J-SiP Walton, Japan*

15:45 G-5-2 (Invited)
System Packaging and Embedded WLP Technologies for Mobile Products
T. Wakabayashi[1], *[1]Casio, Japan*

16:15 G-5-3
Evaluation of Hot-Carrier Hardness and Thick-Film Formation with STP Technique for Seamless Integration Technology
N. Sato[1], N. Shimoyama[1], T. Kamei[2], K. Kudou[2], M. Yano[2], H. Ishii[1] and K. Machida[1], *[1]NTT Corporation and [2]NTT Advanced Technology Corporation, Japan*

16:30 G-5-4
New Process of Self-organized Interconnection in Packaging by Conductive Adhesive with Low Melting Point Filler
K. Yasuda[1], J.-M. Kim[1], M. Yasuda[1] and K. Fujimoto[1], *[1]Osaka Univ., Japan*

Room A	Room B	Room C
16:30 A-5-5 Enhancement of Magneto-Optic Effect in Magneto-Optic Waveguide with Low Refractive Index Undercladding Layer Y. Shoji[1,2], H. Yokoi[1,2] and T. Mizumoto[1], *[1]Tokyo Inst. of Technology and [2]OITDA, Japan*	**16:15 B-5-5** Electrical Properties and Gas Response in Alternate Layer-by-Layer Films of Copper Phthalocyanine Dyes K. Kato[1], N. Watanabe[1], S. Katagiri[1], K. Shinbo[1], F. Kaneko[1] and R.C. Advincula[2], *[1]Niigata Univ. and [2]Univ. of Houston, Japan*	
A-6: Optoelectronic Devices and Photonic Crystal Devices -Lasers for Optical Communication- (17:00-18:15) Chairs: H. Shimizu (The Furukawa Electric) M. Nielsen (Denmark Tech. Univ.)	**B-6: Non-Volatile Memory Technologies** -Non-Volatile Memory V- (17:00-17:40) Chairs: K. Saito (NEC) H. Takada (Mitsubishi Electric)	**C-6: Silicon Process / Materials Technologies** -Interconnect- (17:00-18:20) Chais: S. Saito (NEC) J. Koike (Tohoku Univ.)
17:00 A-6-1 (Invited) Advances in Widely -Tunable Optical Transmitters L.A. Coldren[1], *[1]Agility Communications and UC-Santa Barbara, USA*	**17:00 B-6-1** Hot Carrier Injection / Fowler Nordheim Erase Silicon Nanocrystal Memory Cell Rajesh Rao[1], Robert Steimle[1], M. Sadd[1], C. Swift[1], R. Muralidhar[1], B. Hradsky[1], S. Straub[1], E. Prinz[1], J. Yater[1] and B. White[1], *[1]Motorola SPS, USA*	**17:00 C-6-1** High-modulus Porous MSQ Films for Cu/Low-k Integration (keff<2.7) K. Misawa[1], S. Sone[1], H. Shin[1], K. Inukai[1], Y. Sudo[1], S. Kondo[1], B.U. Yoon[1], S. Tokitoh[1], K. Yoneda[1], T. Yoshie[1], N. Ohashi[1] and N. Kobayashi[1], *[1]SELETE, Japan*
17:30 A-6-2 40 GHz Actively Mode-Locked DBR Laser Diode Module with an Impedance Matching Circuit S. Arahira[1] and Y. Ogawa[1], *[1]Oki Electric Industry Co., Ltd., Japan*	**17:20 B-6-2** A New Investigation on Erase V_T Variation of NOR Flash fabricated with 90 nm Technology T.Y. Kim[1], W.H. Lee[1], J.I. Han[1], S.E. Lee[1], H.G. Lee[1], S.Y. Kim[1], J.H. Park[1], M.K. Cho[1], Y.H. Song[1] and K. Kim[1], *[1]Samsung Electronics, Korea*	**17:20 C-6-2** Control of Pore Size and Porosity in Periodic Porous Silica Low-k Films N. Hata[1,2], C. Negoro[2], K. Yamada[3] and T. Kikkawa[1,4], *[1]MIRAI-ASRC, AIST, [2]ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*
17:45 A-6-3 Very High Frequency Self-Pulsation and Stable Optical Injection Locking for Well-Difined Multi-Electrode DFB Lasers S. Nishikawa[1,2], M. Gotoda[1,2], T. Nishimura[1,2], Y. Tokuda[1,2] and K. Matsumoto[1,2], *[1]Mitsubishi Electric Corporation and [2]OITDA, Japan*		**17:40 C-6-3** Off-time Dependence of Pulsed DC Electromigration MTF of Cu Multilevel Interconnection K. Oshima[1], T. Ishida[1], S. Miyazaki[1], T. Takahagi[1] and S. Shingubara[1], *[1]Hiroshima Univ., Japan*

Room D	Room E	Room F	Room G
		16:30 F-5-5 Microfluidic Devices Integrated with Parmalloy Micropatterns for Manipulating Magnetic Beads N. Ichikawa[1], F. Omasu[2], Y. Nagasaki[3] and T. Ichiki[1,2], *[1]Toyo Univ., [2]PRESTO and [3]Tokyo Univ. of Science, Japan*	
D-6: New Materials and Characterization -Si/SiGe Devices and Materials- (17:00-18:30) Chairs: J. Murota (Tohoku Univ.) A. Sakai (Nagoya Univ.)	**E-6:Novel Devices, Physics, and Fabrication** -Nanoprocess and Nanodevices- (17:00-18:30) Chairs: M. Tabe (Sizuoka Univ.) Y. Takahashi (NTT)	**F-6:Micro-Nano Electromechanical Devices for Bio- and Chemical Applications** -Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - II- (17:00-18:00) Chairs: H. Tabata (Osaka Univ.) K. Shimoide (Asahi Kasei)	**G-6:System-Level Integration and Packaging Technologies** -System-Level Integration and Packaging Technologies III- (17:00-18:15) Chairs: M. Aoyagi (AIST) H. Ezawa (Toshiba)
17:00 D-6-1 (Invited) SiGe in Advanced CMOS Devices-an unique material equally helpful when present or absent T. Skotnicki[1], *[1]STMicroelectronics, Crolled, France*	**17:00 E-6-1 (Invited)** Nanoimprint Lithography–An Enabling Engine to Nanotechnology S.Y. Chou[1], *[1]Princeton Univ., USA*	**17:00 F-6-1 (Invited)** Development of an integrated a-Si:H photodiode detector and its evaluation for chemical and biochemical microfluidic analysis T. Kamei[1,3], B.M. Paegel[1], E.T. Lagally[1], A.M. Skelley[1], J.R. Scherer[1], R.A. Street[2], and R.A. Mathies[1], *[1]Univ. of California at Barkeley and [2]Palo Alto Research Center*	**17:00 G-6-1 (Invited)** AC Coupled Interconnect for High-Density High-Bandwidth Packaging P. Franzon[1], S. Mick[1], J. Wilson[1], L. Luo[1], K. Chandrasakhar[1], *[1]NC State Univ., USA*
17:30 D-6-2 Structural Characterization of Strained Silicon Substrates by X-Ray Diffraction and Reflectivity M. Erdtmann[1], T. Langdo[1], C. Vineis[1], H. Badawi[1] and M. Bulsara[1], *[1]AmberWave Systems Corp., USA*	**17:30 E-6-2** Photon-induced effect on single-charge-tunneling in a Si multidot Schottky FET R. Nuryadi[1], H. Ikeda[1], Y. Ishikawa[1] and M. Tabe[1], *[1]Shizuoka Univ., Japan*	**17:30 F-6-2** Resonant Cavity Thin Film Photodiode for Compact Displacement Sensor M. Sasaki[1], F. Nakai, X. Mi, K. Hane, *[1]Tohoku Univ., Japan*	**17:30 G-6-2** Inter-chip Wireless Interconnection using Si Integrated Antenna A.B.M. H.-U. Rashid[1], S. Watanabe[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*
17:50 D-6-3 Oxidation-Induced Damages on Germanium MIS Capacitors with HfO_2 Gate Dielectrics K. Kita[1], M. Sasagawa[1], K. Tomida[1], K. Kyuno[1] and A. Toriumi[1], *[1]The Univ. of Tokyo, Japan*	**17:45 E-6-3** Room-Temperature Observation of Negative Differential Conductance Due to Large Quantum Level Spacing in Silicon Single-Electron Transistor M. Saitoh[1] and T. Hiramoto[1], *[1]Univ. of Tokyo, Japan*	**17:45 F-6-3** RF Propagation Characteristics and pH Measurement for in vivo Wireless Healthcare Chip T. Yamada[1], H. Uesugi[1], K. Okada[1], K. Masu[1], H. Nakase[2], T. Kazuo[2], A. Oki[3] and Y. Horiike[3] *[1]Tokyo Inst. of Technology, [2]RIEC, Tohoku Univ. and [3]National Inst. for Materials Science, Japan*	**17:45 G-6-3** Magnetic Near-Field Mappings over Fine Circuits by Fiber-Edge Magneto-Optic Probe M. Iwanami[1], S. Hoshino[1], M. Kishi[2] and M. Tsuchiya[2], *[1]ASET and [2]Univ. of Tokyo, Japan*

Room A

18:00 A-6-4
Lasing-Wavelength-Change-Suppression 980 nm Pump Laser Diodes for Metro Applications
K. Kawasaki[1], K. Shigihara[1], H. Matsuoka[1], Y. Kunitsugu[1], T. Yagi[1], E. Omura[1] and Y. Mitsui[1], *[1]Mitsubishi Electric Corporation, Japan*

18:45-20:45
Rump Session A
"Can channel material/structure engineering become a guiding principle for future CMOS device technology?"

Room B

18:45-20:45
Rump Session B
"What paradigm can nanoelectronic devices bring about?"

Room C

18:00 C-6-4
CVD-Al/Flow-Al Technology for Filling Large Aspect Ratio Contact Holes
M. Sakamoto[1], T. Aoki[1], K. Masu[1], S.J. Lim[2], M. Hatanaka[2], M. Ishikawa[2] and Y. Furumura[3], *[1]Tokyo Inst. of Technology, [2]ULVAC Inc. and [3]Philbridge Inc., Japan*

Room D

18:10 D-6-4
Enhanced Metal-Induced Lateral Crystallization in Amorphous Ge/Si Layered Structure by Precursor Modulation
H. Kanno[1], A. Kenjo[1], T. Sadoh[1] and M. Miyao[1], *[1]Kyushu Univ., Japan*

Room E

18:00 E-6-4
Analytical SPICE Modeling of Realistic MOS-based Single-Electron Transistors –"MOSETs" with a Unique Distribution Function in the Coulomb Oscillation Region
K.R. Kim[1], K.-W. Song[1], G. Baek[1], H.H. Kim[1], J.I. Huh[1], J.D. Lee[1] and B.-G. Park[1], *[1]Seoul National Univ., Korea*

18:15 E-6-5
Analysis of Back-Gate Voltage Dependence of Threshold Voltage of Thin SOI MOSFET and Its Application to Si Single-Electron Transistor
S. Horiguchi[1], A. Fujiwara[1], H. Inokawa[1] and Y. Takahashi[1], *[1]NTT Basic Research Labs, Japan*

Room F

Room G

18:00 G-6-4
Variable RF Inductor on Si CMOS Chip
S. Gomi[1], Y. Yokoyama[1], H. Sugawara[1], H. Ito[1], K. Okada[1], H. Hoshino[2], H. Onodera[2] and K. Masu[1], *[1]Tokyo Inst. of Technology, and [2]Kyoto Univ., Japan*

POSTER SESSION (13:00-15:00, OHGI)

P1
Advanced Silicon Circuits and Systems
(6 Papers)

P1-1
Bank-Type Multiport Register File for Highly-Parallel Processors
T. Sueyoshi[1], H. Uchida[1], Y. Mitani[2], K. Hiramatsu[2], H.J. Mattausch[1], T. Koide[1] and T. Hironaka[2], *[1]Hiroshima Univ. and [2]Hiroshima City Univ., Japan*

P1-2
Three-Dimensionally Stacked Analog Retinal Prosthesis Chip
J. Deguchi[1], T. Watanabe[1], T. Nakamura[1], Y. Nakagawa[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ., Japan*

P1-3
Low-Voltage-Triggered PNP for ESD Protection in Mixed-Voltage I/O interface
M.-D. Ker[1], W.-J. Chang[1] and W.-Y. Lo[2], *[1]National Chiao-Tung Univ., and [2]Silicon Intergrated Systems (SiS) Corp., Taiwan*

P1-4
75-qubit Quantum Computing Emulator
M. Fujishima[1], K. Inai[1], T. Kitasho[1] and K. Hoh[1,2], *[1]The Univ. of Tokyo and [2]CREST-JST, Japan*

P1-5
Efficient Suppression of Substrate Noise Coupling in CMOS Technology
W.-K. Yeh[1], S.-M. Chen[2], C.-M. Lai[2] and Y.-K. Fang[2], *[1]National Univ. of Kaohsiung and [2]National Cheng-Kung Univ., Taiwan*

P1-6
All Digital One-chip Wireless Modem LSI with Acquisition Circuit
Y. Sakai[1], H. Nakase[1], Y. Isota[1] and K. Tsubouchi[1], *[1]Tohoku Univ., Research Inst. of Electorical Communication, Japan*

P2
Advanced Silicon Devices and Device Physics
(17 Papers)

P2-1
Efficient Improvement of Hot-Carrier-Induced Degradation for Sub-0.1μm CMOSFET
C.-M. Lai[1], C.-C. Hu[2], J.-C. Lin[3], S.-T. Pan[2] and W.-K. Yeh[4], *[1]Inst. of National Cheng Kung Univ., [2]Shu-Te Univ., [3]National Chiao-Tung Univ. and [4]National Univ. of Kaohsiung, Taiwan*

P2-2
Optimization of STI Stress and Active Geometry Configuration for Advanced CMOS Devices
T. Lin[1], Y. Gong[1], J.T. Tseng[1], L. Yu[1], T. Shen[1], D. Chen[1], T.P. Chen[1], C.L. Kuo[1], W.T. Shiau[1] and J.K. Chen[1], S.C. Chien and S.W.Sum, *[1]United Microelectronics Corporation, Taiwan*

P2-3
Modeling of Pocket Implant Effect on Drain Current Flicker Noise in High Performance Analog CMOS Devices
J.-W.Wu[1], J.C. Guo[2], K.-L. Chiu[1], C.-C. Cheng[1], W.Y. Lien[2], G.W. Huang[3] and T. Wang[1], *[1]National Chiao-Tung Univ., [2]Taiwan Semiconductor Manufacturing Company, and [3]National Nano Device Labs, Taiwan*

P2-4
Novel Substrate Engineering for High Performance CMOSFETs using Channeling Ion Implantation
M. Kitazawa[1], T. Yamashita[1], Y. Kawasaki[1], T. Kuroi[1], T. Eimori[1], M. Inuishi[1] and Y. Ohji[1], *[1]Renesas Technology Corp., Japan*

P2-5
A New Stable Extraction of Threshold Voltage Using Regularization Method
W.Y. Choi[1,2], B.Y. Choi[1,2], D.-S. Woo[1,2], M.W. Lee[1,2], J.D. Lee[1,2] and B.-G. Park[1,2], *[1]Inter-univ. Semiconductor Research Center (ISRC) and [2]Seoul National Univ., Korea*

P2-6
A New Approach to Gate Dielectric Integrity Based on Differences Between i)Strained and ii) Strain-Free Interfacial Regions: *Applications to Devices with Alternative High-k Dielectrics*
G. Lucovsky[1], J.C. Phillips[2] and P. Boolchand[3], *[1]North Carolina State Univ., [2]Rutgers Univ. and [3]Univ. of Cincinnati, USA*

P2-7
A Variable Channel-Size MOSFET with LDD Structure
N. Nakanose[1], Y. Arima[1], T. Asano[1], Y. Kosasayama[2], M. Ueno[2] and M. Kimata[2], *[1]Kyushu Inst. of Technology and [2]Mitsubishi Electric Corp., Japan*

P2-8
Novel ESD Protection Design for Nanoscale CMOS Integrated Circuits
M.-D. Ker[1] and T.-K. Tseng[2], *[1]National Chiao-Tung Univ., Taiwan and [2]Industrial Technology Research Inst., Taiwan, Taiwan*

P2-9
A New One-Transistor One-Bipolar (1T1B) Capacitor-Less DRAM Cell
J.-K. Park[1] and J. Woo[1], *[1]Univ. of California at Los Angeles, USA*

P2-10
On-current Modeling of poly-Si TFT
K.C. Moon[1], S.-H. Kang[1] and M.-K. Han[1], *[1]Seoul National Univ., Korea*

P2-11
Characterization and Modeling of High Q-Factor, High Resonant Frequency Spiral Inductors with 6 μm thick Top-Metal for RF-IC Applications
Y.-S. Lin[1], H.-W. Chiu[2], S.-H. Wu[1] and S.-S. Lu[2], *[1]National Chi-Nan Univ., [2]National Taiwan Univ., Taiwan*

P2-12
Design Issues for Sub-100nm Analog CMOS
M. Garg[1], S. Suryagandh[1] and J. Woo[1], *[1]Univ. of California Los Angeles, USA*

P2-13
Split Gate Engineering for RF/Analog Application In Sub 50 nm NMOSFET
J. Yuan[1] and J. Woo[1], *[1]Univ. of California, Los Angeles, USA*

P2-14
A Simple Wide-Band MIM Capacitor Model for RF Applications and the Effect of Substrate Grounded Shields
S.-S. Song[1], S.-W. Lee[1], J. Gil[1] and H. Shin[2], *[1]Korea Advanced Insititute of Science and Technology and [2]Seoul National Univ., Korea*

P2-15
Improvement on Turn-on Speed of Substrate-Triggered SCR Device by Using Dummy-Gate Structure for On-Chip ESD Protection
K.-C. Hsu[1] and M.-D. Ker[1], *[1]National Chiao-Tung Univ., Taiwan*

P2-16
A new Conductivity Modulated LDMOSFET employing Buried P Region and P+ Drain
J.-K. Oh[1], B.-C. Jeon[1], M.-K. Han[1] and Y.-I. Choi[2], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

P2-17
Trench IGBT for the Improved Short Circuit Capability by Employing the Curved Junction and Wide Cell Pitch
S.-S. Kim[1], M.-W. Ha[1], Y.-I. Choi[2] and M.-K. Han[1], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

P3
Silicon Process / Materials Technologies
(19 Papers)

P3-1
Novel Storage-Node Contacts with Stacked PCM-Sp-TiN Barrier for MIM-Ru/Ta_2O_5/Ru Capacitors in Giga-Bit DRAMs
T. Kawagoe[1], Y. Nakamura[1], K. Kuroki[1], I. Asano[1], H. Goto[1] and N. Nakanishi[1], *[1]Elpida Memory, Inc., Japan*

P3-2
Very High Reliability of Ultrathin Silicon Nitride Gate Dielectric Film for sub-100nm Generation
M. Komura[1], M. Higuchi[1], W. Cheng[1], I. Ohshima[2], A. Teramoto[2], M. Hirayama[2], S. Sugawa[1] and T. Ohmi[2], *[1]Tohoku Univ. and [2]NICHe, Tohoku Univ., Japan*

P3-3
Excellent Contact-Hole Etching with NH_3 Added C_4F_8 Pulse-Modulated Plasma
M. Ooka[1] and S. Yokoyama[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-4
Electroless Copper Seed Activated by 1nm ICB-Pd Catalytic Layer for Fine Cu Interconnections
Z. Wang[1], O. Yaegashi[1], H. Sakaue[1], T. Takahagi[1] and S. Shingubara[1], *[1]Hiroshima Univ., Japan*

P3-5
Atomic Order Flattening of Hydrogen-Terminated Si(110) Substrate For Next Generation ULSI Devices
H. Akahori[1], K. Nii[1], A. Teramoto[1], S. Sugawa[2] and T. Ohmi[1], *[1]NICHe, Tohoku Univ. and [2]Tohoku Univ., Japan*

P3-6
An Integrated Gate Stack Process for Sub-90nm CMOS
S.J. Chang[1], S.Y. Wu[1], C.L. Chen[1], T.L. Lee[1], Y.M. Lin[1], Y.S. Tsai[1], H.D. Su[1], S.B. Chen[1], Y.S. Chen[1], M.S. Liang[1], Y.C. See[1] and Y.C. Sun[1], *[1]Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan*

P3-7
Precursors for chemical vapor deposition of NiSi
M. Ishikawa[1], T. Kada[1], H. Machida[1], Y. Ohshita[2] and A. Ogura[3], *[1]TRI Chemical Labs Inc., [2]Toyota Technological Inst. and [3]NEC Corp., Japan*

P3-8
MOCVD $HfAl_xO_y$ Gate Dielectrics Deposited Using Single Cocktail Liquid Source
M.S. Joo[1], B.J. Cho[1], C.C. Yeo[1], S.J. Whoang[2], S. Matthew[3], L.K. Bera[3], N. Balasubramanian[3] and D.-L. Kwong[4], *[1]SNDL, National Univ. of Singapore, [2]Jusung Engineering Co., Ltd., Korea, [3]Inst. of Microelectronics, Singapore and [4]The Univ. of Texas, Austin, Singapore*

P3-9
Tight-Binding Quantum Chemical Molecular Dynamics Simulation on Chemical Mechanical Polishing Process of Cu Surface
N. Isoda[1], K. Sasata[1], T. Yokosuka[1], A. Endou[1], M. Kubo[1], A. Imamura[2] and A. Miyamoto[1,3], *[1]Tohoku Univ., [2]Hiroshima Kokusai Gakuin Univ. and [3]NICHe, Tohoku Univ., Japan*

P3-10
A Novel Photosensitive Porous Low-k Interlayer Dielectric Film
S. Kuroki[1], T. Hirota[2] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ. and [2]TAZMO Co., Ltd., Japan*

P3-11
Increase of Crystallization Temperatures of Ultrathin Al_2O_3 Films Caused by Si Diffusion during Annealing
S. Migita[1], J.-W. Park[2], T. Yasuda[1], M. Nishizawa[1], R. Kuse[2], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-AIST, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*

P3-12
Neutral Beam Etching for Damage-free 50 nm Gate Electrode Patterning
S. Noda[1,2], H. Nishimori[2], T. Ida[3], T. Arikado[2], K. Ichiki[3] and S. Samukawa[1], *[1]Tohoku Univ. [2]Semiconductor Leading Edge Technologies, Inc., [3]Ebara Research Co., Ltd., Japan*

P3-13
Defect Generation in Gate Oxide by Selective Oxidation in Hydrogen-rich Wet Ambient
H.-J. Cho[1], K.-Y. Lim[1], S.-A. Jang[1], J.-H. Lee[1], J.-G. Oh[1], Y.-S. Kim[1], H.-S. Yang[1] and H.-C. Sohn[1], *[1]Hynix Semiconductor Inc., Korea*

P3-14
Improving Electrical Properties of CVD HfO_2 by Multi-Step Deposition and Annealing in a Gate Cluster Tool
C.C. Yeo[1], B.J. Cho[1], M.S. Joo[1], S.J. Whoang[2], D.-L. Kwong[3], L.K. Bera[4], S. Mathew[4] and N. Balasubramanian[4], *[1]National Univ. of Singapore, [2]Jusung Engineering Co., Ltd., [3]The Univ. of Texas at Austin and [4]Inst.s of Microelectronics, Singapore*

P3-15
Influence of Humidity on Electrical Characteristics of Porous Silica Films
S. Sakamoto[1], S. Kuroki[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-16
Chemical structure of N Atoms in the Transition Region of the SiO(N)/Si Interface -A New Spectroscopic Method with Hydrogenation Reaction in HF Acid-
N. Mizuta[1] and S. Watanabe[1], *[1]Fujitsu Labs Ltd, Japan*

P3-17
The sheet resistance instability in the sub-100 nm tungsten poly-metal wordline due to an *in-situ* NH_3 pre-annealing during the sealing nitride deposition
K.-Y. Lim[1], J.-H. Lee[1], H.-J. Cho[1], J.-G. Oh[1], B.-S. Hong[1], S.-A. Jang[1], Y.-S. Kim[1], H.-S. Yang[1] and H.-C. Sohn[1], *[1]Hynix Semiconductor Inc., Korea*

P3-18
Influence of interface layers and bottom electrode on $(Ba,Sr)TiO_3$ thin film leakage current
M. Yamato[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-19
Interface Oxidation Mechanism in HfO_2/Silicon System with Post-Deposition Annealing
H. Shimizu[1], M. Sasagawa[1], K. Kita[1], K. Kyuno[1] and A. Toriumi[1], *[1]The Univ. of Tokyo, Japan*

P4
New Materials and Characterization
(18 Papers)

P4-1
Improving the Accuracy of Modified Shift-and-Ratio Channel Length Extraction Method Using Scanning Capacitance Microscopy
C.W. Eng[1,2], W.S. Lau[1], Y.Y. Jiang[3], D. Vigar[2], K.C. Tee[2], L. Chan[2], S.W.V. Lim[3] and A. Trigg[3], *[1]Nanyang Technological Univ. of Singapore, [2]Chartered Semiconductor Manufacturing Ltd and [3]Inst. of Microelectronics, Singapore*

P4-2
Influence of nitrogen profile on metal workfunction in Mo/SiO_2/Si MOS structure
M. Hino[1], T. Amada[1], N. Maeda[1] and K. Shibahara[1], *[1]RCNS, Hiroshima Univ., Japan*

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Compact Electrical Characterization of Nano-CMOS Transistor with 1.2nm Ultrathin Gate Dielectric
H.S. Kang[1], W.-Y. Quan[2], K.S. Kim[1], C.B. Oh[1], H.J. Ryu[1], C.K. Baek[2], B. Kim[2], Y.W. Kim[1], K.P. Suh[1], and D.M. Kim[2], *[1]Samsung Electronics, [2]Korea Inst. for Advanced Study, Korea*

P4-4
Cross-Hatch Related Oxidation and Reliability of Gate Oxide of Strained-Si/SiGe
M. Nishisaka[1] and T. Asano[1], *[1]Kyushu Inst. of Technology, Japan*

P4-5
Visible Light Irradiation Effects on Atomic-Scale Observations of Hydrogenated Amorphous Silicon Films by Scanning Tunneling Microscopy
K. Arima[1], H. Kakiuchi[1], M. Ikeda[1], K. Endo[2], M. Morita[1] and Y. Mori[2], *[1]Osaka Univ. and [2]Research Center for Ultra-Precision Science and Technology, Osaka Univ., Japan*

P4-6
Influence of structural variation of Ni silicide thin films on electrical property for contact materials
K. Okubo[1], Y. Tsuchiya[1], O. Nakatsuka[1], A. Sakai[1], S. Zaima[1] and Y. Yasuda[1], *[1]Nagoya Univ., Japan*

P4-7
Ultra-shallow Boron Profile Fitting Compensating for Surface Contamination by Utilizing Genetic Algorithms
M. Murakawa[1], K. Shibahara[2], Y. Oda[3], T. Higuchi[1] and K. Nishi[3], *[1]AIST, [2]Hiroshima Univ. and [3]SELETE, Japan*

P4-8
Nucleation-Control in Solid-Phase-Crystallization of a-Si/SiO_2 by Local Ge Insertion
I. Tsunoda[1], K. Nagatomo[1], A. Kenjo[1], T. Sadoh[1], S. Yamaguchi[2] and M. Miyao[1], *[1]Kyushu Univ. and [2]Hitachi, Japan*

P4-9
Atomic-scale Adsorbent Structure of Contaminant Metal on Si(100) Surface and its Effect on Thermal Oxidation
T. Onizawa[1,2], T. Narushima[1,3,4], K. Miki[1,3] and K. Yamabe[2], *[1]NRI, AIST, [2]Univ. of Tsukuba, [3]NML, NIMS and [4]SFI Trinity Nanoscience Lab, Trinity College Dublin, Japan*

P4-10
Effect of Vacuum Annealing on High-k Dy_2O_3 Thin Films Deposited on Si(100)
S. Ohmi[1], H. Yamamoto[1], J. Taguchi[1], K. Tsutsui[1] and H. Iwai[1], *[1]Tokyo Inst. of Technology, Japan*

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Formation of Strained β-$FeSi_2$(Ge) by Ge-Segregation Controlled Solid-Phase Growth of [Amorphous Si/FeSiGe]$_n$ Multi-Layered Structure
T. Sadoh[1], M. Owatari[1], A. Kenjo[1], T. Yoshitake[1], M. Itakura[1] and M. Miyao[1], *[1]Kyushu Univ., Japan*

P4-12
Electrical properties of crystalline γ-Al_2O_3 films using conductive-AFM and MISFETs with Aluminum gates
T. Okada[1], R. Ito[1], M. Shahjahan[1], K. Sawada[1] and M. Ishida[1], *[1]Toyohashi Univ. of Technology, Japan*

P4-13
Wet Etching Characteristics of both As-deposited and Annealed Al_2O_3 and $HfAlO_x$ Films
T. Nishimura[1], R. Kuse[2], K. Tominaga[2], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI project, ASRC, AIST, [2]MIRAI ASET and [3]The Univ. of Tokyo, Japan*

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Impact of Ti/TiN (Glue/Barrier Layer) Formation on Ultra-thin Gate Oxide Reliability (HCI and NBTI) for Deep Sub-micron CMOS Transistors
C. Liu[1], M.G. Chen[1], Y.R. Yang[1] and Y.T. Loh[1], *[1]UMC, Taiwan*

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Characterization and Comparison of Strained $Si_{1-y}C_y$ MOSFET Grown by Gas Source MBE and Hot Wire Cell Method
T. Watahiki[1], K. Abe[2], A. Yamada[2] and M. Konagai[1], *[1]Tokyo Inst. of Technology, [2]Shinshu Univ., Japan*

P4-16
Effect of Nitrogen Annealing on the Electrical Properties of Ultrathin Crystalline γ-Al_2O_3 High-κ Dielectric Films Deposited on Si(111) Substrates
M. Shahjahan[1], T. Okada[1], K. Sawada[1] and M. Ishida[1], *[1]Toyohashi Univ. of Technology, Japan*

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Electrical properties and conduction mechanism of ZrO_2 films on $Si_{1-y}C_y$
G.K. Dalapati[1], S.K. Samanta[2], S. Chatterjee[3], P.K. Bose[4], S. Varma[5], S. Patil[6] and C.K. Maiti[7], *[1]IIT Kharagpur, [2]Jadavpur Univ., [3]Inst. of Physics, Bhubaneswar, India*

P4-18
Failure Mechanism of Nano-crystalline VN barrier in Cu/VN/SiO_2/Si system
T. Itoi[2], O. Yanada[3], K. Satoh[4], B.M. Takeyama[1] and A. Noya[1], *[1]Kitami Inst. of Technology, [2]Chiba Univ., [3]SEC Ltd. and [4]Hitachi Kokusai Electric Inc., Japan*

P5
Compound Semiconductor Materials and Devices
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P5-1
Metal-Semiconductor-Metal UV Photodetector Based on AlGaN/GaN Heterostructure
H. Jiang[1], T. Egawa[1], H. Ishikawa[1], Y. Dou[1], C. Shao[1] and T. Jimbo[1], *[1]Nagoya Inst. of Technology, Japan*

P5-2
Low Frequency Noise Caused by Substrate Current in AlGaAs/InGaAs HEMTs
M. Wada[1], S. Nishiyama[1], T. Nakamoto[1] and K. Higuchi[1], *[1]Hiroshima Univ., Japan*

P5-3
Electro Static Discharge effects on AlGaN/GaN HEMTs on sapphire substrates
S.-C. Lee[1], J.-C. Her[1], K.-S. Seo[1] and M.-K. Han[1], *[1]Seoul National Univ., Korea*

P5-4
Study of InGaP/InGaAs Double Doped Channel Heterostructure Field-effect Transistor (DDCHFET)
H.-M. Chuang[1], C.-Y. Chen[1], P.-H. Lai[1], S.-I. Fu[1], Y.-Y. Tsai[1], C.-I. Kao[1] and W.-C. Liu[1], *[1]Inst. of Microelectronics, National Cheng-Kung Univ., Taiwan*

P5-5
Nitride-based blue LEDs with GaN/SiN double buffer layers
C.-H. Kuo[1], S.-J. Chang[1], Y.-K. Su[1], C.-K. Wang[1], L.-W. Wu[1], J.-K. Sheu[2] and J.-M. Tsai[3], *[1]National Cheng Kung Univ., [2]National Central Univ. and [3]South Epitaxy Corporation, Taiwan*

P5-6
Thermal Annealing Effect in GaInNAs Thin Films Estimated by X-ray Absorption Fine Structure Spectroscopy
K. Uno[1], M. Yamada[1], T. Takizawa[2] and I. Tanaka[1], *[1]Fac. Systems Eng., Wakayama Univ. and [2]Matsushita Elec. Co., Ltd., Japan*

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A Double-Barrier-Emitter Triangular Barrier Optoelectronic Switch
J.-Y. Chen[1], D.-F. Guo[2], K.-M. Lee[1], H.-M. Chuang[1], C.-Y. Chen[1] and W.-C. Liu[1], *[1]National Cheng-Kung Univ. and [2]Chinese Air Force Academy, Taiwan*

P5-8
GaAs-MISFETs with nm-Thin Gate Insulating Films Formed by Oxi-Nitridation Process
M. Takebe[1], N.C. Paul[1], K. Nakamura[1], K. Iiyama[1] and S. Takamiya[1], *[1]Kanazawa Univ., Japan*

P5-9
Characterization of Threading Dislocation in Si-doped GaN Films by High Spatial Resolution Cathodoluminescence Spectroscopy
R. Sugie[1], M. Yoshikawa[1] and H. Harima[2], *[1]Toray Research Center Inc. and [2]Kyoto Inst. of Technology, Japan*

P5-10
Characterization of AlInAsSb/GaInAsSb Multiple Quantum Wells Grown by MOVPE
Y.-K. Su[1], C.-H. Wu[1] and J.-R. Chang[2], *[1]Inst. of Microelectronics, National Cheng Kung Univ., [2]Epistar Corporation, Taiwan*

P5-11
Growth Temperature Dependence of Nitrogen Incorporation in GaNAs Grown by Chemical Beam Epitaxy
Y. Sun[1], M. Yamamori[1], T. Egawa[1] and H. Ishikawa[1], *[1]Nagoya Inst. of Technology, Japan*

P5-12
Al-doped ZnO Intermediate Layer for AlGaN/GaN HEMT Ohmic Contact
K. Nishizono[1], M. Okada[1], M. Kamei[1], D. Kikuta[1], J.-P. Ao[1], K. Tominaga[1] and Y. Ohno[1], *[1]The Univ. of Tokushima, Japan*

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Optoelectronic Devices and Photonic Crystal Devices
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P6-1
Investigation of Nonreciprocal Phase Shift Characteristics for Integrated Optical Waveguide Isolators Utilizing Magnetic Photonic Crystals
J.S. Yang[1], G. Lee[1], T.H. Lee[1], Y.-I. Kim[1], M.-C. Park[1], Y.T. Byun[1], D.H. Woo[1], S. Lee[1], S.H. Song[2] and S.H. Kim[1], *[1]Korea Inst. of Science and Technology and [2]Hanyang Univ., Korea*

P6-2
Magnetooptic Spatial Light Modulator with One-Step Pattern Growth on Ion-Milled Substrates by Liquid-Phase Epitaxy
J.-H. Park[1,3], J.-K. Cho[2], K. Nishimura[1], H. Uchida[1] and M. Inoue[1,4], *[1]Toyohashi Univ. of Technology, Japan, [2]Gyeongsang National Univ., Korea, [3]ASTF and [4]CREST-JST, Japan*

P6-3
Optical Properties of Acrylate-Based Negative-Type Photoresist and Fabrication of Optical Waveguides
P. Gutafik[1], O. Sugihara[2] and N. Okamoto[1], *[1]Shizuoka Univ. and [2]Tohoku Univ., Japan*

P6-4
Optical Tuning of Defect-Induced Pass-Band in Photonic Crystal Waveguide
M. Tsuji[1], Y. Iida[1] and Y. Omura[1], *[1]Kansai Univ., Japan*

P6-5
Numerical Analysis of Waveguides in Three-Dimensional Photonic Crystal with Finite Thickness
Y. Watanabe[1], N. Yamamoto[1,2] and K. Komori[1], *[1]AIST and [2]CREST, JST, Japan*

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Fabrication of Wide Area Two-Dimensional Photonic Crystal Using Holographic Lithography
J.I. Moon[1], S.H. Kim[1], S.H. Park[1] and Y.T. Lee[1], *[1]Kwangju Inst. of Science Technology, Korea*

P6-7
A Study of Magnetostriction and Its Application to Silicon-on-Insulator Waveguides
P.S. Chan[1] and H.K. Tsang[1], *[1]The Chinese Univ. of Hong Kong., China*

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Blue Luminescence of Porous Alumina Membranes Prepared by Anodic Oxidation
T. Echizenya[1], K. Takase[1], Y. Takahashi[1], Y.Takano[1] and K. Sekizawa[1], *[1]Nihon Univ., Japan*

P6-9
AlGaAs/InGaAs DFB Laser by One Time Selective MOCVD Growth on a Grating Substrate
Y. Takasuka[1,2], K. Yonei[2], H. Yamauchi[1] and M. Ogura[1], *[1]AIST and [2]Shibaura Inst. of Technology, Japan*

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InGaN/GaN Light Emitting Diodes with a Lateral Current Blocking Structure
W.-B. Chen[1], Y.-K. Su[1], C.-L. Lin[1], H.-C. Wang[1] and S.-M. Chen[2], *[1]National Cheng Kung Univ., and [2]Epitech Technology Corporation, Taiwan*

P6-11
Characteristics of P-I-i-I-N GaAs/$Al_{0.35}Ga_{0.65}As$ Phase Modulator and MultiMode Interference Used in the TE/TM Mode Splitter
S.-P. Kim[1,2], J.-M. Son[1,2], S.-S. Lee[1], S. Lee[2], D.-H. Woo[2] and S.-H. Kim[2], *[1]Hanyang Univ. and [2]Korea Inst. of Science and Technology, Korea*

P6-12
Surface Plasmon Resonance and Emission Light Properties of Polystyrene Sphere Thin Films
K. Shinbo[1], S. Miyabayashi[1], K. Yoshizawa[1], H. Shirasawa[1], K. Kato[1] and F. Kaneko[1], *[1]Niigata Univ., Japan*

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Enhanced Frequency Response Associated with Negative Photoconductance in an InGaAs/InAlAs Avalanche Photodetector
G. Kim[1], I.G. Kim[1], J.H. Baek[1] and O.K. Kwon[1], *[1]Electronics & Telecommunication Research Inst., Korea*

P6-14
The Characteristic of InGaN/GaN Multiple-Quantum-Well Metal-Insulater-Semiconductor Photodiodes Using SiO_2 Fabricated by Photochemical Vapor Deposition
P.C. Chang[1], C.H. Chen[2], S.J. Chang[1], Y.K. Su[1], P.C. Chen[1], Y.D. Jhou[1], H. Hung[1], S.L. Wu[2], and K.C. Huang[2], *[1]National Cheng Kung Univ. and [2]Cheng Shiu Inst. of Technology, Taiwan*

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Novel Devices, Physics, and Fabrication
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Novel comb-type differential pressure sensor with silicon beams embedded in a silicone rubber membrane
C.T. Seo[1] and J.H. Lee[1],
[1]Kyungpook National Univ., Korea

P7-2
Periodic Coulomb oscillation in highly doped Si single-electron transistor
T. Kitade[1], K. Ohkura[1] and A. Nakajima[1], *[1]RCNS, Hiroshima Univ., Japan*

P7-3
Active Pixel Sensor Using an SOI MOSFET Photodetector with a Quantum Wire
J.-H. Park[1], S.-H. Seo[1], I.-S. Wang[1], J.-H. Kim[1], J.-K. Shin[1], P. Choi[1], Y.-C. Jo[2] and H. Kim[2], *[1]Kyungpook National Univ. and [2]Korea Electronics Technology Inst., Korea*

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Side Gating Phenomenon in GaAs Quantum Wire Transistors
R. Jia[1], S. Kasai[1] and H. Hasegawa[1], *[1]RCIQE, Hokkaido Univ., Japan*

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Observation of current modulation in SAM-FET fabricated by an air-bridge structure
K. Sasao[1], Y. Azuma[1], N. Kaneda[1], E. Hase[1], Y. Miyamoto[1] and Y. Majima[1], *[1]Tokyo Inst. of Technology, Japan*

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Generation of Local Magnetic Field by Nano Electro-Magnets
H.K. Kim[1,2], S.H. Hong[1], B.C. Kim[1], J.S. Hwang[2], S.W. Hwang[1,2] and D. Ahn[2], *[1]Korea Univ. and [2]Univ. of Seoul, Korea*

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Atomic-scale Smoothing and Structural Analysis of $LiNbO_3$ Surface
A. Saito[1,2], H. Matsumoto[1], S. Ohnisi[1], M. Akai-Kasaya[1], Y. Kuwahara[1,2] and M. Aono[1,3], *[1]Osaka Univ., [2]RIKEN and [3]National Inst. for Materials Science, Japan*

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Electron Transport in Molecular Enamel Wires
Rodion Belosludov[1], Amir Farajian[1], Hiroshi Mizuseki[1], Kyoko Ichinoseki[1] and Yoshiyuki Kawazoe[1], *[1]Tohoku University, Japan*

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P8-1
Spin depolarization via tunneling effects in asymmetric double quantum dot structure
H. Sasakura[1], S. Adachi[1], S. Muto[1], H. Song[2], T. Miyazawa[2] and T. Usuki[2], *[1]Hokkaido Univ. and CREST, JST and [2]Fujitsu Labs Ltd., Japan*

P8-2
Mechanical Properties of Nanometer-sized Cu Contacts
T. Kizuka[1], M. Mori[1], S. Fujisawa[2] and A. Yabe[2], *[1]Univ. of Tsukuba, [2]AIST, Japan*

P8-3
A Study on Doping Density in InAs/GaAs Quantum Dot Infrared Photodetector
U.H. Lee[1], Y.H. Kang[1], J.H. Oum[1], S.-J. Lee[2], M. Kim[2], S.K. Noh[2], Y.D. Jang[3], D. Lee[3] and S. Hong[1], *[1]Korea Advanced Inst. of Science and Technology, [2]Korea Research Inst. of Standards and Science and [3]Chungnam National Univ., Korea*

P8-4
Enhanced Optical Properties of High Density ($>10^{11}/cm^2$) InAs/AlAs Quantum Dots by Using Hydrogen Passivation
S.-K. Park[1], J. Tatebayashi[1], Y.J. Park[2] and Y. Arakawa[1], *[1]RCAST and IIS, Univ. of Tokyo, Japan and [2]Korea Inst. of Science and Technology, Korea*

P8-5
Controlling the optical properties of self-assembled InAs quantum dots by various annealing treatments
J.-J. Yoon[1], S.-I. Jung[1], H. Choi[1], J.W. Lee[1], G.S. Cho[1], M.H. Jeon[1], J.-Y. Leem[1], D.Y. Lee[2], J.S. Kim[3], J.S. Son[4], S.I. Ban[1], J.I. Lee[5] and J.S. Kim[6], *[1]InJe Univ., [2]Yeungnam Univ., [3]Nanomaterials Lab., [4]Kyungwoon Univ., [5]Materials Evaluation Center and [6]Basic Res. Lab., ETRI, Korea*

P8-6
Control of GaSb/GaAs Quantum Nanostructures by Molecular Beam Epitaxy
T. Nakai[1], S. Iwasaki[1] and K. Yamaguchi[1], *[1]The Univ. of Electro-Communications, Japan*

P8-7
Formation of Ge Quantum dots by Selective Oxidation of SiGe alloys for Single-Electron Devices
P.-W. Li[1], W.-M. Liao[1], S.W. Lin[1], P.S. Chen[1] and M.J. Tsai[1], *[1]National Central Univ. Taiwan*

P8-8
Investigation of Ultrafast Carrier Dynamics in Quantum Wire by Terahertz Spectroscopy
I. Morohashi[1,2], K. Komori[1,2], T. Hidaka[3], G.-R. Wang[1], M. Ogura[1] and M. Watanabe[1], *[1]National Inst. of Advanced Industrial Science and Technology, [2]CREST, JST and [3]Shonan Inst. of Technology, Japan*

P8-9
Influence of deep-level concentrations on strong red photoluminescence from nano-porous silicon formed on Fe-contaminated silicon substrate
D.-Y. Lee[1], J.-W. Park[1], S.-S. Choi[1], D.-H. Kim[1], I.-H. Bae[1], J.-Y. Leem[2], J.-S. Kim[3], S.-K. Kang[4], J.-S. Son[5] and I.-S. Kim[5], *[1]Yeungnam Univ., [2]Inje Univ., [3]National Inst. for Materials Science, [4]Kyunghee Univ. and [5]Kyungwoon Univ., Korea*

P8-10
Identification of valence-band ordering in ZnO by using four-wave mixing
S. Adachi[1], S. Muto[1], K. Hazu[2], T. Sota[2], K. Suzuki[2] and S. Chichibu[3], *[1]Hokkaido Univ., [2]Waseda Univ. and [3]Univ. of Tsukuba, Japan*

P9
Silicon-on-Insulator Technologies
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SOI SRAM / DRAM Cells for 0.5 Volt Operation
M. Terauchi[1], *[1]Hiroshima City Univ., Japan*

P9-2
Complete Surface-Potential-Based SOI-MOSFET Model for Circuit Simulation
D. Kitamaru[1], Y. Uetsuji[1] and M. Miura-Mattausch[1], *[1]Hiroshima Univ., Japan*

P9-3
Complementary Operation of Schottky Source/Drain SOI MOSFET with Shallow Doped Extension
S. Matsumoto[1], M. Nishisaka[1] and T. Asano[1], *[1]Kyushu Inst. of Technology, Japan*

P9-4
A Workable Use of Floating-Body SOS MOSFET as a Transconductance Mixer
S. Lam[1], A.C.-K. Chan[1], W.-K. Lee[1], P.K.T. Mok[1], P.K. Ko[1] and M. Chan[1], *[1]Hong Kong Univ. of Science & Technology, Hong Kong*

P9-5
Thereshold Voltage Control on the Body-Tied FinFET (OMEGA MOSFET)
H.J. Jo[1], T.-S. Park[2], J.D. Choe[1], S.Y. Han[1], J.H. Jeong[1], M.C. Chae[1], D.G. Park[1], K. Kim[1], E. Yoon[2] and J.-H. Lee[3], *[1]Samsung Electronics Co., Ltd, [2]Seoul National Univ. and [3]Kyungpook National Univ., Korea*

P9-6
High Performance Buried Gate Surrounding Gate Transistor (BG-SGT) for Future Three-Dimensional Devices
M. Iwai[1], Y. Yamamoto[1], R. Nishi[1], H. Sakuraba[1], T. Endoh[1] and F. Masuoka[1], *[1]RIEC, Tohoku Univ., Japan*

P9-7
Thermal conductivity of high-integrity nanometer buried oxides by SIMOX
Y. Dong[1], X. Wang[1], J. Chen[1], M. Chen[1,2], X. Wang[1,2], P. He[3], L. Tian[3] and Z. Li[3], *[1]Shanghai Inst. of Microsystem and Information Technology, Chinese Academy of Sciences, [2]Shanghai Simgui Technology Co., Ltd. and [3]Inst. of Microelectronics, Tsinghua Univ., China*

P9-8
Low frequency noise in partially-depleted SOI MOSFETs operating from linear region to saturation region at various temperatures
K.-M. Chen[1], H.-H. Hu[2], G.-W. Huang[1], S.-Y. Huang[2], A.S. Peng[1], W.-K. Yeh[3] and C.-Y. Chang[2], *[1]Natioanl Nano Device Labs, [2]Natioanl Chiao Tung Univ. and [3]National Univ. of Kaohsiung, Taiwan*

P10
Non-Volatile Memory Technologies
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P10-1
Improvement of Data Retention in Floating Gate Flash EEPROM's with P-Doped Floating Gate
B.C. Wu[1], H.W. Tsai[1], S.S. Chung[1], C.J. Lin[2], D.S. Kuo[3], and M.S. Liang[2], *[1]National Chiao Tung Univ., [2]Tsmc, Science-based Industrial Park, Hsinchu, Taiwan and [3]Nexflash Inc., San Jose, USA*

P10-2
New Three Dimensional High Density S-SGT Flash Memory Architecture using Self-Aligned Interconnection Fabricating Technology without Photo Lithography Process for Tera Bits and Beyond
H. Sakuraba[1], K. Kinoshita[2], T. Tanigami[2], T. Yokoyama[1], S. Horii[1], M. Saitoh[2], K. Sakiyama[2], T. Endoh[1] and F. Masuoka[1], *[1]RIEC, Tohoku Univ. and [2]Sharp Corporation, Japan*

P10-3
The Impact of Technology Parameters and Scaling on the Programming Performance and Drain Disturb in CHISEL Flash EEPROMs
D. Nair[1], N. Mohapatra[1], S. Mahapatra[1] and S. Shukuri[2], *[1]Indian Inst. of Technology, India and [2]Hitachi Ltd., Japan*

P10-4
Key technologies of First 'Chain' -32M bit Ferroelectric RAM
T. Ozaki[1], N. Nagel[2], Y. Kumura[1], J. Lian[2], A. Hilliger[2], T. Tsuchiya[1], R. Bruchhaus, H. Kanaya[1], H. Koyama, U. Wellhausen, O. Hidaka, S. Shuto, S. Germhardt, Y. Shimojo, B.K. Moon, H. Itokawa, U. Egger, H. Zhuang, K. Tomioka, M. Fukushima, K. Yamakawa, D. Takashima, I. Kunishima[1], Y. Oowaki[1] and G. Beitel[2], *[1]Smiconductor Company, Toshiba Corporation and [2]Infineon Technologies Japan K.K., Japan*

P10-5
High performance Pt/$SrBi_2$ Ta_2 O_9/Hfo_2/Si structure for 1T ferroelectric random access memory
D.-Y. Wang[1], C.-H. Chien[2], M.-J. Yang[2], P. Lehnen[3], C.-C. Leu[2], S.-H. Chuang[2], T.-Y. Huang[1] and C.Y. Chang[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs and [3]AIXTRON AG, Germany*

P10-6
Improvement in Read Endurance of Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode
D.K. Tran[1] and S. Horita[1], *[1]JAIST, Japan*

P10-7
A Novel Sensing Circuit for High Speed Synchronous MRAM
H. Kim[1], S. Lee[1], S. Lee[1], H. Shin[1] and D. Kim[2], *[1]Ewha Womans Univ. and [2]Kookmin Univ., Korea*

P10-8
Electrical Characterization Sub-micron MTJ Cells Using SPM
S. Park[1], J. Heo[1], I. Chung[1] and T. Kim[2], *[1]SungKyunKwan Univ. and [2]Samsung Advanced Inst. of Technology, Korea*

P10-9
Highly Anisotropic and Corrosion-less PtMn Etching using Negative Ions in Pulse-Time-Modulated Chlorine Plasma
S. Kumagai[1], T. Shiraiwa[2] and S. Samukawa[1], *[1]Tohoku Uinversity and [2]Micro Systems Network Company, Sony Corporation, Japan*

P11
SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
(4 Papers)

P11-1
Balanced-type Peak Power Injection Amplifierfor Simultaneous High Efficiency and Large Saturation Power
K. Iyomasa[1], M. Nakayama[1], K. Horiguchi[1], Y. Ikeda[1] and Y. Sakai[1], *[1]Mitsubishi Electric Corporation, Japan*

P11-2
Indium Content Dependence of Electron Velocity and Impact Ionization in InAlAs/InGaAs Metamorphic HEMTs
H. Ono[1], S. Taniguchi[1] and T. Suzuki[2], *[1]Sony Corporation and [2]AIST, Japan*

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Two-Step Electrode Self-Aligned Process of InP-based RTDs for Highly Integrated RTD/HEMT Circuits
T. Ohki[1], N. Okamoto[1], T. Takahashi[1], K. Makiyama[1], K. Imanishi[1] and N. Hara[1], *[1]Fujitsu Labs Ltd., Japan*

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