Tuesday, September 16

EMINENCE HALL

PL: Opening Session (9:30 - 12:30)
Chairpersons: S. Kawamura, AIST and M. Koyanagi, Tohoku Univ.

9:30 PL-0
Welcome Address and Award Presentation
M. Nakamura, Hitachi

9:45 PL-1 (Plenary)
Research and Development Strategy for Creation of Corporate Value
T. Ikoma, Hitotsubashi Univ., Japan

10:30 PL-2 (Plenary)
Role and Strategy of IMEC as a European Player in a Globalized Research Era
G.J. Declerck, IMEC, Belgium

11:15 PL-3 (Plenary)
Progress and Perspective of Nanostructure Devices for Ubiquitous Information Network
Y. Arakawa, Univ. of Tokyo, Japan

12:30-14:00 Lunch

Room A

A-1: Advanced Silicon Devices and Device Physics
-Gate Stack Technologies-(14:00-15:50)
Chairs: T. Mogami (NEC)
K. Shibahara (Hiroshima Univ.)

14:00 A-1-1 (Invited)
Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation
J. Kedzierski[1], E. Nowak[2], M. Ieong[2], T. Kanarski[2], and D. Boyd[2], *[1]SRDC, IBM, [2]Microelectronics Division, USA*

14:30 A-1-2
Influences of Gate-Poly Impurity Concentration on Inversion-Layer Mobility in MOSFETs with Ultrathin Gate Oxide Film
J. Koga[1], T. Ishihara[1] and S. Takagi[1], *[1]Toshiba Corp., Japan*

Room B

B-1: Non-Volatile Memory Technologies
-Non-Volatile Memory I-(14:00-16:00)
Chairs: T. Nakamura (Rohm)
Y. Shimada (Matsushita Electric)

14:00 B-1-1 (Invited)
Current FeRAM Technology Developments and Scaling towards 3-D Capacitor Cells
D.J. Wouters[1], *[1]IMEC, Belgium*

14:30 B-1-2 (Invited)
32Mb Chain FeRAM -An Overview
D. Takashima[1] and T. Rohr[2], *[1]Toshiba Corp., and [2]Infineon Technologies Japan K.K., Japan*

Room C

C-1: Silicon Process / Materials Technologies
-High-k Gate Dielectric I-(14:00-15:50)
Chais: Y. Tsunashima (Toshiba)
H. Kitajima (Selete)

14:00 C-1-1 (Invited)
Mobility in high-κdielectric based field effect transistors
L-A Ragnarsson[1], W. Tsai[2], A. Kerber[3], P.J. Chen[4], E. Cartier[5], L. Pantisano[1], S. De Gendt[1], and M. Heyns[1], *[1]IMEC, Belgium, [2]Intel Corp., [3]Infineon, [4]Texas Instruments, USA, and [5]IBM*

14:30 C-1-2
Effect of the Film Composition of HfAlON Gate Dielectric on the Structural Transformation and the Electrical Properties through High-temperature Annealing
M. Koyama[1], Y. Kamimuta[1], M. Koike[1], M. Suzuki[1] and A. Nishiyama[1], *[1]Toshiba Corp., Japan*

Room D

D-1: New Materials and Characterization
-Oxide Reliability and Surface Characterization-(14:00-16:00)
Chairs: H. Satake (Toshiba)
T. Maruizumi (Hitachi)

14:00 D-1-1
The Effect of Boron and Fluorine Incorporation in SiON Gate Insulator on NBTI
T. Sasaki[1], F. Ootsuka[1], H. Ozaki[1], M. Tomikawa[1], M. Yasuhira[1] and T. Arikado[1], *[1]SELETE, Japan*

14:20 D-1-2
New insights into dynamic negative bias temperature instabilities of pMOSFETs
S.S. Tan[1], T.P. Chen[1], C.H. Ang[2], W.Y. Teo[2] and L. Chan[2], *[1]Nanyang Technological Univ. of Singapore and [2]Chartered Semiconductor Manu. Ltd., Singapore*

Room E

E-1:Quantum Nanostructure Devices and Physics
-Fabrication and Micromechanics-(14:00-16:00)
Chairs: Y. Hirayama (NTT)
J. Motohisa (Hokkaido Univ.)

14:00 E-1-1 (Invited)
Electronic and photonic devices via one-dimensional stacking of quantum structures
L. Samuelson[1], *[1]Lund Univ., Solid State Physics/the Nanometer Consortium*

14:30 E-1-2
Formation of 1μm-period GaAs Kagome Lattice Structure by Selective Area Metalorganic Vapor Phase Epitaxy
P. Mohan[1], J. Motohisa[1] and T. Fukui[1], *[1]Hokkaido Univ., Japan*

Room F

F-1:Compound Semiconductor Materials and Devices
-III-V and Nitride Electron Devices-(14:00-16:00)
Chairs: T. Mizutani (Nagoya Univ.)
M. Kuzuhara (FED)

14:00 F-1-1 (Invited)
Ultrahigh Performance InP HEMTs
A. Endoh[1], Y. Yamashita[1], K. Shinohara[2], K. Hikosaka[1], T. Matsui[2], S. Hiyamizu[2], and T. Mimura[1], *[1]Fujitsu Labs Ltd., [2]Osaka Univ., Japan*

14:30 F-1-2
High f_T 30nm $In_{0.7}GaAs$ HEMT fabricated with SiO_2/SiN_x sidewall Process and BCB Planarization
D.-H. Kim[1], S.-J. Yeon[1], S.-S. Song[1] and K.-S. Seo[1], *[1]Seoul National Univ., Korea*

Room G

G-1:Advanced Silicon Circuits and Systems
-Advanced CMOS Circuits and Systems-(14:00-15:50)
Chairs: T. Kuroda (Keio Univ.)
M. Fujishima (Univ. of Tokyo)

14:00 G-1-1 (Invited)
Silicon Integration of UWB: Choices and Challenges
S.G. Narendra
[1]Circuit Research - Intel Labs, USA

14:30 G-1-2
Low-Power Real-Time Region-Growing Image-Segmentation in 0.35μm CMOS due to BAO-Scheme and Subdivided-Image Approach
T. Morimoto[1], Y. Harada[1], T. Koide[1] and H.J. Mattausch[1], *[1]Hiroshima Univ., Japan*

Room A

14:50 A-1-3
New Self-aligned Metal-gate MOSFETs Using Aluminum Substitution Technology
S. Nakamura[1], H. Shido[1], T. Kurahashi[1], S. Kishii[1], T. Nagata[1], B. Kumasaka[1], T. Usuki[1], S. Sato[1] and Y. Mishima[1], *[1]Fujitsu Labs Ltd., Japan*

15:10 A-1-4
Screening Effect on Remote Coulomb Scattering due to impurities in Polysilicon Gate of MOSFET
T. Ishihara[1], J. Koga[1], S. Takagi[1] and K. Matsuzawa[1], *[1]Toshiba Corporation, Japan*

15:30 A-1-5
Direct evaluation of an interfacial layer in high-*k* gate dielectrics by 1/f noise measurements
T. Ishikawa[1], S. Tsujikawa[1], S. Saito[1], D. Hisamoto[1] and S. Kimura[1], *[1]Hitachi, Ltd., Japan*

Room B

15:00 B-1-3
A proposal of new ferroelectric gate field effect transistor memory based on ferroelectric-insulator interface conduction
G. Hirooka[1], M. Noda[1] and M. Okuyama[1], *[1]Osaka Univ., Japan*

15:20 B-1-4
Long-Term Stabilization of Sense Signals in a Non-Destructive Readout FeRAM by Intentional Modification of the Polarization Hysteresis Curve for Low Voltage Applications
T. Yamada[1], Y. Kato[1], S. Koyama[1] and Y. Shimada[1], *[1]Matsushita Electric Industrial Co., Ltd., Japan*

15:40 B-1-5
A Low Dielectric Constant $Sr_2(Ta_{1-x},Nb_x)_2O_7$ Thin Film Controlling the Crystal Orientaion on IrO_2 Substrate for One Transistor Type Ferroelectric Memory Device
I. Takahashi[1], H. Sakurai[1], A. Yamada[2], T. Goto[1], M. Hirayama[1], A. Teramoto[1], S. Sugawa[1] and T. Ohmi[1], *[1]NICHe, Tohoku Univ. and [2]Tohoku Univ., Japan*

Room C

14:50 C-1-3
Projection of Mobility Degradation in $HfAlO_xSiO_2$ nMOSFET towards the Reduction of Interfacial Oxide Thickness
N. Yasuda[1], H. Hisamatsu[1], H. Ota[2], K. Iwamoto[1], K. Tominaga[1], K. Yamamoto[1], W. Mizubayashi[2], N. Yamagishi[1], M. Ohno[1], S. Migita[2], Y. Morita[2], T. Horikawa[2], T. Nabatame[1] and T. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]The Univ. of Tokyo, Japan*

15:10 C-1-4
Ultra-thin (EOT<1.0nm) Amorphous HfSiON Gate Insulator with High Hf Concentration for High-performance Logic Applications
M. Koike[1], T. Ino[1], M. Koyama[1], Y. Kamata[1], Y. Kamimuta[1], M. Suzuki[1], A. Takashima[1], Y. Mitani[1], A. Nishiyama[1] and Y. Tsunashima[1], *[1]Toshiba Corporation, Japan*

15:30 C-1-5
Hafnium Content Dependence of Bottom Interfacial Layer and Its Impact on $Hf_xAl_{1-x}O_y$ High-k nMOSCAPs and nMOSFETs Characteristics
Y. Tamura[1], Y. Sugiyama[1], M. Yamaguchi[1], H. Minakata[1], Y. Tanida[1], T. Sakoda[1], M. Nakamura[1] and Y. Nara[1], *[1]Fujitsu Labs Ltd., Japan*

Break

Room D

14:40 D-1-3
Neighboring effect in nitrogen-enhanced negative bias temperature instability
S.S. Tan[1], T.P. Chen[1], J.M. Soon[2], K.P. Loh[2], C.H. Ang[3], W.Y. Teo[3] and L. Chan[3], *[1]Nanyang Technological Univ. of Singapore, [2]National Univ. of Singapore and [3]Chartered Semiconductor Manu. Ltd., Singapore*

15:00 D-1-4
Conductive Atomic Force Microscopy Analysis for Local Electric Characteristic in Stressed SiO_2 Gate Films
Y. Watanabe[1], A. Seko[2], H. Kondo[2], A. Sakai[2], S. Zaima[2] and Y. Yasuda[2], *[1]Toyota Central R&D Labs., Inc., [2]Nagoya Univ., Japan*

15:20 D-1-5
Measurement of extension structures in deep sub-micron MOSFETs by scanning capacitance microscopy based on frequency modulation control
Y. Naitou[1] and N. Ookubo[1], *[1]Silicon Systems Research Labs, NEC Corporation, Japan*

15:40 D-1-6
Valence-Mended Si(100) for Nanoelectronic Applications
M. Tao[1], W. P. Kirk[1], D. Udeshi[1], S. Agarwal[1], E. Maldonado[1] and N. Basit[1], *[1]Univ. of Texas at Arlington, USA*

Room E

14:45 E-1-3
Selective MBE Growth of GaAs Hexagonal Nano-wire Networks on (111)B Patterned Substrates
S. Yoshida[1], I. Tamai[1], T. Sato[1] and H. Hasegawa[1], *[1]Hokkaido Univ., Japan*

15:00 E-1-4
Migration-induced Ge Dot Formation
S. Kaechi[1], D. Kitayama[1] and Y. Suda[1], *[1]Tokyo Univ. of Agriculture & Technology, Japan*

15:15 E-1-5
Demonstration of MEMS-Controlled Electronic States in Single Quantum Dots
T. Nakaoka[1], T. Kakitsuka[2], T. Saito[1] and Y. Arakawa[1,2], *[1]RCAST, IIS, and CCR, Univ. of Tokyo and [2]NTT Photonics Labs, NTT Corporation, Japan*

15:30 E-1-6
Displacement Sensing using Quantum Mechanical Interference
H. Yamaguchi[1], S. Miyashita[2] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs, [2]NTT Advanced Technology and [3]CREST-JST, Japan*

15:45 E-1-7
ZnO Metal-Insulator-Semiconductor Field-Effect-Transistor
J. Nishii[2], A. Ohtomo[1], T. Fukumura[1], K. Ohtani[2], F. Matsukura[2], Y. Ohno[2], H. Ohno[2] and M. Kawasaki[1], *[1]Tohoku Univ. and [2]RIEC, Tohoku Univ., Japan*

Room F

14:45 F-1-3
Observation of Thermal Reliability of BCB Passivated InAlAs/InGaAs HEMTs
M. Yoon[1], T. Kim[1], D. Kim[1] and K. Yang[1], *[1]KAIST, Korea*

15:00 F-1-4
High f_{max} 0.1 μm Γ-gate InGaAs/InAlAs/GaAs Metamorphic HEMT
B.H. Lee[1], B.O. Lim[1], M.R. Kim[1], S.D. Kim[1], J.K. Rhee[1] and H.S. Yoon[2], *[1]MINT and [2]Electronics and Telecommunications Research Inst., Korea*

15:15 F-1-5
Reduction of Turn-on Voltage in GaInNAs and InGaAs Base Double Heterojunction Bipolar Transistors
C.-H. Wu[1], Y.-K. Su[1], S.-C. Wei[1] and S.-J. Chang[1], *[1]National Cheng Kung Univ., Taiwan*

15:30 F-1-6
InP/InGaAs Tunneling Emitter Bipolar Transistor (TEBT)
C.-Y. Chen[1], H.-M. Chuang[1], S.-I. Fu[1], P.-H. Lai[1], Y.-Y. Tsai[1], C.-I. Kao[1] and W.-C. Liu[1], *[1]National Cheng-Kung Univ., Taiwan*

15:45 F-1-7
High-Quality Two-Dimensional Electron Gas at Large Scale GaN/AlGaN Wafer Interface Prepared by Mass Production MOCVD Systems
S. Yamada[1], T. Ohnishi[1], T. Kakegawa[1], M. Akabiri[1], T. Suzuki[1], H. Sugiura[2], F. Nakamura[2], E.Yamaguchi[2] and H. Kawai[2], *[1]CNMT, JAIST and [2]Powdec K.K., Japan*

Room G

14:50 G-1-3
Butterfly-Unit Based Programmable Computation Element Using Merged Module of Multiplication, Division and Square Root
L. Karnan[1], N. Miyamoto[1], K. Maruo[1], K. Kotani[1] and T. Ohmi[2], *[1]Tohoku Univ. and [2]NICHe, Tohoku Univ., Japan*

15:10 G-1-4
A Hierarchical 512-Kbit SRAM with 8 ports in 130nm CMOS
S. Fukae[1], N. Omori[1], T. Koide[1], H. J. Mattausch[1] and T. Hironaka[2], *[1]RCNS, Hiroshima Univ. and [2]Hiroshima City Univ., Japan*

15:30 G-1-5
Combined Data/Instruction Cache with Bank-Based Multi-Port Architecture
K. Johguchi[1], Z. Zhu[1], T. Hirakawa[2], T. Koide[1], T. Hironaka[2] and H.J. Mattausch[1], *[1]Hiroshima Univ. RCNS and [2]Hiroshima City Univ., Japan*

Break

Room A

A-2: Advanced Silicon Devices and Device Physics
-Advanced CMOS Technology I-(16:15-18:15)
Chairs: A. Hiroki
(Kyoto Inst. of Technol.)
S. Inaba
(Toshiba)

16:15 A-2-1
Enhancement of V_{th} Degradation under NBT Stress due to Hole Capturing
Y. Mitani[1], M. Nagamine[1], H. Satake[1] and A. Toriumi[2], *[1]Toshiba Corporation and [2]The Univ. of Tokyo, Japan*

16:35 A-2-2
New Mechanism for Negative-Bias-Temperature Instability and Its Impact on Scaling of pMOSFETs
D.-Y. Lee[1], H.-C. Lin[2], C.-C. Chen[3], C.-H. Chien[2], T.-Y. Huang[1], T. Wang[1], T.-L. Lee[3], S.-C. Chen[3] and M.-S. Liang[3], *[1]National Chiao-Tung Univ., [2]National Nano Device Labs and [3]Taiwan Semiconductor Manufacturing Company, Taiwan*

16:55 A-2-3
Origin of Enhanced Thermal Noise for 100nm-MOSFETs
S. Hosokawa[1], Y. Shiraga[1], H. Ueno[1], M. Miura-Mattausch[1], H. J. Mattausch[1], T. Ohguro[2], S. Kumashiro[2], M. Taguchi[2], H. Masuda[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]STARC, Japan*

17:15 A-2-4
Comparison of the Interconnect Capacitances for Various SRAM Cell Lyaouts To Achieve High Speed, Low Power SRAM Cells
Y. Tsukamoto[1], K. Nii[1], Y. Yamagami[2], T. Yoshizawa[1], S. Imaoka[3], T. Suzuki[2], A. Shibayama[2] and H. Makino[1], *[1]Renesas Technology Corporation, [2]Matsushita Electric Industrial Corporation and [3]Renesas Device Design Corporation, Japan*

Room B

B-2: Non-Volatile Memory Technologies
-Non-Volatile Memory II-(16:15-17:35)
Chairs: Y. Shimada
(Matsushita Electric)
T. Nakamura
(Rohm)

16:15 B-2-1
Novel Capacitor Structure Using Sidewall Spacer for Highly Reliable FRAM Device
H.H. Kim[1], J.H. Park[1], Y.J. Song[1], N.W. Jang[1], H.J. Joo[1], S.K. Kang[1], S.H. Joo[1], S.Y. Lee[1] and K. Kim[1], *[1]Samsung Electronics Co. Ltd., Korea*

16:35 B-2-2
High perfomance PZT capacitor using highly crystalline SRO bottom electrode for Mbit FeRAM devices
H. Itokawa[1], K. Natori[1], S. Yamazaki[1], G. Beitel[2] and K. Yamakawa[1], *[1]Toshiba Corp. and [2]Infineon Technologies Japan., Japan*

16:55 B-2-3
A novel chemical solution deposition method suitable for high-yield fabrication of 50 nm-thick $SrBi_2Ta_2O_9$ capacitors
Y. Kawashima[1] and H. Ishiwara[1], *[1]Tokyo Inst. of Technology, Japan*

17:15 B-2-4
Two-Mode Behavior in Time and Temperature Dependence of Imprint-Induced Charge Loss in Integrated $SrBi_2(Ta,Nb)_2O_9$ Capacitors
A. Noma[1], T. Mikawa[1], Y. Nagano[1], Y. Judai[1] and E. Fujii[1], *[1]Matsushita Electric Industrial Co., Ltd., Japan*

Room C

C-2: Silicon Process / Materials Technologies
-High-k Gate Dielectric II-(16:15-17:55)
Chairs: M. Kubota
(Matsushita Electric)
J. Yugami
(Renesas)

16:15 C-2-1
Flatband Voltage Shift Caused by Dopants Diffused from Poly-Si Gate Electrode in Poly-Si/HfSiO/SiO_2/Si
A. Kaneko[1], S. Inumiya[1], K. Sekine[1], M. Sato[1], Y. Kamimuta[1], K. Eguchi[1] and Y. Tsunashima[1], *[1]Toshiba Corporation, Japan*

16:35 C-2-2
Controlled Nitrogen Incorporation into $HfAlO_x$ by Layer-by-Layer Deposition and Annealing (LL-D&A) Process and Its Impact on Electrical Properties of MOSCAPs and nMOSFETs
K. Tominaga[1], K. Iwamoto[1], H. Hisamatsu[1], T. Yasuda[2], H. Ota[2], N. Yasuda[1], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC, AIST and [3]the Univ. of Tokyo, Japan*

16:55 C-2-3
Suppression of Silicidation in Poly-Si/ZrO_2/SiO_2/Si Structure by Helium Through Process
K. Muraoka[1], *[1]Advanced LSI Technology Lab, Toshiba Corporation, Japan*

17:15 C-2-4
Reliability characteristics of an HfO_2/SiO_2 stack gate dielectric annealed in a deuterium ambient
H. Park[1], H. Yang[1], H. Sim[1] and H. Hwang[1], *[1]Kwangju Inst. of Science and Technology, Korea*

Room D

D-2: New Materials and Characterization
-Low k and Silicide Characterization-(16:15-18:15)
Chairs: K. Kikuta
(NEC)
S. Zaima
(Nagoya Univ.)

16:15 D-2-1
Nondestructive Characterization of Pore Size Distributions in Porous Low-k Films by in-situ Spectroscopic Ellipsometry in Vapor Cell
C. Negoro[1], N. Hata[1,2] and T. Kikkawa[2,3], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST and [3]RCNS, Hiroshima Univ., Japan*

16:35 D-2-2
Accurate measurement of mechanical properties of nanoporous silica ultra-low-k films
Y. Seino[1], R. Ichikawa[2], H. Tanaka[3] and T. Kikkawa[4], *[1]MIRAI Project, ASRC, AIST, [2]ASRC, AIST, [3]MIRAI Project, ASET and [4]RCNS, Hiroshima Univ., Japan*

16:55 D-2-3
Mechanical Property and Skeletal Silicate Structure of Periodic Porous Silica Films
S. Takada[1], N. Hata[1,2], Y. Seino[1,2], K. Yamada[3], Y. Oku[3] and T. Kikkawa[2,4], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*

17:15 D-2-4
Determination of the Mechanical Properties of Thin Periodic Porous Silica Films by Laser-Generated Surface Acoustic Wave Technique
X. Xiao[1], N. Hata[2,1], K. Yamada[3], H. Tanaka[3] and T. Kikkawa[4,2], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*

Room E

E-2:Quantum Nanostructure Devices and Physics
-Nanostructured Optical Devices-(16:15-18:00)
Chairs: K. Hirakawa
(Univ. of Tokyo)
L. Samuelson
(Lund Univ.)

16:15 E-2-1 (Invited)
A Light Emitting Diode for Single Photons
A.J. Shields[1], Z. Yuan[1], M.B. Ward[1], R.M. Stevenson[1], B.E. Kardynal[1], P. See[1], C. Lobo[2], P. Atkinson[2] and D.A. Ritchie[2], *[1]Toshiba Research Europe Ltd., Cambridge Research Lab and [2]Cavendish Lab., Univ. of Cambridge, UK*

16:45 E-2-2
Coherent control of exiton in a single quantum dot using a high-resolution Michelson interferometer
T. Okada[1,2,3], K. Komori[2,3], K. Goshima[2,3], S. Yamauchi[2,3], T. Sugaya[2,3], O. Yamazaki[4] and T. Hattori[4], *[1]Tokai Univesity Junior College, [2]AIST, [3]CREST-JST, Japan and [4]Univ. of Tsukuba, Japan*

17:00 E-2-3
Voltage-controlled Emission Wavelength Switching in a Pseudomorphic $Si_{1-x}Ge_x$/Si Double Quantum Well
N. Yasuhara[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo and [2]PRESTO-JST, Japan*

17:15 E-2-4
A Solid-State Multicolor Light-Emitting Device Based on Ballistic Electron Excitations
Y. Nakajima[1], T. Uchida[1], A. Kojima[1], B. Gelloz[1] and N. Koshida[1], *[1]Tokyo Univ. of Agri. & Tech., Japan*

Room F

F-2:Compound Semiconductor Materials and Devices
-Nitride Electron Devices-(16:15-18:00)
Chairs: T. Kikkawa
(Fujitsu Labs.)
N. Maeda
(NTT)

16:15 F-2-1 (Invited)
MOVPE Growth of Wurtzite InN and its Characteristics
T. Matsuoka[1], H. Okamoto[2], M. Nakao[2], H. Harima[3], H. Takahata[4], H. Mitate[4], S. Mizuno[4], Y. Uchiyama[5], T. Makimoto[1], *[1]NTT Basic Research Labs, [2]NTT Photonics Labs, [3]Kyoto Inst. of Technology, [4]NTT Advanced Technology and [5]Meiji Univ., Japan*

16:45 F-2-2
Extrinsic Base Regrowth of p-InGaN for Npn-type GaN/InGaN Heterojunction Bipolar Transistor
T. Makimoto[1], K. Kumakura[1] and N. Kobayashi[2], *[1]NTT Basic Research Labs, NTT Corporation and [2]The Univ. of Electro-Communications, Japan*

17:00 F-2-3
Improvement of DC and RF characteristics of AlGaN/GaN HEMTs by thermally annealed Ni/Pt/Au Schottky gate
T. Nanjo[1], N. Miura[1], T. Oishi[1], M. Suita[1], Y. Abe[1], T. Ozeki[1], S. Nakatsuka[1], A. Inoue[1], T. Ishikawa[1] and Y. Matsuda[1], H. Ishikawa[2] and T. Egawa[2], *[1]Mitsubishi Electric Corporation and [2]Nagoya Inst. of Technology, Japan*

17:15 F-2-4
The improvement of DC performance in AlGaN/GaN HFET with isoelectronic Al doped channel
C.M. Jeon[1], J.-H. Lee[2], J.-H. Lee[2] and J.-L. Lee[1], *[1]POSTECH, and [2]Kyungpook National Univ., Korea*

Room G

G-2:Advanced Silicon Circuits and Systems
-Collaboration of Circuits and Devices-(16:15-17:45)
Chairs: M. Fujishima
(Univ. of Tokyo)
T. Kuroda
(Keio Univ.)

16:15 G-2-1 (Invited)
Performance of Deeply-Scaled, Power-Constrained Circuits
B. Nikolic[1], L. Chang[1], T.-J. King[1], *[1]Univ. of California, USA*

16:45 G-2-2
ESD Circuit Simulation Technology Using Protection Device Model with Generated-Hole-Dependent Base Resistance
Y. Tosaka[1], H. Anzai[1], K. Suzuki[1] and H. Oka[1], *[1]Fujitsu Labs Ltd., Japan*

17:05 G-2-3
A New Protection Circuit of IGBT (Insulated Gate Bipolar Transistor) for Short-Circuit Withstanding Capability
B.-C. Jeon[1], I.-H. Ji[1], M.-K. Han[1] and Y.-I. Choi[2], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

17:25 G-2-4
Dynamic Holding Voltage SCR (DHVSCR) Device for ESD Protection with high Latch-up Immunity
Z.-P. Chen[1] and M.-D. Ker[2], *[1]Industrial Technology Research Inst., Hsinchu, and [2]Inst. of Electronics, National Chiao-Tung Univ., Taiwan*

Room A	Room B	Room C
17:35 A-2-5 Eliminating Threshold Voltage Offset of PMOSFETs in High-Density DRAM N. Takaura[1], R. Takemura[1], H. Matsuoka[1], R. Nagai[2], S. Yamada[2], H. Asakura[1] and S. Kimura[1], *[1]Hitachi, Ltd. and [2]Elpida Memory Inc., Japan*		**17:35 C-2-5** Enhancement of dielectric constant due to expansion of lattice spacing in CeO_2 directly grown on Si (111) D. Matsushita[1], Y. Nishikawa[1], N. Satou[2], M. Yoshiki[2], T. Shimizu[1], T. Yamaguchi[1], H. Satake[1] and N. Fukushima[1], *[1]Toshiba Corporation and [2]Toshiba Nanoanalysis Corporation, Japan*
17:55 A-2-6 Gate Engineering to prevent NMOS Dopant Channeling for Nano-Scale CMOSFET Technology S.-H. Park[1] and H.-D. Lee[2], *[1]Hynix Semiconductor Inc. and [2]Chugiak National Univ., Korea*		

18:30-20:30 Banquet (Eminence Hall)

Room D	Room E	Room F	Room G
17:35 D-2-5 HRTEM and EELS Analyses of Interfacial Nanostructures in Ti/$Si_{1-x}Ge_x$/Si(100) J. Yamasaki[1], N. Tanaka[1], O. Nakatsuka[1], A. Sakai[2], S. Zaima[3] and Y. Yasuda[2], *[1]CIRSE, Nagoya Univ., [2]Nagoya Univ. and [3]CCRAST, Nagoya Univ., Japan*	**17:30 E-2-5** High Brightness Si-based Quantum Dot Light Emitting Diode M. Jo[1], N. Yasuhara[1], K. Kawamoto[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo and [2]PRESTO, JST, Japan*	**17:30 F-2-5** Drain Current DLTS of AlGaN/GaN MIS-HEMTs T. Okino[1], M. Ochiai[1], Y. Ohno[1], S. Kisimoto[1], K. Maezawa[1] and T. Mizutani[1], *[1]Nagoya Univ., Japan*	
17:55 D-2-6 Impact of NiSi Thermal Instability on Junction Shallowing Characterized with Damage-free n+/p Silicon Diodes M. Tsuchiaki[1], K. Ohuchi[1] and C. Hongo[1], *[1]Toshiba Corporation, Japan*	**17:45 E-2-6** Generation of Radiation Pressure in Thermally Induced Ultrasonic Emitter Based on Nanocrystalline Silicon J. Hirota[1], H. Shinoda[2] and N. Koshida[1], *[1]Tokyo Univ. of A & T and [2]Univ. of Tokyo, Japan*	**17:45 F-2-6** Low damage, high selectivity $Ar/Cl_2/CH_4/O_2$ gate recess etching for AlGaN/GaN HEMT fabrication W.-K. Wang[1], Y.-J. Li[1], C.-K. Lin[1], Y.-J. Chan[1], G.-T. Chen[1] and J.-I. Chyi[1], *[1]National Central Univ., Taiwan*	

18:30-20:30 Banquet (Eminence Hall)