Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[A-7] Advanced CMOS: Device Technology

Thu. Sep 9, 2021 9:00 AM - 10:12 AM Room A: Area1

Session Chair:Anabela Veloso(IMEC), Kenichi Goto(TSMC)

9:00 AM - 9:30 AM

[A-7-01 (Invited)] Enablement of Next Generation Nanosheet Technology

○Nicolas Loubet[1], Curtis Durfee [1], Julien Frougier[1], Shogo Mochizuki[1], Maruf Bhuiyan [1], Ruqiang Bao [1], Andrew Greene[1], Eric Miller[1], Indira Seshadri[1] (1.IBM Research)

9:30 AM - 9:37 AM

[A-7-02] High Density & High Drive Current Elongated SGT Transistor for Logic Circuit Having Process Compatibility with 1.5nm node SGT SRAM

○Kenichi Kanazawa[1], Yisuo Li[3], Tetsuo Izawa[1], Koji Sakui[1], Georg Strof[2], Oskar Baumgartner[2], Gerhard Rzepa[2], Markus Karner[2], Zlatan Stanojevic[2], Nozomu Harada[1] (1.Semicon Consulting Ltd., 2.Global TCAD Solutions Ltd., 3.Unisantis Electronics Singapore Pre Ltd.)

9:37 AM - 9:44 AM

[A-7-03] The Impact of Self-Heating Effect on Noise Margin and Propagation Delay of Complementary FET Inverter

○Songhan Zhao[1], Wangyong Chen[1], Linlin Cai[1], Gang Du[1] (1.Institute of Microelectronics Peking University)

9:44 AM - 9:51 AM

[A-7-04] Width Dependence of Drain Current Variability Components in Extremely Narrow GAA Silicon Nanowire MOSFETs down to 2nm Width

○Zihao Liu[1], Tomoko Mizutani[1], Takuya Saraya[1], Masaharu Kobayashi[1], Toshiro Hiramoto[1] (1.Inst. of Indus. Sci., The Univ. of Tokyo)

9:51 AM - 9:58 AM

[A-7-05] Improvement of performance of $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs by ultrathin Y_2O_3 gate stacks with TMA treatment

○Tsung-En Lee[1], Shao-Tse Huang[2], Chiung-Yi Yang[2], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Yao-Jen Lee[2], Shinichi Takagi[1]
(1.Univ. of Tokyo, 2.Taiwan Semiconductor Res. Inst.)

9:58 AM - 10:05 AM

[A-7-06] Attainment of Low D_{it} and Reliable High-Ge-Content $Si_{1-x}Ge_x$ Gate Stacks via Low-Temperature Grown Ultra-Thin Epitaxial Si

○HsienWen Wan[1], Yi-Ting Cheng[1], Chao-Kai Cheng[1], Yu-Jie Hong[1], Tien-Yu Chu[1], Chien-Ting Wu[2], Jueinai Kwo[3], Minghwei Hong[1]
(1.National Taiwan Univ., 2.Taiwan Semiconductor Res. Inst., 3.National Tsing Hua Univ.)

10:05 AM - 10:12 AM

[A-7-07] Low-Temperature Fabrication of Ge MOS Capacitor with Wet Oxidized Yttrium Interlayer

○Keisuke Yamamoto[1], Kento Iseri[1], Dong Wang[1], Hiroshi Nakashima[1] (1.Kyushu Univ.)

2021 International Conference on
ssdm Solid State Devices and Materials
2021 September 6-9, 2021

Session information

Oral Presentation

Joint Session (Area1&10)

[A-8] IGZO for Integrated Devices

Thu. Sep 9, 2021 10:45 AM - 11:13 AM Room A: Area1

Session Chair:Hidetoshi Oishi(Sony Semiconductor Solutions Corp.), Mamoru Furuta(Kochi Univ. of Tech.)

10:45 AM - 10:52 AM

[A-8-01] Computing-in-Memory Demonstration of Multiple-State (>8) Analog Memory Cell with Ultra-Low (<1 nA/cell) Current Enabled by Monolithic CAAC-IGZO FET + Si CMOS FET Stack for Highly-Efficient AI Applications

○Satoru Ohshita[1], Hidefumi Rikimaru[1], Kazuki Tsuda[1], Hiromichi Godo[1], Yoshiyuki Kurokawa[1], Yoshinori Ando[1], Hiromi Sawai[1], Yasumasa Yamane[1], Shunpei Yamazaki[1], Toru Nakura[2], Hiroshi Yoshida[3], Kuo-Chang Huang[3], Miller Liao[4], Shou-Zen Chang[3]
(1.Semiconductor Energy Laboratory Co., Ltd., 2.Fukuoka Univ., 3.Powerchip Semiconductor Manufacturing Corp., 4.National Taiwan Univ.)

10:52 AM - 10:59 AM

[A-8-02] High-Performance Amorphous InGaZnO FET as a Key Enabler for Low Thermal Budget (350^{O}C) BEOL Monolithic 3-D Integration

○CHUNKUEI CHEN[1], Umesh Chand[1], Xinghua Wang[1], Zihang Fang[1], Sonu Hooda[1], Shih-Hao Tsai[1], Aaron Voon Yew Thean[1] (1.National Univ. of Singapore)

10:59 AM - 11:06 AM

[A-8-03] Statistical Analysis on Threshold Voltage Variability of CAAC-IGZO FETs Using Large-Scale Array TEG

Yuki - Ito[1], ○Toshiki - Hamada[1], Yoshinori - Ando[1], Masahiro - Takahashi[1], Tsutomu - Murakawa[1], Hitoshi - Kunitake[1], Masaharu - Kobayashi[2], Kuo Chang Huang[3], Hiroshi - Yoshida[3], Miller - Liao[4], Shou Zen Chang[3], Shunpei - Yamazaki[1]
(1.Semiconductor Energy Laboratory Co., Ltd., 2.d.lab, School of Engineering, the University of Tokyo, 3.Powerchip Semiconductor Manufacturing Corporation, 4.National Taiwan University)

11:06 AM - 11:13 AM

[A-8-04] Simulation Study on Memory Characteristics of IGZO-Channel FeFET from 2D Planer to 3D Vertical Structure for Channel Structure Engineering

Fei Mo[1], Xiaoran Mei[1], Takuya Saraya[1], Toshiro Hiramoto[1], ○Masaharu Kobayashi[1] (1.Univ. of Tokyo)

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[D-7] GaN Power Devices and Process Technologies

Thu. Sep 9, 2021 9:00 AM - 10:19 AM Room D: Area 4

Session Chair:Toru Sugiyama(Toshiba Electronic Device & Storage Corp.), Manabu Yanagihara(ROHM Co., Ltd.)

9:00 AM - 9:30 AM

[D-7-01 (Invited)] GaN-on-Si Power Device Platform: Epitaxy, Device, Reliability and Application

○Roy King-Yuen Wong[1] (1.Innoscience Tech.)

9:30 AM - 9:37 AM

[D-7-02] A Novel ± 1.2 kV Bidirectional Blocking Si-GaN Monolithic Integrated Cascode FET

○Guofang Yang[1], Jiaqi Zhang[1], Dazheng Chen[1], Jincheng Zhang[1], Chunfu Zhang[1], Yue Hao[1] (1.Xidian University, School of Microelectronics)

9:37 AM - 9:44 AM

[D-7-03] Two-step mesa p-GaN gated anode diode for low-power rectification applications

○Yuwei Zhang[1], Naotaka Iwata[1] (1.Toyota Tech. Inst.)

9:44 AM - 9:51 AM

[D-7-04] Fixed Charge Generation in SiO_2/GaN MOS Structures by Forming Gas Annealing and its Suppression by Controlling Ga-oxide Interlayer Growth

○Hidetoshi Mizobata[1], Mikito Nozaki[1], Takuma Kobayashi[1], Takuji Hosoi[1], Takayoshi Shimura[1], Heiji Watanabe[1] (1.Osaka Univ.)

9:51 AM - 9:58 AM

[D-7-05] Comparative study of breakdown and interface properties of gate insulator on N-polar and Ga-polar GaN MIS capacitor

○Takahiro Gotow[1], Tatsushi Suka[1], Yasuyuki Miyamoto[1] (1.Tokyo Institute of Technology)

9:58 AM - 10:05 AM

[D-7-06] SiO_2/n-GaN MOS structures with low interface state density formed by plasma-enhanced atomic layer deposition method

○Keito Aoshima[1], Noriyuki Taoka[1], Masahiro Horita[1,2], Jun Suda[1,2]
(1.Nagoya Univ., 2.IMaSS, Nagoya Univ.)

10:05 AM - 10:12 AM

[D-7-07] Corner Shape Control of GaN Trench Structure Formed by Inductively Coupled Plasma Reactive Ion Etching

○Shinji Yamada[1], Takashi Ishida[1], Toshiyuki Nakamura[2], Ryuichiro Kamimura[2], Jun Suda[1], Tetsu Kachi[1] (1.Nagoya Univ., 2.ULVAC, Inc.)

10:12 AM - 10:19 AM

[D-7-08] High-breakdown-voltage $Al_{0.36}Ga_{0.64}N$-channel HFETs with a dual AlN/AlGaInN barrier layer and selective-area regrowth ohmic contacts

○Akiyoshi Inoue[1], Sakura Tanaka[1], Takashi Egawa[1], Makoto Miyoshi[1] (1.Nagoya Inst. Tech.)