2018 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Special Short Course

ssdm 50th

Mon. September 10, 2018
Yayoi Auditorium, Ichijo Hall Chair: S. Migita (AIST)

— Si Technology Frontier —

9:00 - 9:50

Akihisa Sekiguchi Tokyo Electron

"Process and Manufacturing Science"

One of the essential components needed to realize the evolution of Si technology is the process equipment. As scaling continues into the 1x/1y/1z/1a generation in DRAM, low nm range in logic, and over 96 layers of stacked devices for VNAND, the requirements or "performance specifications" needed to deliver process technologies suitable for their production is, simply put, "incredible" . During the course, requirements for the device technology will be paired with process equipment technology so that the audience can quickly come to understand the current problems, challenges and solutions from an equipment supplier`s point of view. A deeper dive on the Si device evolution will be covered in the Advanced Si Devices lecture to be given by Maeda-san, and therefore the focus of this portion will be more on the process-equipment aspect of the technology.

9:50 - 10:40

Shigenobu Maeda Samsung Electronics

"Device Architecture"

Si technology has been evolved so far by scaling. The scaling law provides power, performance, and area improvement at the same time, and cost is also reduced as a result of area reduction. Although long time has already passed since limit of scaling started to be mentioned, cutting edge logic process development such as 7nm, 6nm, 5nm, 4nm, 3nm, is still continuing under huge competition in reality. In this short course, presenter will overview past decades of Si technology evolution history, and introduce recent cutting edge Si technology which indicates that Si technology will continue to be a mainstream for a while, and regain cost effectiveness by EUV lithography. He will also give Insight on future evolution of Si technology.

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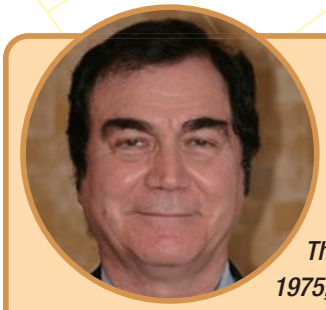
10:50 - 11:40

James H Stathis IBM Research

"Reliability Science"

Gate dielectrics have been key to MOS transistor performance and, at the same time, their Achilles heel for reliability. The standard failure mechanisms -- breakdown, threshold voltage instability -- have not changed, but insulator thickness reduction and materials changes continually challenge our understanding. This lecture will describe new and improved physics understanding and statistical methods which are needed to enable us to anticipate the effects of scaling on reliability. Topics to be covered include: the electrical and physical limits to gate dielectric scaling, recent insights into NBTI (Negative Bias Temperature Instability) and hot carrier damage, physical models of dielectric breakdown, projection to use condition including Weibull and non-Weibull statistics, progressive breakdown, and implications for IC reliability.



11:40 - 12:30

Paolo Gargini Chairman IRDS (IEEE)

"Roadmap for the Next"

The Electronics industry has benefitted from roadmap guidance given by Dr. Gordon Moore in 1965 and 1975, respectively. The subsequent NTRS and ITRS primarily provided devices to systems (bottom up) guidance from 1991 to 2013. However the ecosystem of the electronics industry drastically changed with the introduction of smart phones, tablets and most of all with the ubiquitous access to the Internet made especially possible by extensive wireless coverage of most urban areas. It was therefore necessary to drastically restructure the roadmap process and more strongly connect device requirements with system requirements. The first step towards this renovation consisted making an alliance with the Rebooting Computing Initiative (RCI) and subsequently forming the new International Roadmap for Devices and System (IRDS) under the IEEE umbrella. The 2017 IRDS (https://irds.ieee.org/reports) is aimed at providing a first step encompassing a system to device (top down) and a device to system (bottom up) guidance to the electronics industry. Highlight of the IRDS will be presented in the short course.

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