2017 International Conference on Solid State Devices and Materials
= Short Course B =
Si-related Technology
September 19, 2017 Sendai International Center, Sendai, Japan

Organizer

Dr. Masato Koyama (Toshiba Corporation)

Speakers

13:00-13:50 "CMOS Scaling and Integration: Present Status and Roadmap"

Prof. Toshiro Hiramoto (The University of Tokyo)

The exponential improvement by CMOS scaling still continues. The 10nm FinFET technologies are now in mass production and the 7nm FinFET technologies have been reported in conferences. The developments of the 5nm technology are under way. In this short course, the historical trends of advanced CMOS devices in the past and at present will be reviewed in terms of device speed and energy dissipation, and the future technological trends predicted by the roadmap will be outlined. On the other hand, new device aspects that are required in the IoT (Internet of Things) era will also be touched.

13:50-14:40 "Advanced MOS device technology"

Prof. Shinichi Takagi (The University of Tokyo)

Traditional CMOS scaling has confronted a variety of difficulties, attributed to essential Si material properties as well as practical problems such as limitation of lithography, performance variation, cost and so on. Here, reduction in both device foot print and power consumption is the most serious concerns for realizing future integrated systems. Ultrathin body channels and multi-gate structures, resulting in FinFETs and nanowire MOSFETs, are indispensable in order to minimize short channel effects and to decrease the device size. On the other hand, the reduction in power consumption requires the decrease in supply voltage, which can be realized by two strategies. One is the increase in on-current due to higher mobility (velocity) channel materials with low effective mass. The other is the development of steep slope devices with lower sub-threshold swing than CMOS. From these points of view, this short course will deliver the current status and future prospects of these advanced MOS device technologies for 5-nm technology node and beyond with an emphasis on non-conventional materials and device structures for low power applications. The content can include typical examples of advanced CMOS, SiGe/Ge/III-V CMOS and steep slope devices such as tunneling FETs and negative capacitance gate MOSFETs.

Break (20min.)

15:00-15:50 "Formation Mechanisms of Gate Oxide Films"

Prof. Takanobu Watanabe (Waseda University)

Thermally grown SiO2 film has played a central role in the gate insulating technology. The kinetics of the thermal oxidation of silicon surfaces has long been discussed based on the Deal-Grove model, but it cannot be applied to thin oxide films less than ~30 nm formed in a dry oxygen ambient. The so-called "layer-by-layer growth mode" also cannot be explained by the Deal-Grove model. This lecture ruminates on the initial oxidation mechanism of Si surfaces, shedding light on the presence of the strained oxide layer in the vicinity of the SiO2/Si interface. The latest understanding will play an essential role in the on-going evolution from planar devices to three-dimensional multi-gate devices.

Implementation of high-k/metal gate stack poses a new challenge in controlling the threshold voltage of CMOS devices. The threshold voltage is known to be shifted by an electric dipole layer formed at the interface between high-k oxide and underling interfacial SiO2 layer. This lecture will address the origin of the dipole layer focusing on a recent molecular dynamics studies, in which dipoles at various high-k/SiO2 interfaces are successfully reproduced in the course of redistribution of ion species around the interface.

15:50-16:40 “Challenges in Si device and process technology for dimensional and voltage scaling”

Dr. Takashi Matsukawa (National Institute of Advanced Industrial Science and Technology)

CMOS scaling has been conducted by reducing transistor dimension and supply voltage Vdd. FinFETs having the gate surrounding the channel have been introduced to suppress off-leakage current which becomes unacceptable level for bulk-planar MOSFETs with the gate length of 30 nm and less. With the shrink of the transistor size, random variation caused by discreteness of dopant atoms also causes the characteristics variability significantly. Since the FinFETs can be operated with an undoped channel, the FinFETs can also suppress the characteristics variability effectively. The suppression of the off-leakage, i.e. improvement of the subthreshold slope, and the suppression of the characteristics variability both are beneficial for conducting scaling of Vdd. Half of this lecture is given for the FinFET device and process technology including suppression of the characteristics variability. In order to conduct Vdd scaling further, achievement of steeper on/off characteristics beyond the theoretical limit of MOSFETs will be needed. Latter half of this lecture is given for a silicon-base tunnel FET, which is one of the candidate of the super-steep transistors.

16:40-17:30 “Future Si functional nano-devices and their important analyzing technologies”

Prof. Yasuo Takahashi (Hokkaido University)

Higher functionality of Si CMOS logic LSIs has been achieved by means of miniaturization and integration. The progress is in the process of limiting due to the miniaturization difficulties and increase of power density. On the one hand, fabrication technologies for nanoscale structure have been already developed to create new functional devices for quantum computing or neural network for AI (Artificial Intelligence). Here, the fabrication methods and their functionalities are introduced. It is not so hard to make Si single-electron islands though the formation of the tunnel barrier that isolates the island one from the other is still an issue. To build the neural-network hardware for AI, analog nonvolatile memories are needed. There are many candidates, such as ferroelectric memory, resistive memory, phase change memory, etc.

Another important subject for the nanoscale devices is how to analyze the failure mechanism. Here, in-situ observation of the nanoscale devices in a transmission electron microscopy (TEM) is introduced. One of the problems of TEM was that it needs very thin sample less than 100 nm. But now, device size has already less than 100 nm. The method is powerful to analyze the operation mechanisms and reliability of nano-devices.