2014 International Conference on Solid State Devices and Materials
= Short Course B =
Functional Devices in Integrated Systems
September 8, 2014 Tsukuba International Congress Center, Ibaraki, Japan

Organizer

Prof. Hitoshi Wakabayashi (Tokyo Tech)

Speakers

13:05-13:55 "Multigate Transistors: Pushing Moore's law to the limit"

Dr. Jean-Pierre Colinge (TSMC)

Improvements in electrostatic channel control allow FinFETs and trigate FETs to extend Moore's law down to gate lengths of 15-20nm. Further scaling may require the better control that is provided by multigate devices. Using multigate FET architectures, gate length scaling down to 5 and 3 nm has been demonstrated experimentally and theoretically, respectively. At these dimensions, quantum confinement begins to appear and new effects such as drain current oscillations and tunneling through soft barriers can be observed. FET to SET and metal-semiconductor transitions resulting from quantum confinement present opportunities for new types of devices. Examples of circuits and sensor applications using multigate/nanowire transistors will be given.

13:55-14:45 "Volatile and Non-volatile Semiconductor Memories: Past, Present and Future Outlook"

Mr. Toshiharu Watanabe (Toshiba Corporation)

There are two kinds of memories. One is volatile memories such as DRAM and SRAM. They are widely used as a working memory of computers and so on. The other is nonvolatile memories and the typical example of them is NAND Flash which is produced in high volume and widely used as a data storage of smart phone, tablet PC, digital camera, SSD and so on. Although the scaling limitation of traditional NAND is said to be around the corner, 3D structure is going to be adopted in order to realize even higher Bit-density. In addition to that, new nonvolatile memories such as MRAM and ReRAM have been attracting attention. They may offer faster Program/Erase or Read speed and are expected to replace some part of both volatile and nonvolatile memories. This short course will cover structure, operation principle, feature and application of these memories. The history and present status, and future trend will be also covered.

Break (15 min.)

15:00-15:50 "Co-designs of Devices and Circuits to improve performances of RF/Analog and High voltage I/Os in SoC/MCUs"

Dr Yoshihiro Hayashi (Renesas Electronics Corporation)

Human life is enriched by seamless man-machine interfaces by connecting digital worlds and analog ones. Here, several methodologies are explained how to boost performances of peripheral functions such as RF/analog and high voltage I/Os. The key factor is "co-design" to modify both of the device structures and the circuit configurations. In this lecture are shown a low-loss RF-MOSFET with a special metal-backed gate and compact RF- LCVCO and RF-PLL with compact "3D-inductors". An add-on high-voltage I/O with wide band-gap oxide-semiconductors, such as IGZO, is also explained.

15:50-16:40 "Recent Challenges and Solutions in Image Sensor Technology"

Mr. Hideo Nomura (Sony Corporation**)**

In the last decade, CMOS image sensor market has been growing rapidly according to the growth of camera phone market, and CMOS image sensors have become main stream for camera technologies due to excellent features such as minimal power consumption, high frame rate, and low noise.

In this lecture, I talk about the recent challenges and solutions in CMOS image sensor technology, that have been applied to back illuminated and stacked sensors.

16:40-17:30 "Integrated MEMS Technology for Construction of Diverse Functional Devices"

Prof. Hidekuni Takao (Kagawa University)

These days, the word "integrated MEMS technology" is widely used for various fabrication approaches related to micro sensors and highly functional CMOS devices. Silicon based MEMS has advantageous to integrate CMOS circuit function

for enhancement of MEMS device functionality. On the other hand, MEMS device structure is utilized for CMOS performance enhancement in some devices. Both CMOS and MEMS can be the leading part of the integrated MEMS devices. In order to realize such diverse functional devices, post-CMOS integration process is the most suitable approach to integrated MEMS device structures on CMOS wafers. Also, monolithic approach has a higher ability than 2-chip (MEMS and CMOS) approach especially in arrayed devices. However, advance of heterogeneous3D integration process will make it possible to fabricate high performance arrayed devices in 2-chips configurations. In this lecture, the essential features and fabrication technologies of integrated MEMS/CMOS devices are discussed, and the future of the technology is estimated based on the essential difference between CMOS and MEMS devices..