2013 International Conference on Solid State Devices and Materials
= Short Course A =
Fundamentals on Advanced CMOS/Memory Technologies
September 24, 2013 Hilton Fukuoka Sea Hawk, Fukuoka, Japan

Organizer

Prof. Shinichi Takagi (The University of Tokyo)

Speakers

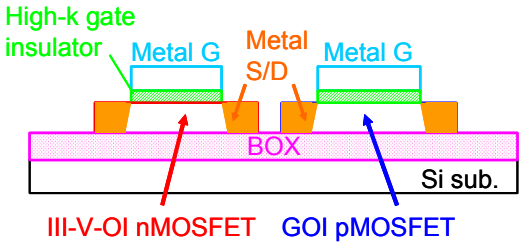
13:00-14:30 "Present Status and Future Trend of CMOS Scaling"

Prof. Toshiro Hiramoto (The University of Tokyo)

The CMOS devices for VLSI have been scaled down for more than forty years in order to attain higher speed, lower power, higher integration, and lower cost. The gate length has reached as small as 20 nm and more than billion transistors are now integrated in a single chip. The CMOS devices are certainly in both the nanometer regime and the giga-scale integration regime. However, there are a lot of technical barriers to realize such small and giga-scale devices. In this short course, the historical trend of MOSFETs in the past and the future trend predicted by ITRS are compared in order to look into the technological barriers that should be targeted. In particular, issues of power dissipation and variability are reviewed in detail. Then, the technology trend of non-conventional devices with new structures and new materials is described.

14:30-16:00 "High Mobility Channel CMOS Technology"

Prof. Shinichi Takagi (The University of Tokyo)



It has been recognized that MOSFETs with high mobility channels such as Ge and III-V semiconductors are expected for overcoming difficulties of advanced CMOS and realizing high performance LSIs under 10 nm regime. The ITRS 2013 is predicting that the timeline for introducing Ge and/or InGaAs channels into mass production can be set around 2018. However, there are still many technological issues to be solved for realizing Ge/III-V MOSFETs on the Si platform in order to realize III-V/Ge MOSFETs. The critical issues for are listed as follows; (1) high quality Ge/III-V film formation on Si substrates (2) gate insulator formation with superior MOS/MIS interface quality (3) low resistivity source/drain (S/D) formation (4) total CMOS integration.

This short course will give the current status and future prospects of the high mobility channel MOSFET technologies for future integrated logic circuits with emphasizing fundamental aspects of these semiconductor materials. Possible and viable technological solutions for the above critical issues will also be addressed.

Break (15min.)

16:15-17:45 "Impact of 3D structured Memory and Spintronics based NV-Memory for High Performance & Low Power Systems"

Prof. Tetsuo Endoh (Tohoku University)

Recently, it is becoming difficult to achieve the target performance by technology development based solely on device scaling in semiconductor memories.

In this short course, Three-dimensional (3D) structured Memory and Spintronics based NV-Memory are discussed focusing on key technologies for High Performance and Low Power Systems. At first, 3D structured Memory technologies are mentioned. Especially, vertical MOSFET based novel SRAM cell, vertical MOSFET type DRAM cell including 1T-DRAM cell, and 3D NAND memories with the stacked vertical type memory array technologies are discussed.

Next, spintronics based nonvolatile memories such as STT-MRAMs are discussed. It is shown that STT-MRAMs have excellent potential for nonvolatile working memories such as nonvolatile main memories and embedded memories etc. for high performance and low power systems. Finally, it is shown that nonvolatile logic hybridized STT-MRAM and CMOS logic with fine-grained level have big impact from the viewpoint of the super-low power consumption system.

Finally, we will summarize that 3D structured Memory and spintronics based nonvolatile memory will spur revolution on semiconductor memories.