History of SSDM AWARD

Year of the award	Awarded thesis			
	Conference number held	Thesis number	Name of awardees	Title of thesis
1st (1990)	1st	4-1	Y. Tarui, Y. Hayashi and T. Sekigawa, ETL, Japan	“Diffusion Self-Aligned MOST: A New Approach for High Speed Device”
2nd (1991)	6th	A-1-1	T. Tsukada, Hitachi, Japan	“Buried-Heterostructure Injection Lasers”
3th (1992)	11th	C-3-4	M. Tajima, A. Yusa* and T. Abe**, ETL, *Komatsu Electronic Metals and **Shin-Etsu Handotai, Japan	“Characterization of Residual Impurities in Highly Pure Si Crystals by Photoluminescence Technique”
4th (1993)	7th	A-1-1	Y. Horiike and M. Shibagaki, Toshiba, Japan	“A New Chemical Dry Etching”
5th (1994)	10th	A-1-4	M. Koyanagi and N. Hashimoto, Hitachi, Japan	“Novel High Density, Stacked Capacitor MOS RAM”
6th (1995)	5th	3-4	H. Yonezu, I. Sakuma, T. Kamejima, M. Ueno, K. Kobayashi, K. Nishida, Y. Nannichi and I. Hayashi, Nippon Electric, Japan	“Degradation of AlxGa1-xAs Double Heterostructure Lasers”
7th (1996)	11th	A-3-7	K. Izumi, M. Dohken, H. Ariyoshi, NTT, Japan	“High Speed C-MOS IC Using Buried SiO2 Layers Formed by Ion Implantation”
8th (1997)	12th	A-4-7	T. Sakai, Y. Kobayashi, H. Yamauchi, M. Sato and T. Makino, NTT, Japan	“High Speed Bipolar ICs Using Super Self-Aligned Process Technology”
9th (1998)	12th	C-3-9(LN)	T. Mimura, S. Hiyamizu, H. Hashimoto and H. Ishikawa, Fujitsu Labs., Japan	“An Enhancement-Mode High Electron Mobility Transistor for VLSI”
10th (1999)	6th	B-2-1	H. Abe, Mitsubishi, Japan	"The Application of Gas Plasma to the Fabrication of MOS LSI (Invited)"
	18th	B-8-4	Y. Matsushita, M. Wakatsuki and Y. Saito, Toshiba, Japan	"Improvement of Silicon Surface Quality by H2 Anneal"
11th (2000)	4th	6-1	T. Warabisako, I. Yoshida and T. Tokuyama, Hitachi, Japan	"Properties of MOS Structures Prepared on Substrates Having Ion-Implanted Impurity Distribution Profile"
12th (2001)	6th	B-3-3	M. Esashi and T. Matsuo, Tohoku Univ., Japan	"Biomedical Cation Sensor Using Field Effect of Semiconductor"
13th (2002)	3th	5-5	H. Hara, T. Sato, Y. Takeishi, K. Ohuchi, H. Tango, Y. Ohmori, H. Iizuka, Y. Yasuda, F. Masuoka, Toshiba Research and Development Center, Japan	"Avalanche-Injection MOS Read-Only Memory"

History of SSDM AWARD

Year of the award	Awarded thesis			
	Conference number held	Thesis number	Name of awardees	Title of thesis
14th (2003)	24th	S-1-1	I. Akasaki, H. Amano, Meijo Univ., Japan	Room Temperature Ultraviolet/Blue Light Emitting Devices Based on AlGaN/GaN Multi-Layered Structure
15th (2004)	22th	S-CII-4	Y. Hayashide, H. Miyatake, J. Mitsuhashi, M. Hirayama, T. Higaki and H. Abe, Mitsubishi Electric, Japan	Fabrication of Storage Capacitance-Enhanced Capacitors with a Rough Electrode
		S-CII-5	H. Watanabe, N. Aoto, S. Adachi, T. Ishijima, E. Ikawa and K. Terada, NEC, Japan	A New Stacked Capacitor Structure using Hemispherical-Grain (HSG) Poly-Silicon Electrodes
16th (2005)	19th	C-4-2	H. Matsunami, N. Kuroda, W. S. Yoo, S. Nishino, K. Shibahara, Kyoto Univ., Japan	Step-Controlled VPE Growth of SiC Single Crystals at Low Temperatures
17th (2006)	14th	B-2-3	H. Soda, Y. Motegi, K. Iga, Tokyo Tech.	Threshold Condition and Design of Surface Emitting GaInAsP/InP Injection Lasers
18th (2007)	3rd	5-2	H. Sakaki and T. Sugano, Univ. of Tokyo	Anistropic Channel Conductivity of a MOS Transistor on the (110) Surface of Silicon
19th (2008)	2nd	1-1	S. Furukawa and H. Ishiwara, Tokyo Tech.	Vacancy Distribution Theory for Ion-Implanted Target
20th (2009)	25th	PB-3-9	K. Natori, Univ. of Tsukuba	I-V Characteristics of SOI MOSFETs in Ballistic Mode
21st (2010)	18th	A-7-4	K. Yamada, Univ. of Tsukuba	Thermodynamical Approach to a New High Dielectric Capacitor Structure: W/HfO2/W
22nd (2011)	17th	C-3-9 LN	T. Sekigawa, Y. Hayashi*, K. Ishii** and S. Fujita***, Nanoelectronics Research Institute of AIST, *Nanosystem Research Institute of AIST, ** (Ex) Nanoelectronics Research Institute of AIST, ***Corporate Technology Planning Center, Ricoh Company, Ltd.	XMOS Transistor for a 3D-IC