Tuesday, September 25

Opening & Plenary Session (Main Hall)

Opening Session
Chair : T. Oomori, Mitsubishi Electric Corp.

9:30 Welcome Address
K. Kyuma, Mitsubishi Electric Corp.

9:40 Welcome Address
M. Konagai, The Japan Society of Applied Physics

Non-Technical Plenary Session

9:45 PL-1-1
"Future Prospects of Semiconductor Industry" T. Nomakuchi, AIST

SSDM Award/Paper Award Presentation
Chair : S. Miyazaki, Nagoya Univ.
K. Kyuma, Mitsubishi Electric Corp.

Technical Plenary Session
Chair : S. Miyazaki, Nagoya Univ.

10:45 PL-2-1
"It is a small world" A. Steegen, IMEC, Belgium

11:30 PL-2-2
"One-step Further of Wide Band-gap Semiconductor SiC" H. Matsunami, Kyoto Univ.

12:20-13:30 Lunch

2F B-1	2F B-2	1F C-1	1F C-2	1F D	1F E
A-1: Silicon Photonics (1): Active Devices (Area 7) (13:30-15:15) Chairs: J. Liu (Thayer School of Engineering Dartmouth College) H. Isshiki (Univ. of Electro-Communications)	**B-1: Volatile Memory (Area 4)** (13:30-14:40) Chairs: K. Hamada (Elpida Memory) M. Moniwa (Renesas Electronics)	**C-1: Carbon Interconnect (Area 2&13)** (13:30-15:10) Chairs: S. Sato (AIST) M. Sato (AIST)	**D-1: High-k MOS (Area 1)** (13:30-15:20) Chairs: T. Nabatame (NIMS) K. Kita (Univ. of Tokyo)	**E-1: Nanowire FET (Area 3)** (13:30-15:20) Chairs: T. Hiramoto (Univ. of Tokyo) M. Masahara (AIST)	**F-1: III-V MOSFETs (Area 6)** (13:30-15:00) Chairs: Y. Miyamoto (Tokyo Tech.) E. Y. Chang (National Chiao Tung Univ.)
13:30 A-1-1 (Invited) **Silicon/Ge/Silica monolithic photonic integration for telecommunications applications** *K. Yamada, T. Tsuchizawa, H. Nishi, R. Kou, T. Hiraki, H. Fukuda, Y. Ishikawa and K. Wada, NTT (Japan)*	**13:30 B-1-1 (Invited)** **Overview and Future Challenge of High Density DRAM for 20nm and beyond** *Y. Hwang, J. Park, G. Y. Jin and C. Chung, Samsung Electronics Co., Ltd. (Korea)*	**13:30 C-1-1** **Highly Dense Carbon Nanotube Forests for Interconnect Applications** *J. Robertson, G. Zhong, C. Zhang and S. Esconjauregui, Univ. of Cambridge (UK)*	**13:30 D-1-1 (Invited)** **Ultimate Scaling of High-k Gate Dielectrics: Current Status and Challenges** *T. Ando[1], M. M. Martin[1], E. A. Cartier[1], B. P. Linder[1], J. Rozen[1] and K. Choi[2], [1]IBM T. J. Watson Research Center and [2]GLOBALFOUNDRIES (USA)*	**13:30 E-1-1 (Invited)** **High-Performance Tri-Gate Silicon Nanowire Transistors for Ultra-Low Power LSI** *M. Saitoh, C. Tanaka, K. Ota, K. Uchida and T. Numata, Tokyo Tech. (Japan)*	**13:30 F-1-1 (Invited)** **III-V 3D Transistors** *Y. Peide and J. J. Gu, Purdue Univ. (USA)*
14:00 A-1-2 **High Speed and High Efficiency Si Optical Modulator with MOS Junction, Using Large-Grain of Poly-Silicon Gate** *J. Fujikata[1,2], M. Takahashi[1,3], S. Takahashi[1,2], T. Akagawa[1,2], M. Noguchi[1,2], T. Horikawa[1,3], T. Nakamura[1,2] and Y. Arakawa[1,4], [1]PECST, [2]PETRA, [3]AIST and [4]Univ. of Tokyo (Japan)*	**14:00 B-1-2** **Novel Field Effect Diode type Vertical Capacitorless 1T-DRAM Cell with Negative Hold Bit Line Bias Scheme for Improving the Hold Characteristics** *T. Imamoto[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]JST-CREST (Japan)*	**13:50 C-1-2** **Characterization of carbon nanotubes based vertical interconnects** *B. Vereecke[1], M. H. van der Veen[1], Y. Barbarin[1], M. Sugiura[2], Y Kashiwagi[2], D. J. Cott[1], C. Huyghebaert[1] and Zs. Tokei[1], [1]IMEC and [2]Tokyo Electron Ltd (Belgium)*	**14:00 D-1-2** **Effective Work Function Engineering for Aggressively Scaled Planar and FinFET-based Devices with High-k Last Replacement Metal Gate Technology** *A. Veloso[1], S. A. Chew[1], Y. Higuchi[2], L. A. Ragnarsson[1], E. Simoen[1], T. Schram[1], T. Witters[1], A. Van Ammel[1], H. Dekkers[1], H. Tielens[1], K. Devriendt[1], N. Heylen[1], F. Sebaai[1], S. Brus[1], P. Favia[1], J. Geypen[1], H. Bender[1], A. Phatak[3], M. S. Chen[4], X. Lu[4], S. Ganguli[4], Y. Lei[4], W. Tang[4], X. Fu[4], S. Gandikota[4], A. Noori[4], A. Brand[4], N. Yoshida[4], A. Thean[1] and N. Horiguchi[1], [1]IMEC , [2]Panasonic, [3]Applied Materials Belgium NV and [4]Applied Materials Inc. (Belgium)*	**14:00 E-1-2** **Analytical Formulas for the Drain Current of Silicon Nanowire MOSFET** *K. Natori, Toyko Tech. (Japan)*	**14:00 F-1-2 (Invited)** **InGaAs MOSFETs with Regrown Source: DC and RF Performance** *L. E. Wernersson, M. Egard and E. Lind, Lund Univ. (Sweden)*

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1F G	1F H	2F I	2F J	2F K	5F 554	5F 555
G-1: Optical and Electrical Properties in Nano Materials (Area 9) (13:30-15:15) Chairs: S. Kuroki (Hiroshima Univ.) Y. Uraoka (NAIST)	**H-1: Compound Solar Cells (Area 15)** (13:30-15:00) Chairs: H. Katagiri (Nagaoka National College of Technology) N. Kojima (Toyota Technological Institute)	**I-1: Nitrides (Area 8)** (13:30-15:00) Chairs: T. Nagata (NIMS) T. Iwai (Fujitsu)	**J-1: Image Sensor (Area 5)** (13:30-15:20) Chairs: M. Ikebe (Hokkaido Univ.) K. Kagawa (Shizuoka Univ.)		**L-1: Si Power Devices (Area 14)** (13:30-15:15) Chairs: G. Majumdar (Mitsubishi Electric) S. Shiraki (Denso)	**M-1: OTFT(1):Fabrication and Novel Structures (Area 10)** (13:30-15:15) Chairs: H. Usui (Tokyo Univ. of Agriculture and Technology) S. Naka (Univ. of Toyama)
13:30 G-1-1 (Invited) **Multiexciton generation and recombination in semiconductor nanomaterials** *Y. Kanemitsu, Kyoto Univ. (Japan)*	**13:30 H-1-1** **Defects in Electron-Irradiated and Hydrogenated GaAsN Grown by Chemical Beam Epitaxy** *B. Bouzazi, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)*	**13:30 I-1-1 (Invited)** **Interface Control of III-Oxide/Nitride Composite Structures** *M. Higashiwaki[1,2], S. Chowdhury[3], B. R. Swenson[3], U.K. Mishra[3], T. Igaki[4], T. Yamaguchi[4] and T. Honda[4], [1]National Inst. of Information and Communications Tech., [2]PRESTO, Japan Science and Tech. Agency, [3]Univ. of California and [4]Kogakuin Univ. (Japan)*	**13:30 J-1-1 (Invited)** **Advanced Radiation Image Sensors with SOI Technology** *Y. Arai, High Energy Accelerator Research Organization (Japan)*		**13:30 L-1-1 (Invited)** **Future role of power semiconductors: From "Silicon vs. WBG" to "Silicon and WBG** *I. Omura, Kyusyu Inst. of Tech. (Japan)*	**13:30 M-1-1 (Invited)** **Electrodeposited and Patterned Polymer Thin Films and Devices** *R. C. Advincula, Case Western Reserve Univ. (USA)*
14:00 G-1-2 **Disorder-Induced Enhancement of Avalanche Multiplication in a Silicon Nanodot Array** *N. Mori[1,2], M. Tomita[3], H. Minari[1,2], T. Watanabe[3] and N. Koshida[4], [1]Osaka Univ., [2]JST CREST, [3]Waseda Univ. and [4]Tokyo Univ. A&T (Japan)*	**13:45 H-1-2** **Enhancement of Light Harvesting and Power Conversion Efficiency in GaAs Solar Cell Using Flexible Nano-pattern PDMS Film** *H. V. Han, H. C. Chen, C. C. Lin, H. S. Shih, T. Y. Tsao, Y. L. Yeh, Y. L. Tsai, H. C. Kuo and P. Yu, National Chiao Tung Univ. (Taiwan)*	**14:00 I-1-2** **MOVPE growth of GaN epitaxial films on AlN/h-BN/AlN double hetero-structures** *Y. Kobayashi, Y. Noguchi, K. Kumakura, T. Akasaka, H. Yamamoto and T. Makimoto, NTT Basic Research Laboratories (Japan)*	**14:00 J-1-2** **A 2.8 μm pixel-pitch 55 ke− Full-Well Capacity Global-Shutter CMOS Image Sensor Using Lateral Overflow Integration Capacitor** *S. Sakai, Y. Tashiro, R. Kuroda and S. Sugawa, Tohoku Univ. (Japan)*		**14:00 L-1-2** **Real Time Failure Imaging of Power Semiconductors under Power Stress using Scanning Acoustic Tomography** *A. Watanabe and I. Omura, Kyushu Inst. of Tech. (Japan)*	**14:00 M-1-2** **Simple Push-coating for High-Performance Polymer Thin-Film Transistors** *M. Ikawa, H. Matsui, H. Minemawari, J. Tsutsumi, T. Yamada and T. Hasegawa, FLEC AIST (Japan)*

Tuesday, September 25

2F B-1

A-1: Silicon Photonics (1): Active Devices (Area 7)

14:15 A-1-3
Electrical and Optical Characteristic Modeling of Silicon Modulator
T. Akagawa[1,2], S. Akiyama[1,2], T. Baba[1,2], M. Imai[1,2] and T. Usuki[1,2], [1]Inst. for Photonics-Electronics Convergence System Tech. (PECST) and [2]Photonics Electronics Tech. Research Association (PETRA) (Japan)

14:30 A-1-4
Strain Tuning of Franz-Keldysh Ge Electro-Absorption Modulation
R. Kuroyanagi[1], M. L. Nguyen[1], T. Tsuchizawa[2], Y. Ishikawa[1], K. Yamada[2] and K. Wada[1], [1]The Univ. of Tokyo and [2]NTT Microsystem Tech. Labs., NTT Corp. (Japan)

14:45 A-1-5
Optimization of Taper Structures for III-V on Silicon Lasers
D. Van Thourhout[1], S. Keyvaninia[1], G. Roelkens[1], M. Lamponi[2], F. Lelarge[2], J. M. Fedeli[3], S. Messaoudene[3] and G. H. Duan[2], [1]Ghent Univ.-IMEC, [2]III-V lab and [3]CEA-LETI (Belgium)

15:00 A-1-6
Operation Power Reduction of Si Electro-optics Switch by Decreasing Current Leakage
T. Matsumoto, S. Sekiguchi, T. Kurahashi and K. Morito, Fujitsu Labs. (Japan)

2F B-2

B-1: Volatile Memory (Area 4)

14:20 B-1-3
Multi-Level Cell Memory with High-Speed, Low-Voltage Writing and High Endurance Using Crystalline In-Ga-Zn Oxide Thin Film Transistor
T. Ishizu, H. Inoue, T. Matsuzaki, S. Nagatsuka, Y. Okazaki, T. Onuki, A. Isobe, Y. Shionoiri, K. Kato, T. Okuda, J. Koyama and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd. (Japan)

1F C-1

C-1: Carbon Interconnect (Area 2&13)

14:10 C-1-3
Highly Thermo-stable and Oriented Catalytic Metal using Co/Ir/Ta Layer Stack for Graphene Growth
M. Kitamura, Y. Yamazaki, M. Wada, T. Saito, M. Katagiri, M. Suzuki, A. Isobayashi, N. Sakuma, A. Sakata , A. Kajita and T. Sakai, Low-power Electronics Association & Project (LEAP) (Japan)

14:30 C-1-4
Heat-Resistant Co-W Catalytic Metals for Multilayer Graphene CVD
S. Baba[1], S. Kuwahara[1], Y. Karasawa[1], H. Hanai[1], Y. Yamazaki[2], N. Sakuma[2], A. Kajita[2], T. Sakai[2] and K. Ueno[1], [1]Shibaura Inst. Tech. and [2]LEAP (Japan)

14:50 C-1-5
Initial Growth Observation of Networked Nano Graphite on SiO_2 (90 nm)/Si dependent on Process Gas Concentration
Y. Ojiro[1], S. Ogawa[1], M. Satou[2], M. Nihei[2], Y. Takakuwa[1] and N. Yokoyama[2], [1]Tohoku Univ. and [2]AIST/GNC (Japan)

1F C-2

D-1: High-k MOS (Area 1)

14:20 D-1-3
Enhanced Hole Mobility in High-k Gated pMOSFETs by Dislocation-free Epitaxial Si/Ge Super-lattice Channel
L. J. Liu[1], K. S. Chang Liao[1], C. H. Fu[1], H. C. Hsieh[1], C. C. Lu[1], T. K. Wang[1], P. Y. Gu[2] and M. J. Tsai[2], [1]National Tsing Hua Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)

14:40 D-1-4
RMG Technology Integration in FinFET Devices
G. Boccardi, R. Ritzenthaler, M. Togo, T. Chiarella, M. S. Kim, S. Yuichiro, A. Veloso, S. A. Chew, E. Vecchio, S. Locorotondo, K. Devriendt, P. Ong, S. Brus, N. Horiguchi and A. Thean, IMEC (Belgium)

15:00 D-1-5
Fabrication and Demonstration of Ultra Short Channel Atomically Thin SOI MOSFETs (ATFET) Using Anisotropic Wet Etching and Lateral Dopant Diffusion
S. Migita, Y. Morita, M. Masahara and H. Ota, GNC-AIST (Japan)

1F D

E-1: Nanowire FET (Area 3)

14:20 E-1-3
Extraction of Carrier Mobility in Intrinsic Channel Tri-Gate Single Silicon Nanowire MOSFETs
K. Mao, T. Saraya and T. Hiramoto, Univ. of Tokyo (Japan)

14:40 E-1-4
High Performance Nanoscale n-MOS Gate-all-around poly-Si Thin Film Transistors by Microwave Annealing
M. S. Yeh[1], Y. C. Wu[1], Z. Y. Tang[1], H. F. Hung[1] and Y. J. Lee[2], [1]Univ. of National Tsing Hua and [2]National Nano Device Labs (Taiwan)

15:00 E-1-5
Systematic Study of Back-Gate Bias Effects in Ultrathin-BOX Tri-gate (UTBT) Transistor with 10 nm-Diameter Nanowire Channel
K. Ota, M. Saitoh, C. Tanaka and T. Numata, Toshiba Corp. (Japan)

1F E

F-1: III-V MOSFETs (Area 6)

14:30 F-1-3
BEOL InGaAs nMOSFETs on Polyimide
T. Maeda[1], H. Ishii[1], T. Itatani[1], W. Jevasuwan[1], O. Ichikawa[2], M. Hata[2] and T. Yasuda[1], [1]AIST and [2]Sumitomo Chemical (Japan)

14:45 F-1-4
Effective Mobility Enhancement in Al_2O_3/InSb/Si Quantum Well MOSFETs for Thin InSb Channel Layers
T. Ito[1], A. Kadoda[1], K. Nakayama[1], Y. Yasui[1], M. Mori[1], K. Maezawa[1], E. Miyazaki[2] and T. Mizutani[2], [1]Univ. of Toyama and [2]Nagoya Univ. (Japan)

Coffee Break

2F B-1

A-2: Silicon Photonics (2): Fabrication & Materials (Area 7)
(15:40-17:25)
Chairs: D. V. Thourhout (Ghent Univ.)
Y. Tanaka (Fujitsu)

15:40 A-2-1
The Impacts of ArF Excimer Immersion Lithography on Integrated Silicon Photonics Technology
H. Takahasi[1,2], M. Toyama[1,3], M. Seki[1,3], D. Shimura[1,2], K. Koshino[1,3], N. Yokoyama[1,3], M. Ohtsuka[1,3], A. Sugiyama[1,3], E. Ishitsuka[1,3], T. Sano[1,3] and T. Horikawa[1,3], [1]Inst. for Photonics-Electronics Convergence System Tech.(PECST), [2]Photonics Electronics Tech. Research Association(PETRA) and [3]National Inst. of Advanced Industrial Science and Tech.(AIST) (Japan)

2F B-2

B-2: Flash Memory (Area 4)
(15:40-17:15)
Chairs: E. Yang (eMemory Technology)
S. Shuto (Toshiba)

15:40 B-2-1
New Erase Verify Scheme for Improving the Cycling Endurance of 2x nm NAND Flash Cell
J. Kim, T. Youn, S. Seo, N. Park, S. Yi, E. Park, H. Kim, H. Yang, K. Noh, S. Park and S. Lee, SK hynix Inc. (Korea)

1F C-1

C-2: Nanowire Growth and Characterization (Area 13)
(15:40-17:10)
Chairs: M. Arita (Univ. of Tokyo)
K. Kawaguchi (Fujitsu)

15:40 C-2-1 (Invited)
Growth and Characterization of Novel Material and Heterostructure III-V Semiconductor Nanowires
S. Lehmann[1], S. Ghalamestani[1], D. Jacobsson[1], M. Heurlin[1], J. Bolinsson[1], M. E. Messing[1], L. E. Wernersson[3], J. Johansson[1], P. Caroff[4], K. Deppert[1] and K. A. Dick[1,2], [1]Solid State Physics, Lund Univ., [2]Polymer & Materials Chemistry, Lund Univ., [3]Electrical and Information Technologies, Lund Univ. and [4]Institut d'Electronique, de Microelectronique et de Nanotechnologie, UMR (Sweden)

1F C-2

D-2: Characterization in Gate Stack (1) (Area 1)
(15:40-17:10)
Chairs: H. Nohira (Tokyo City Univ.)
T. Yamaguchi (Renesas)

15:40 D-2-1 (Invited)
Raman Spectroscopy for Strain Measurement in State-of-the-art LSI
A. Ogura[1], D. Kosemura[1], M. Takei[2] and M. Tomita[2], [1]School of Science and Tech., Meiji Univ. and [2]JSPS Research Fellow (Japan)

1F D

E-2: Fin FET (Area 3)
(15:40-17:25)
Chairs: M. Masahara (AIST)
S. Yamaguchi (SONY)

15:40 E-2-1 (Invited)
Device Architectures and Their Integration Challenges for 1x nm Node: FinFETs with High Mobility Channel
N. Horiguchi, G. Zschaetzsch, Y. Sasaki, A. K. Kambham, M. Togo, L. -Å. Ragnarsson, J. Mitard, J. Franco, G. Eneman, G. Hellings, L. Witters, T. Romeo, L. Pantisano, N. Waldron, D. Lin, N. Collaert, W. Vandervorst and A. Thean, Inst. voor Ker and Stralings Fysika (Belgium)

1F E

F-2: High Frequency GaN Devices (Area 6)
(15:40-17:25)
Chairs: N. Hara (Fujitsu)
T. Suzuki (JAIST)

15:40 F-2-1 (Invited)
Sub-Millimeter-Wave GaN-HEMT Technology
K. Shinohara, D. Regan, A. Corrion, D. Brown, I. Alvarado Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden and M. Micovic, HRL Laboratories (USA)

Tuesday, September 25

1F G

G-1: Optical and Electrical Properties in Nano Materials (Area 9)

14:15 G-1-3
Floating Gate Memory with High-density Nanodot Array Formed Utilizing Ti-binding Dps
H. Kamitake[1,2], K. Ohara[1], M. Uenuma[1,2], B. Zheng[1,2], Y. Ishikawa[1,2], I. Yamashita[1,2,3] and Y. Uraoka[1,2], [1]Nara Inst. of Science and Tech., [2]CREST and [3]ATRL, Panasonic Corporation (Japan)

14:30 G-1-4
Performance Revelation and Optimization of Gold Nanocrystal for Future Nonvolatile Memory Application
C. T. Lin[1], P. W. Huang[1], J. C. Wang[1], L. C. Chang[2], C. H. Chen[1], Y. Y. Chen[1] and C. S. Lai[1], [1]Chang Gung Univ. and [2]Ming Chi Univ. of Tech. (Taiwan)

14:45 G-1-5
3-Dimensional and Defect-free Etching by Neutral Beam for MEMS Applications
T. Kubota[1,2], A. Wada[1], Y. Yanagisawa[1], B. Altansukh[1], K. Miwa[2], T. Ono[1] and S. Samukawa[1,2], [1]Tohoku Univ. and [2]BEANS (Japan)

15:00 G-1-6
Direct Observation of Microstructure Changes Arising from Electromigration
Y. Murakami, M. Arita, K. Hamada and Y. Takahashi, Hokkaido Univ. (Japan)

G-2: Single Electron Devices (Area 9)
(15:40-17:10)
Chairs: H. Inokawa (Shizuoka Univ.)
T. Tanamoto (Toshiba)

15:40 G-2-1
Discrete Energy Levels in Synthesized Au Nanoparticle by Chemically Assembled Single-Electron Transistors
S. Kano[1,2], K. Maeda[1,2], D. Tanaka[2,3], T. Teranishi[2,4], L. W. Smith[5], C. G. Smith[5] and Y. Majima[1,2,6], [1]Tokyo Tech., [2]CREST-JST, [3]Univ. of Tsukuba, [4]Kyoto Univ., [5]Univ. of Cambridge and [6]Sunchon National Univ. (Japan)

1F H

H-1: Compound Solar Cells (Area 15)

14:00 H-1-3
Reduction of Operating Temperature in 25 Series-Connected 820X CPV
Y. Ota[1], T. Sueto[1], H. Nagai[2], K. Araki[2] and K. Nishioka[1], [1]Univ. of Miyazaki and [2]Daido steel (Japan)

14:15 H-1-4
Novel High-sensitivity Broadband Image Sensor with CIGS Thin Films
Y. Ota[1], T. Maekawa[1], O. Matsushima[1], H. Sekiguchi[1], T. Maeda[1], T. Fujii[1], D. Ohnishi[1], H. Takasu[1] and S. Niki[2], [1]ROHM Corp. Ltd. and [2]National Inst. of Advanced Indus. Sci. and Tech. (Japan)

14:30 H-1-5
Direct Bonding using a-Si:H Thin Films for the Fabrication of Chalcopyrite Tandem Solar Cells
S. Oonishi, Y. Kurokawa and A. Yamada, Tokyon Inst. of Tech. (Japan)

14:45 H-1-6
First-Principles Study of Diffusion of Constituent Atom in $CuInSe_2$
S. Nakamura, T. Maeda and T. Wada, Ryukoku Univ. (Japan)

H-2: Crystalline Silicon Solar Cells (Area 15)
(15:40-17:10)
Chairs: K. Ohdaira (JAIST)
T. Ujihara (Nagoya Univ.)

15:40 H-2-1 (Invited)
Crystal Growth Mechanisms of Silicon during Melt Growth Processes
K. Fujiwara, H. Koizumi, K. Nozawa and S. Uda, Tohoku Univ. (Japan)

2F I

I-1: Nitrides (Area 8)

14:15 I-1-3
Formation of a Step-Free Ultrathin InN Layer on a Step-Free GaN Surface
T. Akasaka, A. Berry, Y. Kobayashi and H. Yamamoto, NTT Corp. (Japan)

14:30 I-1-4
Optically pumped lasing action around unusual wavelength of 390 nm in hexagonal GaN microdisks fabricated by rf-MBE
T. Kouno[1], M. Sakai[2], K. Kishino[3] and K. Hara[1], [1]Shizuoka Univ., [2]Univ. of Yamanashi and [3]Sophia Univ. (Japan)

14:45 I-1-5
Nano-Patterned Sapphire Substrates-Induced Strain-Related Quantum-Confined-Stark-Effect Behaviors of InGaN-Based Light-Emitting Diodes
V. C. Su[1], Y. J. Chen[1], M. L. Lee[1], Y. H. You[1], C. H. Kuan[1], P. H. Chen[1], C. J. Hsieh[1], R. M. Lin[2] and S. F. Yu[2], [1]National Taiwan Univ. and [2]Chang Gung Univ. (Taiwan)

I-2: Growth and Characterization of Group IV Related Materials (Area 8)
(15:40-17:25)
Chairs: T. Suemasu (Tsukuba Univ.)
K. Hara (Shizuoka Univ.)

15:40 I-2-1
Increase of Si0.5Ge0.5 Bulk Single Crystal Size as Substrates for Strained Ge Epitaxial Layers
K. Kinoshita[1], O. Nakatsuka[2], Y. Arai[1], K. Taguchi[3], H. Tomioka[3], R. Tanaka[3] and S. Yoda[1], [1]JAXA, [2]Nagoya Univ. and [3]AES Co. Ltd. (Japan)

2F J

J-1: Image Sensor (Area 5)

14:20 J-1-3
Experimental Verification of a CMOS Imager with Block-parallel Scanning for Focal-plane Pinhole Effect in Multi-beam Confocal Microscopy
M.W. Seo, K. Kagawa, K. Yasutomi and S. Kawahito, Shizuoka Univ. (Japan)

14:40 J-1-4
A Column-Parallel Hybrid ADC using SAR and Single-Slope with Error Correction for CMOS Image Sensors
T. L. Li, S. Sakai, S. Kawada, Y. Goda, S. Wakashima, R. Kuroda and S. Sugawa, Tohoku Univ. (Japan)

15:00 J-1-5
A Programmable Difference-of-Gaussian Analog CMOS Image sensor Operating in the Subthreshold Regime
Z. Wang and T. Shibata, the Univ. of Tokyo (Japan)

J-2: CMOS- MEMS Modeling & Biomedical Applications (Area 5&11)
(15:40-17:30)
Chairs: Y. Mita (Univ. of Tokyo)
K. Ajito (NTT)

15:40 J-2-1 (Invited)
Modeling and Simulation of CMOS Integrated MEMS: Application to Low-cost Sensors
F. Mailly, L. Latorre and P. Nouet, Laboratoire d'Informatique, de Robotique et de Microelectronique de Montpellier, LIRMM, Univ. Montpellier 2/ CNRS (France)

2F K

K-2: Future Interconnects (1) (Area 2)
(15:40-17:10)
Chairs: S. Ogawa (AIST)
M. Kodera (Toshiba)

15:40 K-2-1 (Invited)
Chemical Soldering: New Method for Single Molecular Interconnects
Y. Okawa[1] and M. Aono[2], [1]International Center for Materials Nanoarchitectonics (WPI-MANA) and [2]National Inst. for Materials Science (NIMS) (Japan)

5F 554

L-1: Si Power Devices (Area 14)

14:15 L-1-3
Triggering Mechanism for Neutron Induced Single Event Burnout in Power Diode
T. Shoji[1], S. Nishida[2] and K. Hamada[2], [1]Toyota Central R&D Labs., Inc and [2]Toyota Motor Corporation (Japan)

14:30 L-1-4
Effects of Trap Energy Levels on Reverse Recovery Surge of Silicon Power Diode
S. Machida[1], Y. Yamashita[1], T. Misumi[2] and T. Sugimaya[1], [1]Toyota Central R&D Labs. Inc. and [2]Toyota Motor Corp. (Japan)

14:45 L-1-5
Compact Modeling of Floating-Base Effect in IGBT Based on Potential Modification by Accumulated Charge
T. Yamamoto[1], M. Miyake[2] and M. Miura Mattaush[2], [1]DENSO Corp. and [2]Hiroshima Univ. (Japan)

15:00 L-1-6
Super Junction Power MOSFET by Multi step Trench Process
J. M. Wang[1], K. Y. Tai[1], L. C. Wang[1], C. H. Huang[2], C. Lin[2], C. J. Lin[1] and Y. C. King[1], [1]National Tsing-Hua Univ. and [2]Taiwan Semiconductors Company Ltd. (Taiwan)

L-2: SiC Processing and Characterization Technology (Area 14)
(15:40-17:25)
Chairs: M. Kato (Nagoya Institute of Technology)
T. Ishikawa (Toyota Central R&D Labs., Inc.)

15:40 L-2-1
X-Ray Three-Dimensional Topography Analysis of Basal-Plane Dislocations and Threading Edge Dislocations in 4H-SiC
R. Tanuma[1], D. Mori[2], I. Kamata[1] and H. Tsuchida[1], [1]Central Res. Inst. Electric Power Indus. (CRIEPI) and [2]Fuji Electric Co., Ltd. (Japan)

5F 555

M-1: OTFT(1):Fabrication and Novel Structures (Area 10)

14:15 M-1-3
Fabrications of Low Threshold Voltage Organic Thin Film Transistor by Using Inkjet-Printed Hybrid Gate Dielectrics
C. T. Liu and W. H. Lee, Dept. of Electrical Engineering, National Cheng Kung Univ. (Taiwan)

14:30 M-1-4
Laminated Sheet Organic Field-Effect Transistors Fabricated by Thermal Press Methods
M. Sakai[1], A. Inoue[1], T. Okamoto[1], Y. Yamazaki[1], H. Yamauchi[1], S. Kuniyoshi[1], M. Nakamura[2], K. Kudo[1], T. Watanabe[1], S. Unno[1] and N. Hu[1], [1]Chiba Univ. and [2]NAIST (Japan)

14:45 M-1-5
Using Self-Assemble-Monolayer on Nanopore Sidewalls to Fabricate Vertical Poly-mer Transistors with High Output Current
H. W. Zan[1], Y. H. Hsu[1], H. F Meng[1], C. H. Huang[1], Y. T. Tao[2] and W. W. Tsai[2], [1]National Chiao Tung Univ. and [2]Academia Sinica (Taiwan)

15:00 M-1-6
Dinaphtho Thieno Thiophene Thin-Film Transistors with Modified Platinum Electrodes in Bottom-Contact Configuration
M. Kitamura[1,2], Y. Tanaka[1], W. Kang[2] and Y. Arakawa[2], [1]Kobe Univ. and [2]Univ. of Tokyo (Japan)

M-2: OTFT(2): Materials and Characterization (Area 10)
(15:40-17:25)
Chairs: K. Fujita (Kyushu Univ.)
T. Manaka (Tokyo Institute of Technology)

15:40 M-2-1 (Invited)
Recent Development of New Organic Semiconductors for Thin-film Transistor Applications
K. Takimiya[1,2], I. Osaka[1] and E. Miyazaki[1], [1]Hiroshima Univ. and [2]RIKEN Advanced Science Inst., (Japan)

Coffee Break

Tuesday, September 25

2F B-1

A-2: Silicon Photonics (2): Fabrication & Materials (Area 7)

15:55 A-2-2
Low-loss Si waveguides with Variable-Shaped-Beam EB Lithography for Large-scaled Photonic Circuits
N. Hirayama[1,2], H.Takahashi[1,3], Y.Noguchi[1,2], M.Yamagishi[1,2] and T.Horikawa[1,2], [1]Inst. for Photonics-Electronics Convergence System Tech., [2]National Inst.of Advanced Industrial Science and Tech. and [3]Photonics Electronics Tech. Res. Association (Japan)

16:10 A-2-3
Characterization of Electroluminescence from One-dimensionally Self-Aligned Si-based Quantum Dots
H. Takami[1], K. Makihara[1], M. Ikeda[2] and S. Miyazaki[1], [1]Univ. of Nagoya and [2]Univ. of Hiroshima (Japan)

16:25 A-2-4
Design of Silicon Photonic Crystal Waveguides for High Gain Raman Amplification Using Two Symmetric TE-Like Slow-Light Modes
Y. H. Hsiao, S. Iwamoto and Y. Arakawa, Univ. of Tokyo (Japan)

16:40 A-2-5
Mixture formaion of $ErxYb_2$-xSi_2O_7 and $ErxYb_2$-xO_3 for broadening the C - band in an optical amplifier on Si
H. Omi[1,2], Y. Abe[1], M. Anagnosti[1] and T. Tawara[1,2], [1]NTT Basic Research Labs., NTT Corp. and [2]Nanophotonics Center, NTT Corp. (Japan)

16:55 A-2-6
Fabrication of Er silicate crystalline waveguide by directed self-assembly approach using radical assisted sputtering
T. Nakajima[1], T. Shinagawa[1], T. Kimura[1], H. Isshiki[1], T. Sugawara[2] and Y. Jiang[2], [1]Univ. of Electro-Communications and [2]Shincron Co. Ltd. (Japan)

17:10 A-2-7
Theoretical analysis method of vertical coupling optical I/O interface with mirrors
M. Nara, T. Kita, Y. Tanushi and H. Yamada, Tohoku Univ. (Japan)

2F B-2

B-2: Flash Memory (Area 4)

16:00 B-2-2
Characterization RTN(Random Telegraph Noise) Generated by Process and Cycling Stress Induced Traps in 26nm NAND Flash Memory
B. S. Jo[1], H. J. Kang[1], S. M. Joe[1], M. K. Jeong[1], S. K. Park[2], K. R. Han[2], B. G. Park[1] and J. H. Lee[1], [1]Seoul National Univ. and [2]SK Hynix Inc. (Korea)

16:20 B-2-3
Single-Poly Flash Memory with Degradation-Separated Scheme
H. W. H, Ching, W. Robert, Y. Kevin, L. Yen Hsin, B. Francis, C. Hsin Ming and Y. Evans, eMemory Tech. Inc. (Taiwan)

16:40 B-2-4
A Ultra-low-voltage operation on Ultra-thin poly-Si p-channel Flash Memory with Silicon Nanocrystals
H. B. Chen[1], S. H. Lin[2], J. J. Wu[1], Y. C. Wu[2] and C. Y. Chang[1], [1]Univ. of National Chiao Tung Univ. and [2]Univ. of National Tsing Hua Univ. (Taiwan)

17:00 B-2-5 (Late News)
Exploring Trapped Charge Evolution in P-Channel SONOS Memory Device
F. H. Li[1], Y. Y. Chiu[1], Y. H. Lee[1], R. W. Chang[1], B. J. Yang[1], W. T. Sun[2], E. Lee[2], C. W. Kuo[2] and R. Shirota[1], [1]National Chiao Tung Univ. and [2]eMemory Tech. Inc. (Taiwan)

1F C-1

C-2: Nanowire Growth and Characterization (Area 13)

16:10 C-2-2
InAsP-InAs-InAsP hetero-nanowires grown via the self-assisted vapor-liquid-solid mode
G. Zhang, K. Tateno, H. Gotoh and T. Sogawa, NTT Basic Res. Labs. (Japan)

16:25 C-2-3
Control of Diameter and Pitch of InGaAs Nanowire Arrays in Selective-area Metalorganic Vapor Phase Epitaxy
Y. Kohashi[1], S. Sakita[1,2], S. Hara[1,2] and J. Motohisa[1], [1]Graduate School of Info. Sci. and Tech., Hokkaido Univ. and [2]Res. Center for Integrated Quantum Electronics, Hokkaido Univ. (Japan)

16:40 C-2-4
Tuning the electro-optical properties of nanowires by applying uniaxial and ultrahigh strain
A. Lugstein[1], J. Greil[1], C. Zeiner[1], J. Stangl[2], M. Keplinger[2], R. Grifone[2], D. Kriegner[2], C. Somaschini[3], L. Geelhaar[3] and E. Bertagnolli[1], [1]Vienna Univ. of Tech., Inst. for Solid State Electronics, [2]Johannes Kepler Univ. Linz, Inst. of Semiconductor and Solid State Physics and [3]Paul-Drude-Inst. for Solid State Electronics (Austria)

16:55 C-2-5
Growth and Characterization of AlGaAs Nanowires on Insulateing Al_2O_3 Layers by Selective-Area Metal-Organic Vapor Phase Epitaxy
S. Sakita, M. Yatago and S. Hara, Hokkaido Univ. (Japan)

1F C-2

D-2: Characterization in Gate Stack (1) (Area 1)

16:10 D-2-2
Analysis of Channel Stress Induced by NiPt-silicide and Its Generation Mechanism
M. Mizuo[1], T. Yamaguchi[2], S. Kudo[2], Y. Hirose[1,2], H. Kimura[2], J. Tsuchimoto[2] and N. Hattori[2], [1]Renesas Semiconductor Engineering Corp. and [2]Renesas Electronics Corp. (Japan)

16:30 D-2-3
Band-offset Determination at Ge/GeO_2 Interface by Internal Photoemission and Charge-corrected X-ray Photo-electron Spectroscopies
W. F. Zhang[1,2], T. Nishimula[1,2], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)

16:50 D-2-4
Characterization of phosphorus-implanted n+/p Ge junctions by reversely biased leakage current and Raman spectroscopy
C. H. Lee[1,2], T. Tabata[1,2], T. Nishimura[1,2], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]The Univ. of Tokyo and [2]JST-CREST (Japan)

1F D

E-2: Fin FET (Area 3)

16:10 E-2-2
Investigation and Comparison of Work Function Variation for FinFET and Ultra-Thin-Body SOI Devices Using a Voronoi Approach
S. H. Chao, M. L. Fan and P. Su, Univ. of National Chiao Tung (Taiwan)

16:30 E-2-3
Impact of Junction Non-abruptness on Random Discrete Dopant Induced Variability in Intrinsic Channel Tri-gate MOSFETs
K. L. Wei, X. Y. Liu and G. Du, Peking Univ. (China)

16:50 E-2-4
2D and 3D Fully-Depleted Extension-less Devices for Advanced Logic and Memory Applications
A. Veloso, A. De Keersgieter, M. Aoulaiche, M. Jurczak, A. Thean and N. Horiguchi, IMEC (Belgium)

17:10 E-2-5 (Late News)
The impact of Side Surface Roughness on Carrier Mobility in Tri-Gate Silicon Nanowire MOSFETs
K. Mao, T. Saraya and T. Hiramoto, Univ. of Tokyo (Japan)

1F E

F-2: High Frequency GaN Devices (Area 6)

16:10 F-2-2
A 0.25 μm Gate AlGaN/GaN HEMT for X-band Using RELACS Process
H. Koyama, Y. Kamo, S. Miwa, Y. Yamamoto, K. Onoe, A. Inoue and Y. Hirano, Mitsubishi Electric Corp., High Frequency & Optical Device Works (Japan)

16:25 F-2-3
Characteristics of InAlN/GaN Heterostructures Fabricated by Regrowth Technique
M. Hiroki[1,2], N. Watanabe[1], N. Maeda[1], H. Yokoyama[1], K. Kumakura[2] and H. Yamamoto[2], [1]Photonics Labs., NTT Corporation and [2]Basic Research Labs., NTT Corporation (Japan)

16:40 F-2-4
Improved effective channel electron velocity in AlGaN/GaN HEMTs with sub-100 nm gate-to-drain distance
K. Kodama, Y. Naito, H. Tokuda and M. Kuzuhara, Univ. of Fukui (Japan)

16:55 F-2-5
Suppression of off-state drain leakage current in AlGaN channel high electron mobility transistors on SiC substrate
T. Nanjo, Y. Suzuki, A. Imai, H. Okazaki, M. Suita, Y. Abe, E. Yagyu and H. Ohji, Mitsubishi electric Corp. (Japan)

17:10 F-2-6 (Late News)
High Performance Normally Off Nanochannel Al_2O_3/GaN FinFET
K. S. Im[1], K. W. Kim[1], D. S. Kim[1], H. S. Kang[1], Y. W. Jo[1], R. H. Kim[1], C. H. Won[1], K. I. Jang[1], M. K. Kwon[1], S. M. Jeon[1], D. H. Son[1], Y. M. Kwon[1] and J. H. Lee[2], [1]Kyungpook National Univ. and [2]Samsung LED Corp. Ltd. (Korea)

Banquet/Young ReseacherAward (1F, Swan & Garden, Kyoto International Conference Center)

Tuesday, September 25

1F G	1F H	2F I	2F J	2F K	5F 554	5F 555
G-2: Single Electron Devices (Area 9)	**H-2: Crystalline Silicon Solar Cells (Area 15)**	**I-2: Growth and Characterization of Group IV Related Materials (Area 8)**	**J-2: CMOS- MEMS Modeling & Biomedical Applications (Area 5&11)**	**K-2: Future Interconnects (1) (Area 2)**	**L-2: SiC Processing and Characterization Technology (Area 14)**	**M-2: OTFT(2): Materials and Characterization (Area 10)**
15:55 G-2-2 **Placement of Single Ge Quantum Dot along with Self-aligned Electrodes for Effective Single Hole Tunneling** *I. H. Chen, K. H. Chen, M. T. Kuo and P. W. Li, National Central Univ. (Taiwan)*	**16:10 H-2-2** **Single Crystalline Silicon Substrate Lift-off Using Electrodeposition Process** *Y. Kwon, S. Jin, S. Yoon and B. Yoo, Hanyang Univ. (Korea)*	**15:55 I-2-2** **Impact of Sn Corporation on Epitaxial Growth of Ge Layers on Si(110) Substrates** *S. Kidowaki, T. Asano, Y. Shimura, N. Taoka, O. Nakatsuka and S. Zaima, Graduate School of Eng., Nagoya Univ. (Japan)*	**16:10 J-2-2** **A CMOS-MEMS Design Technique based on an Electrical Circuit Simulator with Hardware Description Language** *T. Konishi[1], S. Maruyama[2], M. Mita[3], D. Yamane[4], H. Ito[4], K. Machida[1,4], N. Ishihara[4], K. Masu[4], H. Fujita[2] and H. Toshiyoshi[2], [1]NTT Advanced Tech. Corp., [2]Univ. of Tokyo, [3]JAXA and [4]Tokyo Tech (Japan)*	**16:10 K-2-2** **Growth of Dense Vertical and Horizontal Graphene for Thermal Vias and its Thermal Property** *A. Kawabata, T. Murakami, M. Nihei and N. Yokoyama, AIST (Japan)*	**15:55 L-2-2** **Evolution of Threading Edge Dislocation During Solution Growth of SiC** *S. Harada, Y. Yamamoto, K. Seki, A. Horio, T. Mitsuhashi and T. Ujihara, Nagoya Univ. (Japan)*	**16:10 M-2-2** **Influence of the First-layered Grain Size on Bias-stress Effect in Pentacene-based Thin Film Transistors** *Y. W. Zhang[1,2], D. X. Li[1] and C. Jiang[1], [1]National Center for Nanosci. and Tech. and [2]Graduate School of Chinese Academy of Sci. (China)*
16:10 G-2-3 **Integration of 1-bit CMOS Address Decoders and Single-Electron Transistors Operating at Room Temperature** *R. Suzuki, M. Nozue, T. Saraya and T. Hiramoto, Univ. of Tokyo (Japan)*	**16:25 H-2-3** **Monocrystalline Si Sorlar Cells with Selective Emitter Structure Formed by Ion Shower Doping Technique** *H. Hashiguchi[1], T. Tachibana[1], M. Aoki[2], T. Kojima[2], Y. Ohshita[2] and A. Ogura[1], [1]Meiji Univ. and [2]Toyota Tech. Inst. (Japan)*	**16:10 I-2-3** **Temperature Dependent Al-Induced Crystallization of Amorphous Ge Thin Films on Glass Substrates** *K. Toko[1], M. Kurosawa[2], N. Fukata[3], N. Saitoh[4], N. Yoshizawa[4], N. Usami[5], M. Miyao[2] and T. Suemasu[1], [1]Univ. of Tsukuba, [2]Kyusyu Univ., [3]National Inst. for Materials Science, [4]National Inst. of Advanced Industrial Science and Tech. and [5]Tohoku Univ. (Japan)*	**16:30 J-2-3** **A CMOS-Based Implantable Imaging Device for Wide-Area Brain Functional Imaging** *M. Haruta[1], T. Kobayashi[1,2], C. Kitsumoto[1], T. Noda[1,2], K. Sasagawa[1,2], T. Tokuda[1,2] and J. Ohta[1,2], [1]Nara Inst. of Science and Tech. and [2]JST-CREST (Japan)*	**16:30 K-2-3** **Annealing Condition Optimization of Sputtered Amorphous Carbon for Large-grain, Multi-layer Graphene** *M. Sato[1], H. Nakano[1], M. Takahashi[1], T. Muro[2], Y. Takakuwa[3], S. Sato[1], M. Nihei[1] and N. Yokoyama[1], [1]AIST/GNC, [2]JASRI/SPring-8 and [3]Tohoku Univ. (Japan)*	**16:10 L-2-3** **Point Defect Reduction and Carrier Lifetime Improvement of Si- and C-face 4H-SiC Epilayers** *T. Miyazawa and H. Tsuchida, Central Res. Inst. of Electric Power Industry (Japan)*	**16:25 M-2-3** **DC Bias-Stress Effect for Organic Thin-Film Transistors with Parylene-C Dielectric Layers** *K. Fukuda, T. Suzuki, D. Kumaki and S. Tokito, Yamagata Univ. (Japan)*
16:25 G-2-4 **Photoexcited-Electron Trapping by Individual Donor in Lateral Nanowire pn Junction** *S. Purwiyanti, A. Udhiarto, D. Moraru, T. Mizuno and M. Tabe, Shizuoka Univ. (Japan)*	**16:40 H-2-4** **Adoption of 2D-nanorod Arrays with Slanted ITO Film to Enhance Optical Asorption for Photovoltaic Applications** *Y. C. Yao, L. W. She, C. M. Cheng, Y. C. Chen and Y. J. Lee, National Taiwan Normal Univ. (Taiwan)*	**16:25 I-2-4** **Leading Wave Crystallization from Fast Moving Molten Zone Formed by Micro-Thermal-Plasma-Jet Irradiation to Amorphous Silicon Films** *S. Hayashi, Y. Fujita, T. Kamikura, K. Sakaike, M. Ikeda, H. Hanafusa and S. Higashi, Hiroshima Univ. (Japan)*	**16:50 J-2-4** **A 36-channel Neural Recoding Chip for Brain Machine Interface** *T. Yoshida[1], H. Ando[2], M. Ono[3], Y. Murasaka[3], A. Iwata[3], T. Suzuki[2], K. Matsushita[4] and M. Hirata[4], [1]Hiroshima Univ., [2]National Inst. of Info. and Communications Tech., [3]A-R-Tec Corp. and [4]Osaka Univ. (Japan)*	**16:50 K-2-4** **Integrating Carbon Nanotubes as Vias in a Monolithic 3DIC Process** *S. Vollebregt[1], R. Ishihara[1], A.N. Chiaramonti[2], J.[1] and C. I. M. Beenakker[1], [1]Delft Univ. of Tech. and [2]National Inst. of Standards and Tech. (The Netherlands)*	**16:25 L-2-4** **Suppression of Al Memory Effect on Growing 4H-SiC Epilayers by Hot-wall Chemical Vapor Deposition** *S.Y. Ji[1], K. Kojima[1], Y. Ishida[1], S. Yoshida[1], H. Tsuchida[2] and H. Okumura[1], [1]National Inst. of Adv. Ind. Sci. and Tech. and [2]Central Res. Inst. of Electric Power Indust. (Japan)*	**16:40 M-2-4** **Mobility Limiting Factors in Pentacene Thin-Film Transistors: Influence of the Film Growth Rate** *R. Matsubara[1], T. Nomura[2], M. Sakai[2], K. Kudo[2] and M. Nakamura[1], [1]Nara Inst. of Science and Tech. and [2]Chiba Univ. (Japan)*
16:40 G-2-5 **Dual Function of Charge Sensor: Charge Sensing and Gating** *T. Kambara[1], T. Kodera[1,2,3] and S. Oda[1,2], [1]Toyko Tech. of Tech., [2]Univ. of Tokyo and [3]PRESTO-JST (Japan)*	**16:55 H-2-5 (Late News)** **Post-Annealing Effects on Characteristics of Crystalline Germanium Solar Cells with the Double Heterostructure** *T. Kaneko and M. Kondo, National Inst. of Advanced Indus. Sci. and Tech. (Japan)*	**16:40 I-2-5** **Low-temperature Crystallization of a-Si, a-Ge and a-Si. A-Ge and a-$Si_{1-x}Ge_x$ Films by Soft X-ray Irradiation** *A. Heya[1], S. Kino[1], N. Matsuo[1], K. Kanda[2], S. Miyamoto[2], S. Amano[2], T. Mochizuki[2], K. Toko[3], T. Sadoh[3] and M. Miyao[3], [1]Univ. of Hyogo, [2]LASTI and [3]Kyushu Univ. (Japan)*	**17:10 J-2-5** **A 37x37 Pixels Photoreceptor Chip with Switchable Photosensitivity Circuit for 3-D Stacked Retinal Prosthesis Chip** *H. Naganuma[1], T. Tani[1], K. Kiyoyama[1,2] and T. Tanaka[1], [1]Tohoku Univ. and [2]Nagasaki Inst. of Applied Sci. (Japan)*		**16:40 L-2-5** **Phosphorus Doping of 4H-SiC by KrF Excimer Laser Irradiation in Phosphoric Solution** *A. Ikeda, K. Nishi, H. Ikenoue and T. Asano, Kyushu Univ. (Japan)*	**16:55 M-2-5** **Limiting Factor Analysis of Device Operation of Organic Thin Film Transistors by Field-Induced Electron Spin Resonance** *H. Matsui[1], D. Kumaki[2], E. Takahashi[1,3], M. Ikawa[1], I. Osaka[4], T. Abe[4], K. Takimiya[4], S. Tokito[2] and T. Hasegawa[1], [1]FLEC, AIST, [2]ROEL, Yamagata Univ., [3]SCAS and [4]Hiroshima Univ. (Japan)*
16:55 G-2-6 **Observation of Charging and Discharging Effects of Dopant Atoms in Nanoscale Lateral pn Junction by Kelvin Probe Force Microscope** *R. Nowak[1,2], M. Anwar[1], D. Moraru[1], T. Mizuno[1], R. Jablonski[2] and M. Tabe[1], [1]Shizuoka Univ. and [2]Warsaw Univ. of Tech. (Japan)*		**16:55 I-2-6** **Intrinsic Bonding Defects in Non-crystalline (nc-) SiO_2 and GeO_2: Spectroscopic Detection of Differences between Vacancy Sites with and without O-atom occupancy** *G. Lucovsky, D. Zeller, K. Wu, B. Papas and J. L. Whitten, NC State Univ. (USA)*			**16:55 L-2-6** **Leakage Current Suppression Using Passivation of Defect by Anodic Oxidation for 4H-SiC Schottky Contacts** *M. Kato, M. Kimura and M. Ichimura, Nagoya Inst. of Tech. (Japan)*	**17:10 M-2-6** **Gas Sensor Integrate with a Vertical Polymer Space-Charge-Limited Transistor** *H. W. Zan, C. H. Li, C. K. Yu and H. F. Meng, National Chiao Tung Univ. (Taiwan)*
		17:10 I-2-7 **Scaling of Channel Length for Highly Conductive Silicon Nanocrystal Films** *J. F. Susoma, Y. Nakamine, K. Usami, T. Kodera, Y. Kawano and S. Oda, Toyko Tech. of Tech. (Japan)*			**17:10 L-2-7** **Transistor Characteristics of Lateral MOSFETs with a Thin 3C-SiC Layer on an Insulator** *H. Uchida, A. Minami, T. Sakata, H. Nagasawa and M. Kobayashi, HOYA Corp. (Japan)*	

Banquet/Young ReseacherAward (1F, Swan & Garden, Kyoto International Conference Center)