2011 International Conference on Solid State Devices and Materials / 2011 International School on Tokai Region Nanotechnology Manufacturing Cluster

=Short Course (1)=

Materials and Processing for Adavaced CMOS -From Fundamentals to State-of-the-Art

September 27, 2011, Nagoya University.

Organizers
Seiichi Miyazaki (Nagoya University)

This short course is aimed at graduated students and young researchers from both industry and academia, and world's leading experts in the field of Silicon technology will lecture on fundamental aspect and knowledge about material processing and device technologies for Si CMOS devices including the overview of technological issues and challenges in the past, today and the future. All lectures will be done in English, and all participants at SSDM 2011 are welcome.

Plenary Lecture

10:00 Prof. Mitsumasa Koyanagi , Tohoku University , New Industry Creation Hatchery Center
"3D Integration Technology and New Application"

Three-dimensional (3-D) integration technologies are discussed focusing on key technologies such as through-silicon via (TSV), metal microbump, wafer thinning, wafer bonding, wafer alignment and so forth. In addition, a new 3-D integration technology and heterogeneous integration technology based on a reconfigured wafer-to-wafer bonding method called a super-chip integration is described. A number of known good dies (KGDs) with different sizes and different devices are simultaneously aligned and bonded onto lower chips or wafer by a chip self-assembly method using the surface tension of liquid in the super-chip integration. Influences of 3D chip stacking and wafer stacking on device characteristic and reliability are also discussed referring to mechanical stress and Cu contamination induced by Cu-TSVs and metal microbumps. Furtheremore, possibilities for new system-on-a chip and heterogeneous LSIs by 3D integration and super-chip integration such as 3D stacked multicore processor using new shared memory with reconfigurable memory address, 3D stacked dependable processor with self-test and self-repair function, GPU stacked 3D image sensor with extremely fast processing speed, ultra-low power 3D green LSI with energy scavenger devices operated by reusable energy, 3D brain-machine interface (BMI) devices etc. are discussed.

Speakers

12:30 Prof. Byoung Hun Lee, Gwangju Institute of Science and Technology
"Review on Advanced Gate Stack Technology"

Metal gate and high-k gate dielectric has been implemented in recent logic technology, replacing conventional polysilicon gate and SiO2 based gate dielectric. However, the paths to the implementation were divided into gate first and gate last integration scheme. This lecture will review the history of gate stack development to explain the technical bases for two different integration schemes and their merits and demerits. Also, further discussion on future development path will be included using recent results reported in the literatures.

13:15 Prof. Shinichi Takagi, The University of Tokyo

"Channel Engineering for Advanced CMOS Devices"

MOS channel engineering is indispensable in overcoming difficulties of advanced CMOS, caused by physical and essential limitations of scaled Si MOSFETs. Particularly, MOSFETs using the carrier-transport-enhanced channels featuring high mobility and low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage. From this viewpoint, attentions have recently been paid to introduction of strain and new channel materials into MOS channels. In this short course presentation, motivation to the channel engineering, effect of stress on device performance, evolution of stress engineering and prospective/critical issues of MOS technologies using new channel materials such as SiGe, Ge and III-V will be addressed.

14:00 Dr. Tetsuya Tatsumi, Sony Corporation

"Control of plasma-surface reactions for next generation semiconductor devices"

Dry etching technologies for various devices have been continuously improved for over 30 years as the most advanced application of the low temperature plasmas. In this presentation, a brief history of the development of dry etching systems, current issues, and the future technologies for the quantitative control of atomic layer reactions will be discussed.

14:45 Break

15:00 Dr. Shinji Okazaki, EUVA/Gigaphoton INC.

"Advanced Lithography"

The development of ULSI devices has been promoted by the evolution of lithography. More than 40 years ago, the minimum feature size of the IC was 5 to 10 microns. At that time we had been using optical lithography. Various lithography named NGL(Next Generation Lithography) were developed and tried to replace the optical way but all attempts were failed. In these 40 years, the exposure wavelength of optical lithography was reduced from 436nm (g-line of mercury lamp) to 193nm (ArF excimer laser light). But the reduction of exposure wavelength could not solely realize such miniaturization. So various resolution enhancement technologies were proposed and utilized. Such resolution enhancement tricks and techniques will be shown and the limitations of these technologies will be discussed. According to such efforts to delineate smaller patterns by optical way, we are still using optical lithography for the delineation of 30 nanometers and below. However, it is very difficult to delineate such small patterns by this wavelength. We are trying to use every possible tricks and ideas for the delineation of such smaller patterns. Also we are still developing NGLs for the future use. The future technology will also be discussed in the lecture.

15:45 Prof. Toshiro Hiramoto, University of Tokyo

“Random Variability in Scaled MOS Transistors”

The variability is one of the most significant technological barriers for further device scaling and lowering supply voltage. It is known that in conventional bulk MOSFETs, the main origin of random Vth variability is random dopant fluctuation (RDF) in the channel. In this presentation, it will be shown that RDF also causes DIBL (drain-induced barrier lowering) and COV (current-onset voltage) variability that leads to drain-current variability and SRAM instability. It will be also shown that the elimination of dopants from the channel is one of the solutions, and the variability of Vth, DIBL, and COV in intrinsic channel fully-depleted (FD) SOI MOSFETs will be discussed.