POSTER SESSION (13:30-15:00, 6F Exhibition Hall)

Area 1: Advanced LSI Processing & Materials Science (20 Papers)

P-1-1
High Quality Germanium Dioxide Formation using Damage-Free and Low-Temperature Neutral Beam Oxidation Process
A. Wada[1], K. Endo[2], M. Masahara[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)

P-1-2
Passivation of Ge(100) and (111) Surfaces by Termination of Nonmetal Elements
D. H. Lee, K. Kubo, T. Kanashima and M. Okuyama, Osaka Univ. (Japan)

P-1-3
First-Principles Study on Interface Properties of GeO_2/Ge System
S. Saito and T. Ono, Osaka Univ. (Japan)

P-1-4
Evaluation of Thermally-Grown Ge Oxide on Ge(100) and Ge(111) Surfaces
S. K. Sahari[1], A. Ohta[1], M. Matsui[1], H. Murakami[1], S. Higashi[1] and S. Miyazaki[2], [1]Hiroshima Univ. and [2]Nagoya Univ. (Japan)

P-1-5
Control of Defect Properties in Ge Heteroepitaxial Layers by Sn Incorporation and H_2-Annealing
M. Adachi, Y. Shimura, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)

P-1-6
Formation of Ohmic Contacts with Shallow NiGe/n^+ Ge Junction
M. Miura[1,2], M. Noguchi[1,2], J. Fujikata[1,2], T. Horikawa[1,3], M. Takahashi[1,3], Y. Noguchi[1,3] and Y. Arakawa[1,4], [1]PECST, [2]PETRA, [3]AIST and [4]Univ. of Tokyo (Japan)

P-1-7
Estimation of breakdown electric-field strength reflecting local structures of SiO_2 by using first-principles molecular orbital calculation technique
H. Seki[1], Y. Shibuya[2], D. Kobayashi[3], H. Nohira[2], K. Yasuoka[1] and K. Hirose[3], [1]Keio Univ., [2]Tokyo City Univ. and [3]ISAS/JAXA (Japan)

P-1-8
Clear Difference between Chemical Structure of SiO_2/Si Interface Formed Using Oxygen Radicals and That Formed Using Oxygen Molecules
T. Suwa[1], Y. Kumagai[1], A. Teramoto[1], T. Muro[2], T. Kinoshita[2], S. Sugawa[1], T. Hattori[1] and T. Ohmi[1], [1]Tohoku Univ. and [2]Japan Synchrotron Radiation Res. Inst. (Japan)

P-1-9
Thermal Stability of Single and Alloy Noble Metals as for PMOS Gate Electrode
C. Choi[1], J. Ahn[1] and R. Choi[2], [1]Hanyang Univ. and [2]Inha Univ. (Korea)

P-1-10
Analysis of Raman Spectra from Offset Spacer Region of Si-MOSFET Structure using Simulated Stress Tensor and Absorbed Light Intensity by FDTD Simulation
A. Satoh[1], T. Tada[1], V. Poborchii[1], T. Kanayama[1], S. Satoh[2] and H. Arimoto[1], [1]AIST and [2]Fujitsu Semiconductor Ltd. (Japan)

P-1-11
Chemical Bonding States of As in Si Shallow Junctions Detected by Soft X-ray Photoelectron Spectroscopy and their Profiles
J. Kanehara[1], Y. Miyata[1], H. Nohira[2], Y. Izumi[3], T. Muro[3], T. Kinoshita[3], P. Ahmet[1], K. Kakushima[1], K. Tsutsui[1], T. Hattori[1] and H. Iwai[1], [1]Tokyo Tech, [2]Tokyo City Univ. and [3]JASRI/SPring-8 (Japan)

P-1-12
Comprehensive Understanding of Flatband Voltage Shift Based on Energy Band Alignment of the Whole Metal/high-k/SiO_2/Si Stack
X. Wang[1], W. Wang[1], K. Han[1], J. Zhang[2], X. Ma[1], J. Xiang[1], D. Chen[1] and T. Ye[1], [1]Chinese Academy of Sci. and [2]North China Univ.of Tech. (China)

P-1-13
Lateral Large-Grained Low-Temperature Polycrystalline Silicon-Germanium Thin-Film Transistors on Glass Substrate
Y. Okabe[1], K. Kondo[1], J. Suzuki[2], K. Kitahara[2] and A. Hara[1], [1]Tohoku Gakuin Univ. and [2]Shimane Univ. (Japan)

P-1-14
Enhanced Sidewall Growth (ESG) process: towards PEALD with conformality above 100%
S. Ueda, A. Fukazawa, H. Fukuda and N. Kobayashi, ASM Japan K.K. (Japan)

P-1-15
Mean time to failure distribution in thin oxide film: Observation at nano and devices scale and modelling using a filamentary growth model
P. Delcroix[1,2], S. Blonkowski[1], M. Kogelschatz[2] and M. Rafik[1], [1]STMicroelectronics and [2]CNRS (France)

P-1-16
Electrical Characteristics of Back Gated FET on a Wrinkle Free Graphene Channel
C. H. Cho, S. K. Lim, C. G. Kang, Y. G. Lee, H. J. Hwang, E. Park and B. H. Lee, Gwangju Inst. of Sci. and Tech. (Korea)

P-1-17
Novel activation method of B by soft X-ray undulator
T. Fukuoka[1], A. Heya[1], N. Matsuo[1], K. Kanda[1] and T. Noguchi[2], [1]Univ. of Hyogo and [2]Univ. of the Ryukyus (Japan)

P-1-18
Impact of Zirconia addition for ALD Hafina in HKMG Device Fabricated GF vs. GL
C. K. Chiang[1,3], C. H. Wu[2], H. Y. Huang[1], J. F. Lin[3], C. L. Yang[3], J. Y. Wu[3] and S. J. Wang[1], [1]National Cheng Kung Univ., [2]Chung Hua Univ. and [3]United Microelectronics Corp. (Taiwan)

P-1-19 (Late News)
Fermi Level Depinning for Metal/Germanium Schottky Junction by CF_4 Plasma Treatment
J. R. Wu, C. Y. Hou, M. L. Wu, C. C. Lin and Y. H. Wu, National Tsing-Hua Univ. (Taiwan)

Area 2: Advanced Interconnect / Materials Technology and Characterization (18 Papers)

P-2-1
Direct wafer bonding technology of 300mm wafer
S. Hongo, K. Tanida, N. Yamaguchi and K. Takahashi, Toshiba Corp. (Japan)

P-2-2
Thinning Process Induced Surface Defects in Ultra-Thin Si Wafer
M. Murugesan[1], H. Nohira[2], C. Miyazaki[3], H. Shimamoto[3], H. Kobayashi[3], T. Fukushima[1], T. Tanaka[1] and M. Koyanagi[1], [1]Tohoku Univ., [2]Tokyo City Univ. and [3]ASET (Japan)

P-2-3
Mn_2O_3 Slurry Reuse for SiO_2 Film CMP
S. Kishii[1, 3], K. Nakamura[1], K. Hanawa[2], S. Watanabe[1], Y. Arimoto[1], S. Kurokawa[3] and T. K. Doi[3], [1]Fujitsu Labs. Ltd., [2]Showa Denko K. K. and [3]Kyushu Univ. (Japan)

P-2-4
Optimum Design of MEMS Resonator Array to Measure the Young's Modulus of Nano-Scale Thin Films for the Reliability of Semiconductor Devices
H. Yamagiwa[1], S. Ito[1], T. Namazu[1,2], T. Takeuchi[3], K. Murakami[3], Y. Kawashimo[3] and T. Takano[4], [1]Univ. of Hyogo, [2]PRESTO-JST, [3]Shinko Seiki Co. Ltd. and [4]The New Industry Research Organization (Japan)

P-2-5
A New Technique for in-Plane Poisson's Ratio Measurement of Thin Films - Cases of Single-Crystal Silicon and Aluminum Thin Films -
T. Fujii[1], T. Namazu[1,2], M. Takahashi[1], M. Tanaka[1], K. Yoshiki[1] and S. Inoue[1], [1]Univ. of Hyogo and [2]PRESTO-JST (Japan)

P-2-6
Evolution of Wafer Shape and Localized Stress of Silicon Surrounded by Through Silicon Via Patterns along Various Process Integration Steps
C. H. Lee[1], S. H. Jie[1], S. H. Son[1], J. T. Kim[1], H. W. Yoo[1], I. K. Han[1] and W. S. Yoo[2], [1]Hynix Semiconductor Inc. and [2]WaferMasters, Inc. (Korea)

P-2-7
Improvement of the BCB Adhesion on Cr/Au Metal Layer for RF Packaging Module
N. Jeon, Y. H. Oh, Y. Ryoo and K. S. Seo, Seoul National Univ. (Korea)

P-2-8
Testkey Design of Through Silicon Vias (TSVs) for Accurate De-embedding and RF Model Parameters Extraction
J. Y. Wang[1], T. K. Huang[1], Y. C. Wu[1], S. S. H. Hsu[1], Z. H. Lin[2], C. S. Lin[2], S. S. Sheu[2], T. K. Ku[2] and C. H. Lin[2], [1]National Tsing Hua Univ. and [2]ITRI (Taiwan)

P-2-9
Study of Local Charging Phenomena during SiO_2 Contact Hole Etching
T. Yagisawa[1], T. Tatsumi[2] and T. Makabe[1], [1]Keio Univ. and [2]Sony Corp. (Japan)

P-2-10
Thermal Cycling Reliability of ChipArray® Thin Core Ball Grid Array assemblies with Fast Cure and Reworkable Capillary Flow Underfill
H. Shi and T. Ueda, Waseda Univ. (Japan)

P-2-11
Selective Heating of Microbumps Using Microwave for Low Strain Heterogeneous Chip Stack Integration
L. Qiu and T. Asano, Kyushu Univ. (Japan)

P-2-12
Room temperature fabrication of silver nanowire transparent electrodes
T. Tokuno, M. Nogi, M. Karakawa, J. T. Jiu and K. Suganuma, Osaka Univ. (Japan)

P-2-13
Low-Energy Ion-Beam-Assisted Sputtering for Si Nanocrystals
C. Y. Hsiao, K. W. Su, K. T. Hung, H. T. Wu, H. J. Chen, S. W. Fu, S. H. Wu and C. F. Shih, National Cheng Kung Univ. (Taiwan)

P-2-14
Highly Accurate Lattice-Strain mapping near Interfaces of Hetero-Structures by Convergent-Beam and Nano-Beam Electron Diffraction
K. Saitoh, H. Nakahara, Y. Daikyo and N. Tanaka, Nagoya Univ. (Japan)

P-2-15
Multi-layer Graphene for High-Frequency Interconnect
H. J. Lee, E. Kim and J. W. Jung, Sejong Univ. (Korea)

P-2-16
Investigation of Electrical Properties of HfN/HfSiON Gate Stacks In-situ Formed on Si(100) and Si(110)
T. Sano and S. Ohmi, Tokyo Tech (Japan)

P-2-18 (Late News)
MIM Capacitors with High Capacitance Density and Low Quadratic Voltage Coefficient by Employing Crystalline-TiO_2/SiO_2 Stacked Dielectric
C. C. Lin, W. Y. Ou, J. R.Wu, M. L.Wu, L. L.Chen and Y. H. Wu, National Tsing Hua Univ. (Taiwan)

Area 3: CMOS Devices / Device Physics (22 Papers)

P-3-1
Impact of Aspect Ratio on the Subthreshold RTN Amplitude of Multi-Gate MOSFETs
B. K. Lu, M. L. Fan and P. Su, National Chiao Tung Univ. (Taiwan)

P-3-2
Saturation Behavior in the Generation of Interface Traps by Hot-Carrier Stress in Nanoscale MOSFETs
M. Hu, T. Yamane and T. Tsuchiya, Shimane Univ. (Japan)

P-3-3
Investigation of Temperature Dependence on DC and Low-Frequency Noise Characteristics in Uniaxial Tensile Strained nMOSFETs
S. C. Tsai[1], S. L. Wu[2], J. F. Chen[1], S. J. Chang[1], C. Y. Chang[1], P. C. Huang[1], C. Y. Wu[2], M. S. Chen[3], Y. C. Cheng[3] and O. Cheng[3], [1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]United Microelectronics Corp. (Taiwan)

P-3-5
The Effect of La_2O_3 Capping Layer Thickness on Hot Carrier Degradation of *n*-MOSFETs with High-*k*/Metal Gate Stack
D. W. Kim[1], S. H. Lee[1], C. G. Kim[1], T. K. Oh[2] and B. K. Kang[1], [1]Pohang Univ. Sci. Tech. and [2]Hynix Semiconductor Inc. (Korea)

P-3-6
Characterization of Oxide Traps in 28 nm pMOSFETs with Σ-Shaped SiGe-S/D by Utilizing Random Telegraph Noise (RTN)
B. C. Wang[1], S. L. Wu[2], S. J. Chang[1], C. T. Huang and O. Cheng, [1]National Cheng Kung Univ. and [2]Univ. of Cheng Shiu (Taiwan)

P-3-7
Hot-Carrier Effects on High-frequency Characteristics of RF LDMOS Transistors
K. M. Chen[1], Z. W. Mou[2], H. C. Kuo[2], C. S. Chiu[1], B. Y. Chen[1], W. D. Liu[1], M. Y. Chen[3], Y. C. Yang[3], K. L. Wang[3] and G. W. Huang[1, 2], [1]National Nano Device Labs., [2]National Chiao Tung Univ. and [3]United Microelectronics Corp. (Taiwan)

P-3-8
Impact of OFF-state Degradation under Dynamic Stress on Reliability of Nanoscale n-Channel Metal-Oxide-Semiconductor Field-Effect Transistors at Elevated Temperature
N. H. Lee[1], K. J. Kim[1], H. W. Kim[2] and B. K. Kang[1], [1]POSTECH and [2]Samsung Electronics Corp. Ltd. (Korea)

P-3-9
Modeling Subthreshold Current and Threshold Voltage of Fully-Depleted Double-gate Junctionless(J-less) Transistors
Z. M. Lin[1], H. C. Lin[1,2], K. M. Liu[3] and T. Y. Huang[1], [1]National Chiao Tung Univ., [2]Labs of National Nano Device and [3]National Dong Hwa Univ. (Taiwan)

P-3-10
Integration of InGaAs Nanowire Vertical Surrounding-Gate Transistors on Si
K. Tomioka[1,2], M. Yoshimura[1] and T. Fukui[1], [1]Hokkaido Univ. and [2]PREST-JST (Japan)

P-3-11
Body Channel Type Vertical MOSFET to Suppress Gate Leakage Current
T. Sasaki[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)

P-3-12
Investigation of Short-Channel Effects in Junctionless Nanowire Transistors
P. Razavi, N. Dehdashti-Akhavan, R. Yu, G. Fagas, I. Ferain and J.P. Colinge, Univ. College Cork (Ireland)

P-3-13
Stack Gate Technique for Feasible Bulk FinFETs
Y. B. Liao[1], M. H. Chiang[2], W. C. Hsu[1], Y. S. Lai[3] and H. Li[2], [1]National Cheng Kung Univ., [2]National Ilan Univ. and [3]National Nano Device Lab. (Taiwan)

P-3-14
Strain Effects on Ballistic Currents of Silicon Nanowire pFETs with Different Orientations
J. Qin, X. Liu, H. Xu, J. Zhang and G. Du, Peking Univ. (China)

P-3-16
Evidence of the universality of the hole mobility in accumulation MOS transistors
P. Gaubert, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)

P-3-17
Simulation of Electron Transport in Source and Drain Electrodes of Ultrathin Body III-V Channel MOSFETs
Y. Maegawa[1], S. Koba[1], H. Tsuchiya[1,2] and M. Ogawa[1], [1]Kobe Univ. and [2]CREST-JST (Japan)

P-3-18
Evaluation of Drain Current Fluctuations of Si MOSFETs using BSIM3-like Current Model and TCAD
A. Satoh[1], T. Tada[1], T. Kanayama[1], S. Satoh[2] and H. Arimoto[1], [1]AIST and [2]Fujitsu Semiconductor Ltd. (Japan)

P-3-20 (Late News)
Critical Parameters for Accurate Calculation of Si Nanowire MOSFET Current
K. Natori, Tokyo Tech (Japan)

P-3-21 (Late News)
Impact of Poly Depletion on Accurate Evaluation of Self-Heating Effects in SOI MOSFETs with Four-point Gate Resistance Measurement Method
N. Beppu, T. Takahashi, T. Ohashi and K. Uchida, Tokyo Tech (Japan)

P-3-22 (Late News)
Random Interface-Traps-Induced Characteristic Fluctuation in 16-nm High-k/Metal Gate CMOS Device and Digital Circuit
Y. Y. Chiu, Y. Li and H. W. Cheng, National Chiao Tung Univ. (Taiwan)

Area 4: Advanced Memory Technology

(16 Papers)

P-4-1
Pushing Scaling Limit Due to Short Channel Effects and Channel Boosting Leakage from 13nm to 8nm with SOI NAND Flash Memory Cells
K. Miyaji, C. Hung and K. Takeuchi, Univ. of Tokyo (Japan)

P-4-4
Electrical Property of DNA FET —Charge Retention Property—
S. Takagi[1], N. Matsuo[1], K. Yamana[1], A. Heya[1], T. Takada[1] and S. Yokoyama[2], [1]Univ. of Hyogo and [2]Hiroshima Univ. (Japan)

P-4-5
Areal and Structural Effect on Oxide based RRAM cell for Improving Resistive Switching Characteristics
K. C. Ryoo[1,2], J. H. Oh[1,2], S.H. Jung[1], G. T. Jeong[2], H. S. Jeong[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics. Co., Ltd. (Korea)

P-4-6
Investigation of Switching Behavior of 2-terminal Devices on VO_2
I. P. Radu[1,2], K. Martens[1], B. Govoreanu[1], S. Mertens[1], X. Shi[1], M. Cantoro[1], M. Schaekers[1], M. Jurczak[1], S. De Gendt[1,2], A. Stesmans[1,2], M. Heyns[1,2] and J. A. Kittl[1], [1]IMEC and [2]Univ. of Leuven (Belgium)

P-4-7
Evaluation of the WO_x Film Properties for ReRAM Application
Y. Y. Chen[1,2], W. C. Chien[2], M. H. Lee[2], Y. C. Chen[2], A. T. H. Chuang[2], T. J. Hong[1], S. J. Lin[1], T. B. Wu[1] and C. Y. Lu[2], [1]National Tsing Hua Univ. and [2]Macronix International Corp., Ltd. (Taiwan)

P-4-8
Characterization and improved endurance for HfO_2 resistive memory with CMP treated TiN bottom electrode
P. S. Chen[1], Y. S. Chen[2,3], H. Y. Lee[2], T. Y. Wu[2], W. H. Liu[2], P. Y. Gu[2], F. Chen[2] and M. J. Tsai[2], [1]MingShin Univ. Sci. and Eng., [2]Industrial Tech. Res. Inst. and [3]National Tsing Hua Univ. (Taiwan)

P-4-9
Study of Bipolar Multilevel Memristive Mechanism and Characterizations in a Thin FeO_x Transition Layer Device
G. Y. Wu[1], Y. F. Chang[1], L. W. Feng[1], C. Y. Chang[1] and T. C. Chang[2], [1]National Chiao Tung Univ. and [2]National Sun Yat-Sen Univ. (Taiwan)

P-4-10
Multi-Level Phase-Change Memory Cells with SiN or Ta_2O_5 Barrier Layers
A. Gyanathan and Y. C. Yeo, National Univ. of Singapore (Singapore)

P-4-11
Endurance enhancement of elevated-confined phase change random access memory
*H. X. Yang[1,2], L. P. Shi[1], H. K. Lee[1], R. Zhao[1] and T. C. Chong[3], [1]A*STAR, [2]National Univ. of Singapore and [3]Singapore Univ. of Tech. and Design (Singapore)*

P-4-12
Simulation of Retention Behavior for the Phase Change Memory
J. Chen, D. Song, G. Du, G. Lian, J. Kang and X. Liu, Peking Univ. (China)

P-4-13 (Late News)
Filament Formation by Cu and Ag Ions for Memory Applications Utilizaing Oxide Dielectrics With Pre-existing Vacated O-atom Sites
Z. Zhang[1], E. Katz[1], D. Zeller[2], G. Lucovsky[2] and L. F. Brillson[1], [1]Ohio State Univ. and [2]North Carolina State Univ. (USA)

P-4-14 (Late News)
Effect of Oxidation Amount on Gradual Switching Behavior in Reset Transition of Al/TiO_2 based Resistive Switching Memory and its Mechanism for MLC Operation
J. H. Oh[1,2], K. C. Ryoo[1,2], S. Jung[1], Y. Park[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)

P-4-15 (Late News)
Design and Optimization of Program and Restore Operations in CMOS-Compatible Nonvolatile Latch
J. G. Lee and S. Masui, Tohoku Univ. (Japan)

P-4-16 (Late News)
SET polarity dependent resistive switching memory characteristics using IrOx/GdOx/WOx/W structure
D. Jana[1], S. Maikap[1], T. C. Tien[2], H. Y. Lee[2], W. S. Chen[2], F. T. Chen[2], M. J. Kao[2] and M. J. Tsai[2], [1]Chang Gung Univ. and [2]ITRI (Taiwan)

Area 5: Advanced Circuits and Systems

(17 Papers)

P-5-1
Wireless Charge Based Capacitance Measurement Circuits with On-chip Spiral Inductor for RFID Biosensor
B. Kim[1], S. Uno[2] and K. Nakazato[1], [1]Nagoya Univ. and [2]Ritsumeikan Univ. (Japan)

P-5-2
SPICE MOSFET Analog Model Parameter Verification and Re-optimization Based on g_m/I_D Lookup Table Design Methodology
T. Konishi[1], B. Patrick[1], T. Kaho[2] and S. Masui[1], [1]Tohoku Univ. and [2]NTT Network Innovation Labs. (Japan)

P-5-3
Write Speed Evaluation of Reconfigurable Spin Logic Block with SPRAM for 3D-Stacked Reconfigurable Spin Processor
R. Nakazawa[1], H. Kino[1], K. Kiyoyama[1,2], M. Koyanagi[1] and T. Tanaka[1], [1]Tohoku Univ. and [2]Nagasaki Inst. of Applied Science (Japan)

P-5-4
Nonvolatile Low Power 16-bit/32-bit MTJ Based Binary Counter and its Scaling
S. Togashi, T. Ohsawa and T. Endoh, Tohoku Univ. (Japan)

P-5-5
Evaluation of Reconfigurable Processor Test Chip for Dependable 3D Stacked Multicore Processor
H. Hashimoto, T. Fukushima, K. W. Lee, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)

P-5-6
A High-Voltage Tolerant Interface Circuit for Embedded CMOS Non-volatile Memories
C. Y. Huang and H. Lin, National Chung Hsing Univ. (Taiwan)

P-5-7
The Integrated a-Si Gate Driver Circuit using Voltage Controlled Capacitance Modeling for HDTV/XGA
S. K. Han[1], J. Y. Kim[1], H. Choi[1], K. H. M. Choi[1], Y. S. Choi[1], K. M. Park[2] and S. Y. Choi[2], [1]LG Display Co. Ltd. and [2]Kyungpook National Univ. (Korea)

P-5-8
A Fully-Parallel Self-Learning Analog Support Vector Machine Employing Compact Gaussian-Generation Circuits
R. Zhang and T. Shibata, Univ. of Tokyo (Japan)

P-5-9
Current Compensation Circuit for Precise Nano-Ampere Current Reference
K. Isono, T. Hirose, Y. Osaki, N. Kuroki and M. Numa, Kobe Univ. (Japan)

P-5-10
A Wide-Range Tunable Level-Keeper using Vertical MOSFETs for Current-Reuse Systems
S. Tanoi[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)

P-5-11
A Reduced-Ripple PMOS Charge Pump Circuit with Small Filtering Capacitors
B. Y. Jaw and H. Lin, National Chung Hsing Univ. (Taiwan)

P-5-12
CMOS Op-amp Offset Calibration Technique Using a Closed Loop Offset Amplifier and Compact Resistor String DAC
H. Morimoto[1], H. Goto[1], H. Fujiwara[2] and K. Nakamura[1], [1]Kyushu Inst. of Tech. and [2]New Japan Radio Co. Ltd. (Japan)

P-5-13
A Twistedly-Cascaded Time Difference Amplifier for High Robustness Against Process Variation
N. Harigai, K. Niitsu, D. Oki, M. Sakurai, T. J. Yamaguchi and H. Kobayashi, Gunma Univ. (Japan)

P-5-14
An Experimental Verification of the Design Margin Analysis Method for Even-Stage Ring Oscillators with CMOS Latch
Y. Hirakawa, N. Mimura, A. Motomura and K. Nakamura, Kyushu Inst. of Tech. (Japan)

P-5-15
Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS
Q. Bu, N. Li, H. Asada, K. Okada and A. Matsuzawa, Tokyo Tech (Japan)

P-5-16
MOS Power Cells for Output Power Levels of 17 to 23 dBm
R. L. Wang[1], C. H. Liu[2], C. C. Chuang[2], C. H. Tu[3], Y. Z. Juang[3] and Y. K. Su[2], [1]National Kaohsiung Normal Univ., [2]National Cheng Kung Univ. and [3]National Chip Implementation Center (Taiwan)

P-5-17
Power Amplifier for E-band Wireless Link Using 0.1μm GaAs pHEMT
M. Kang, B. Kim, K. Kim and W. Byun, ETRI (Korea)

Area 6: Compound Semiconductor Electron Devices and Related Technologies
(12 Papers)

P-6-1
Hot Carrier Effect on RF Characteristics of High-k/Metal Gate SiGe Channel pMOSFETs
E. Y. Jeong[1], H. C. Sagong[1], D. Y. Choi[1], C. W. Sohn[1], J. S. Lee[1], C. Y. Kang[2] and Y. H. Jeong[1], [1]POSTECH and [2]SEMATECH (Korea)

P-6-2
Effect of Etch Damage on Device performance in Trench-gate and Mesa-gate GaN Vertical MOSFET
K. W. Kim[1], S. D. Jung[1], M. K. Kwon[1], R. H. Kim[1], D. S. Kim[1], K. S. Im[1], H. S. Kang[1], C. H. Won[1], K. I. Jang[1], J. H. Lee[2], K. S. Kim[2] and J. H. Lee[1], [1]Kyungpook National Univ. and [2]Samsung LED (Korea)

P-6-3
Electrical and Photo-response Properties of Titanium Contacts on n-type N-face and Ga-face GaN Layer for Vertical Power Devices Prepared by ELOG and Laser Lift-off
D. K. Kim[1], C. J. Lee[1], Y. J. Kwon[1], J. Y. Yun[1], D. S. Kim[1], H. B. Lee[2], J. H. Lee[1] and S. H. Hahm[1], [1]Kyungbook National Univ. and [2]Samsung LED (Korea)

P-6-4
Plasma-Induced Damage of GaN and Its Recovery by Atomic Hydrogens at a Room Temperature
Y. Lu[1], S. Chen[1], R. Kometani[1], K. Takeda[1], H. Kondo[1], T. Egawa[2], K. Ishikawa[1], H. Amano[1], M. Sekine[1] and M. Hori[1], [1]Nagoya Univ. and [2]Nagoya Inst. of Tech. (Japan)

P-6-5
Temperature Dependent Characteristics of Fe/n-GaN Schottky Diodes
R. Adari[1], B. Sarkar[1], T. Patil[1], D. Banerjee[1,2], P. Suggisetti[1], S. Ganguly[1] and D. Saha[1], [1]Center of Excellence in Nanoelectronics and [2]IITB-Monash Research Academy (India)

P-6-6
Air-Gap Capacitance-Voltage Analyses of InP Surfaces after Wet and Dry Processes
T. Yoshida, Shimane Univ. (Japan)

P-6-7
High-Voltage AlGaN/GaN HEMTs on Si Substrate with Implant Isolation
C. J. Yu[1], C. F. Huang[1], P. J. Chu[1], K. Y. Chen[1], S. S. H. Hsu[1], H. C. Chiu[2] and F. Zhao[3], [1]National Tsing Hua Univ., [2]Chang Gung Univ. and [3]Univ. of South Carolina (Taiwan)

P-6-8
Investigation of Plasma-Induced Damages in GaN with Different Processing
C. Y. Lee, H. Sekiguchi, H. Okada and A. Wakahara, Toyohashi Univ. of Tech. (Japan)

P-6-10
2D Device Simulation of AlGaN/GaN HFET Current Collapse Caused by Deep Levels in GaN Buffer Layer
Y. Ikawa, T. Hosokawa, Y. Kio, J. P. Ao and Y. Ohno, Univ. of Tokushima (Japan)

P-6-11
Deep levels in n-GaN Doped with Carbon Studied by Deep Level and Minority Carrier Transient Spectroscopies
U. Honda[1], Y. Yamada[1], Y. Tokuda[1] and K. Shiojima[2], [1]Aichi Inst. of Tech. and [2]Univ. of Fukui (Japan)

P-6-12 (Late News)
An Al_2O_3/InSb/Si MOS Diode Having an Ultra-Thin InSb Layer
A. Kadoda[1], T. Iwasugi[1], K. Nakatani[1], K. Nakayama[1], M. Mori[1], K. Maezawa[1], E. Miyazaki[2] and T. Mizutani[2], [1]Univ. of Toyama and [2]Nagoya Univ. (Japan)

Area 7: Photonic Devices and Optoelectronic Integration
(30 Papers)

P-7-1
GaN-based LED with embedded air voids array structure
D. S Kuo, S. J. Chang, T. K. Ko[2], W. Y. Yen[2] and S. J. Hon[2], National Cheng Kung Univ. (Taiwan)

P-7-2
Investigation of Efficiency Droop for UV-LED with N-type AlGaN Layer
Y. C. Chen[1], C. C Tu[2], J. R. Chang[1], P. M. Tu[1], S. P. Chang[1], S. S. Yen[1], Y. C. Chen[1], H. C. Kuo[1] and C. Y. Chang[1], [1]National Chiao Tung Univ. and [2]Chung Yuan Christian Univ. (Taiwan)

P-7-3
Nanoscale epitaxial lateral overgrowth of GaN-based light-emitting diodes on a SiO_2 nanorod-array patterned sapphire template
C. H. Chiu[1], C. C. Lin[1], C. H. Wang[1], S. P. Chang[1,2], C. Y. Jang[1], Z. Y. Li[1], H. C. Yang[2], H. C. Kuo[1], T. C. Lu[1] and S. C. Wang[1], [1]National Chiao Tung Univ. and [2]Epistar Co. Ltd. (Taiwan)

P-7-4
Enhanced Light Output of Vertical GaN-Based LEDs with Surface Roughening Using IZO Nano Roughened
P. R. Wang, S. J. Wang, D. M. Kuo, C. H. Kuo, H. R. Kuo, T. H. Lin and P. H. Wang, National Cheng Kung Univ. (Taiwan)

P-7-5
Elucidating the electrical characteristics of an inversion domain boundary in p-type GaN of light-emitting diodes
Y. S. Wang[1], M. C. Hsieh[1], J. F. Chen[1], J. B. Huang[2] and N. C. Chen[3], [1]National Chiao Tung Univ., [2]National Taiwan Univ. of Sci. and Tech. and [3]Chang Gung Univ. (Taiwan)

P-7-6
Deep UV Light Emitting Diodes on AlN Templates Grown by Commercialized MOCVD (‹1200℃)
M. Kurouchi, T. Takeuchi and Y. Aoyagi, Ritsumeikan Univ. (Japan)

P-7-7
An *n*-ZnO/*p*-GaN Ultraviolet Light Emitting Diode Prepared Using Radio-Frequency Magnetron Cosputtering System
N. J. Wu[1], C. P. Hsu[2], Y. J. Tsai[2], B. T. Lai[1] and D. S. Liu[1], [1]National Formosa Univ. and [2]ITRI (Taiwan)

P-7-8
Low efficiency droop of InGaN/GaN blue LEDs with super-lattice active structure
S. P. Chang[1,2], J. R. Chang[1], B. M. Tu[1], Y. C. Chen[1], K. P. Sou[1], Y. C. Hsu[1], S. S. Yen[1], Y. J. Li[1], H. C. Yang[2], T. C. Hsu[2], H. C. Kuo[1] and C. Y. Chang[1], [1]National Chiao Tung Univ. and [2]Epistar Corp. Ltd. (Taiwan)

P-7-9
Design of Optically Pumped PbS-Based Mid-Infrared Surface Emitting Lasers
Y. Sugiyama, K. Kodama, Y. Isaji, T. Yokoyama, S. Kobayashi, Y. Takano and A. Ishida, Shizuoka Univ. (Japan)

P-7-10
The Fabrication of a multiple Outputs Semiconductor Ring Laser Diode and its Output Characteristics
M. C. Shih, C. S. Chen and W. H. Lan, National Univ. of Kaohsiung (Taiwan)

P-7-12
Strudy on Structure Dependent Optical Characteristics of GaAs-related Photonic Crystal Cavities
K. Nakano, R. Nakao, H. Nagatomo, K. Kukita, K. Uwai, F. Ishikawa, M. Morifuji and M. Kondow, Osaka Univ. (Japan)

P-7-13
Enhanced localized surface plasmon resonance in a stacked structure
H. H. Chen, Y. T. Chang, C. W. Yu, S. Y. Huang, F. T. Chuang and S. C. Lee, National Taiwan Univ. (Taiwan)

P-7-14
Low-temperature Photoluminescence Characteristics of GaAs Quantum-well Waveguides
Y. Nagao, Y. Kuwamura, A. Nizamuddin, T. Nakahora, T. Hotani, N. Katsuki and T. Katsuyama, Univ. of Fukui (Japan)

P-7-15
Band-pass Optical Filter in Light-induced Self-written Waveguide
H. Watanabe[1], M. Tomiki[1], H. Sakata[1], T. Yamashita[2], A. Kawasaki[2] and M. Kagami[2], [1]Shizuoka Univ. and [2]Toyota Central R&D Labs. (Japan)

P-7-16
Basic Study of Coupling on 3D Cross of Si Photonic Wire waveguide for Optical Interconnection on Inter/inner-chip
K. Furuya[1,2], T. Takei[1,2], T. Kamei[1,2], Y. Sakakibara[1,2] and M. Mori[1,2], [1]AIST and [2]PECST (Japan)

P-7-17
Fabrication and Characterization of InGaAs/InAlAs Multiple FACQW Structures with Larger Tolerance to Impurity in Intrinsic Layer
Y. Amma and T. Arakawa, Yokohama National Univ. (Japan)

P-7-18
Numerical Demonstration of InP 1xN Planar Optical Switch Based on Beam Deflection
S. Che, M. Zaitsu, A.Higo, T. Tanemura and Y. Nakano, Univ. of Tokyo (Japan)

P-7-19
Effect of Plasma Processes on the Characteristics of GaAs Related Optical Device Structure
A. Watanabe, F. Ishikawa and M. Kondow, Osaka Univ. (Japan)

P-7-20
Characterization of the Oxide Film Obtained by Wet Oxidation of $Al_xGa_{1-x}As$ with x=0.55-0.99
Y. Hirai, T. Yamada, M. Kondow and F. Ishikawa, Osaka Univ. (Japan)

P-7-21
Structural and luminescence properties of highly crystalline ZnO nanoparticles prepared by sol-gel method
W. Bousslama[1], H. Elhouichet[1,2], B. Gelloz[3], B. Sieber[4], M. Moreau[4], M. Férid[1] and N. Koshida[3], [1]Centre National de Recherches en Sciences des Matériaux, [2]Faculté des Sciences de Tunis, [3]Tokyo Univ. of Agri. and Tech. and [4]Université Lille 1 (Tunisia)

P-7-22
Reduction of Hydrogen Annealing Temperature for Shape Transformation of Si Surface by Very Short Water Rinse
M. Fukuyama, Y. Amemiya and S. Yokoyama, Hiroshima Univ. (Japan)

P-7-23
Optical fiber sensor with multimode interference structure
Y. Matsumoto, S. Taue, K. Tsuruta and H. Fukano, Okayama Univ. (Japan)

P-7-24
Periodic Arrangement of Au Nanoparticles on SOI Photodiode for Absorption Enhancement
A. Ono, H. Satoh, R. Kawai and H. Inokawa, Shizuoka Univ. (Japan)

P-7-25
Enhanced Light Sensitivity of Thin SOI Photodiode by Metal Line-and-Space Grating of Various Materials
H. Satoh, H. Inokawa and A. Ono, Shizuoka Univ. (Japan)

P-7-26
Wavelength Sensitive PIN Photodetector Using Guided Mode Resonance
K. W. Lai, S. D. Lin, Y. J. Fu and Y. S. Li, National Chiao Tung Univ. (Taiwan)

P-7-27
Active Layer Thickness Dependence of the Bandwidth of Amorphous Silicon Photoconductors
T. Maruyama, H. Otosaka and K. Iiyama, Kanazawa Univ. (Japan)

P-7-28
A Visible Light Blinded Photo-detector With an ITO/ZST/Si MIS Device Structure
K. E. Chiu, Y. Y. Lin, Y. C. Sun, M. C. Shih and W. H. Lan, National Univ. of Kaohsiung (Taiwan)

P-7-29
GaN-based MIS Ultra-violet Photodetectors with the CsF current suppressing Layer
C. H. Chen, C. M. Tsai, C. F. Cheng, S. F. Yen and P. Y. Su[1], Cheng Shiu Univ. (Taiwan)

P-7-30
Performance Improvement of 850nm Si Photodiodes by Symmetric Layout in Standard 0.18 µm CMOS Technology
F. P. Chou[1], G. Y. Chen[1], C. W. Wang[1], Z. Y. Li[1], Y. C. Liu[2], W. K. Huang[3] and Y. M. Hsin[1], [1]National Central Univ., [2]HTC Corp. and [3]Novatek Microelectronics Corp. (Taiwan)

Area 8: Advanced Material Synthesis and Crystal Growth Technology
(24 Papers)

P-8-1
Selective-area growth of 4-color InAs-QD ensembles for broadband light source
K. Takeuchi[1], N. Ozaki[1], S. Ohkouchi[2], N. Ikeda[3], Y. Sugimoto[3], K. Asakawa[4] and R. A. Hogg[5], [1]Wakayama Univ., [2]NEC Corp., [3]NIMS, [4]Univ. of Tsukuba and [5]Univ. of Sheffield (Japan)

P-8-2
Characterization of highly stacked InGaAs quantum dots structures grown with ultrahigh-rate MBE growth technique
F. Tanoue[1,2], H. Sugawara[1], K. Akahane[2] and N. Yamamoto[2], [1]Tokyo Metropolitan Univ. and [2]NICT (Japan)

P-8-3
Field Emission Properties of 10-nm Pillars of Organics Fabricated by Pt particles and Plasma Etching
T. Suzuki[1], K. Takeda[1,4], H. Kondo[1], K. Ishikawa[1], Y. Setsuhara[2,4], M. Shiratani[3,4], M. Sekine[1,4] and M. Hori[1,4], [1]Nagoya Univ., [2]Osaka Univ., [3]Kyushu Univ. and [4]CREST-JST (Japan)

P-8-4
Self-induced InAs nanowires grown on natural-oxide-covered Si(111) by molecular-beam epitaxy
S. Wang, X. Yu, H. Wang and J. Zhao, Chinese Academy of Sci. (China)

P-8-5
Epitaxial graphene produced by thermal decomposition of TiC
W. Norimatsu[1,2], K. Kimura[1] and M. Kusunoki[1,2], [1]Nagoya Univ. and [2]JFCC (Japan)

P-8-6
Forms of CVD-grown graphene layers on polycrystalline nickel
K. Kanzaki, H. Hibino and T. Makimoto, NTT Basic Res. Labs. (Japan)

P-8-7
Influence of Annealing Atmosphere on the Epitaxial Graphene Growth on 3C-SiC (111)/Si (111)
H. R. Aryal, K Fujita and T. Egawa, Nagoya Inst. of Tech. (Japan)

P-8-8
Graphene Synthesis on Cu-Ni alloy by Chemical Vapor Deposition
E. Kim[1], Y. S. Kim[1], S. H. Chun[1], W. G. Lee[2] and J. Jung[1], [1]Sejong Univ. and [2]National Nano Fab Center (Korea)

P-8-9
Quantum Chemical Molecular Dynamics Simulation on Si Thin-film Crystal Growth for Solar Cells
T. Kuwahara, Y. Higuchi, N. Ozawa, T. Shimazaki and M. Kubo, Tohoku Univ. (Japan)

P-8-10
Growing high crystallinity Ge NCs on patterned Si substrate by post thermal annealing
C. W. Chiu, T. W. Liao and C. H. Kuan, National Taiwan Univ. (Taiwan)

P-8-11
Polytype transformation path on 4H-SiC during top-seeded solution growth
S. Harada, Alexander, K. Seki, Y. Yamamoto and T. Ujihara, Nagoya Univ. (Japan)

P-8-12
Alignment of In-plane Crystallographic Grain Orientations in Polycrystalline Si Films by Normal and Oblique-Angle Ion-Implantations
A. Nakajima[1], S. Kuroki[2], S. Fujii[2] and T. Ito[1], [1]Hiroshima Univ. and [2]Tohoku Univ. (Japan)

P-8-13
Novel Direct Patterning Technique of Vapor-Deposited Si Thin Films by Laser-Induced Si/Ag Layer Exchange
M. Kiyooka and H. Ikenoue, Kochi National College of Tech. (Japan)

P-8-14
Excimer laser crystallization of a-Ge nanowires on Si substrate
T. W. Liao, Y. K. Wu, C. W. Chiu, H. M. Chen and C. H. Kuan, National Taiwan Univ. (Taiwan)

P-8-15
Characterization of GaGdN/AlGaN/GaGdN Triple-layer Structures with High Gd Concentration for Tunneling Magnetoresistance Devices
K. Higashi, D. Abe, Y. Mitsuno, S. Komori, S. Sano, S. Hasegawa and H. Asahi, Osaka Univ. (Japan)

P-8-16
Molecular Beam Epitaxy of AlGaPN alloys for Optical Confinement structure of Monolithic Optoelectyonic Integrated Circuits on Si Substrate.
K. Kumagai, T. Kawai, K. Yamane, H. Sekiguchi, H. Okada and A. Wakahara, Toyohashi Univ. of Tech. (Japan)

P-8-17
Improving Si Doping Efficiency in GaAsN Epilayers by Using (211)B and (311)B GaAs Substrates
X. Han, M. Inagaki, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-8-18
Quality improvement of GaN grown on Si (111) using metal-organic vapor-phase epitaxy
C. W. Hsu, J. H. Lin, Y. F. Chen and Y. K. Su, National Cheng Kung Univ. (Taiwan)

P-8-19
Controlling the Immobilized process of Au NPs onto TiO_2(110) through Electrostatic Interaction of Ionic Liquids
S. Suzuki[1], Y. Ohta[1], T. Kurimoto[1], S. Kuwabata[2,3] and T. Torimoto[1,3], [1]Nagoya Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)

P-8-22
The bias-crystallization mechanism on structural characteristics and electrical properties of Zn-In-Sn-O film
K. J. Chen, F. Y. Hung, S. J. Chang, T. S. Lui, S. P. Chang, Z. S. Hu, T. P. Chen and T. Y. Liao, National Cheng Kung Univ. (Taiwan)

P-8-23
Growth of ZnMgTe/ZnTe Waveguide Structures and Analysis of the Light Polarization with the Electric Field
Y. Kumagai and M. Kobayashi, Waseda Univ. (Japan)

P-8-24
Optical Properties of Ordered arrays of Silica-Metal Core-Shell Nanoparticles
K. Sugawa[1], T. Sakai[1], D. Tanaka[1], J. Otsuki[1] and T. Akiyama[2], [1]Nihon Univ. and [2]Univ. of Shiga Prefecture (Japan)

P-8-25
Photoluminescence and conduction type of $Mg_xZn_{1-x}O$:(N,Cu) films
S. K. Mohanta, A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan)

Area 9: Physics and Application of Novel Functional Devices and Materials
(19 Papers)

P-9-1
Photo-rechargeable Battery Based on Photo-induced Copper Intercalation into Quasi-One-Dimensional Compound $KFeS_2$
S. Takenoshita, R. Yatabe, M. Kozaki, H. Kuriyaki and K. Toko, Kyushu Univ. (Japan)

P-9-2
Gap Plasmon Enhancement on a Silver Nanowire with AFM Metal Tip
Y. C. Wang[1,2], C. T. Yuan[1], M. Y. Kuo[1], M. C. Wu[2], J. Tang[1] and M. H. Shih[1], [1]National Tsing Hua Univ. and [2]Academia Sinica (Taiwan)

P-9-3
Observation of cavity polaritons in one-dimensional photonic crystal with organic dye J-aggregates
K. Ishii, M. Yamashima, Y. Kondo, S. Nakanishi and N. Tsurumachi, Kagawa Univ. (Japan)

P-9-4
Phonon-Assisted Band-to-Band Luminescence and Carrier Recombination Processes in $SrTiO_3$
Y. Yamada and Y. Kanemitsu, Kyoto Univ. (Japan)

P-9-5
Effects of Interface Grading on Electronic States in Columnar Type-II Quantum Dots
T. Kawazu, NIMS (Japan)

P-9-6
Dynamic Nuclear Polarization Induced by Breakdown of Even-integer Quantum Hall Effect
S. Umezawa[1], R. Moriya[1], T. Yamashita[1], M. Kawamura[1,2,3], S. Masubuchi[1,3], Y. Hashimoto[1], S. Katsumoto[4] and T. Machida[1], [1]Univ. of Tokyo, [2]RIKEN and [3]PRESTO-JST (Japan)

P-9-7
A Multi-purpose Electrostatically Defined Silicon Quantum Dot Structure
M. A. Sulthoni, T. Kodera, Y. Kawano and S. Oda, Tokyo Tech (Japan)

P-9-8
Time-resolved observation of carrier and coherent phonon in 4H-SiC under off-resonant excitation
K. Kato, K. Oguri, A. Ishizawa, H. Nakano and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-9-9
First-Principles Study of Electronic Structures of AlN/GaN Superlattices
K. Kamiya[1], M. Kasu[2] and K. Shiraishi[1], [1]Univ. of Tsukuba and [2]NTT Basic Res. Labs. (Japan)

P-9-11
Effect of Capping Layer Growth on Bound Exciton Luminescence in Nitrogen δ-Doped GaAs
Y. Harada, T. Kubo, T. Inoue, O. Kojima and T. Kita, Kobe Univ. (Japan)

P-9-12
Electron emission properties of GaAsN/GaAs quantum well containing N-related localized states: the influence of illuminance
M. C. Hsieh, J. F. Wang, K. H. Tseng, C. H. Chao, Y. C. Chi, R. C. C. Chen, C. H. Yang, Y. S. Wang, C. H. Chiang and J. F. Chen, National Chiao Tung Univ. (Taiwan)

P-9-13
Electrical Characteristics and TDDB Reliability of $ZrO_2/Al_2O_3/ZrO_2$ Stack High-κ Gate Dielectric
C. L. Lin[1], S. C. Wu[1], C. C. Tang[1] and M. Y. Li[2], [1]Feng Chia Univ. and [2]ProMOS Tech. Inc. (Taiwan)

P-9-14
Retention characteristics of resistance switching memory using $Si/CaF_2/CdF_2$ quantum-well structures
M. Watanabe and K. Uryu, Tokyo Tech (Japan)

P-9-15
Two Terminal Switching Device for Spin Transfer Torque (STT) MRAM
G. H. Kil, H. J. Yang, S. H. Lee and Y. H. Song, Hanyang Univ. (Korea)

P-9-16
P-type Tunneling Transistors with Poly-Si by Sequential Lateral Solidification (SLS) Growth Technique
M. H. Lee, T. H. Wu and S. C. Weng, National Taiwan Normal Univ. (Taiwan)

P-9-17
***In-situ* TEM Observation for Formation of Au Nanowires and Nanogaps caused by Electromigration**
Y. Murakami, M. Arita, K. Hamada and Y. Takahashi, Hokkaido Univ. (Japan)

P-9-18
Optical selection rules for graphene nanoribbons
K. Sasaki, K. Kato, Y. Tokura and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-9-19
Tunnel Spin Injection into Graphene Using Al_2O_3/PTCA Barrier Grown by Atomic Layer Deposition
T. Yamaguchi[1], S. Masubuchi[1], K. Iguchi[1], R. Moriya[1] and T. Machida[1,2], [1]Univ. of Tokyo and [2]PRESTO-JST (Japan)

P-9-20 (Late News)
Si-Nanowire-Based Memristors Constructed Using Top-Down Methods for Flexible Electronic Systems
T. Moon[1], J. Kang[1], Y. Han[1], C. Kim[2], Y. Jeon[1], H. Kim[1] and S. Kim[1], [1]Korea Univ. and [2]Lawrence Berkeley National Laboratory (Korea)

Area 10: Organic Materials Science, Device Physics, and Applications
(20 Papers)

P-10-1
Formation of Organic Nanodots Using Diamine Derivative and Self-Assembled Monolayer
T. Morimoto[1], S. G. Park[1], T. Inden[1], T. Nishikawa[2] and T. Mori[1], [1]Nagoya Univ. and [2]Iwate Univ. (Japan)

P-10-2
Thermal Annealing Effects on Aligned π-Conjugated Polymer Films Fabricated by Capillary Action
T. Higashi, N. Yamasaki, H. Utsumi, H. Yoshida, A. Fujii and M. Ozaki, Osaka Univ. (Japan)

P-10-3
Fabrication and Characterization of Uniaxially Oriented Vinylidene Fluoride Oligomer Thin Films
Y. Kuroda, Y. Koshiba, M. Misaki, S. Horie, K. Ishida and Y. Ueda, Kobe Univ. (Japan)

P-10-4
Enhancing the performance of pentacene-based organic thin film transistors by inserting alternately stacked NPB and Alq_3 buffer layers
C. M. Wu, S. H. Su, W. C. Weng, H. L. Tsai and M. Yokoyama, I-Shou Univ. (Taiwan)

P-10-5
Charge transport through film surface and substrate interface in solution-processed polymer field-effect transistors
K. Takagi[1], T. Nagase[1,2], T. Kobayashi[1,2], T. Kushida[3] and H. Naito[1,2], [1]Osaka Prefecture Univ. and [2]Teijin Ltd. (Japan)

P-10-6
Light-Emitting Field-Effect Transistors Having Metal Electrodes Modified with an Organic Thin Film
A. Okada, Y. Fukaya, S. Hotta and T. Yamao, Kyoto Inst. of Tech. (Japan)

P-10-7
High Transparent Conductive Film by Self-Assembled Silver Nanoparticles Network Electrode with Anti-Reflective Coating
K. Fujimoto[1], S. Shiratori[1], K. Yamane[2], K. Nakata[2] and K. Tamari[2], [1]Keio Univ. and [2]Toda Kogyo Corp. (Japan)

P-10-8
Crystalline quality variations in epitaxial-grown C_{60} thin films by magnesium atoms doping.
C. Morales, N. Kojima, S. Nishi, N. Ogata and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-10-9
Metal patterning for organic electronics based on metal undeposition effect on soft polymer surfaces
K. Tsuji and T. Tsujioka, Osaka Kyoiku Univ. (Japan)

P-10-10
Change in Capacitance of Organic Light-Emitting Diodes
T. Inden[1], T. Satoh[2], S. G. Park[1], T. Morimoto[1], T. Nishikawa[3] and T. Mori[1], [1]Nagoya Univ., [2]Toyota Central Research & Development Labs. and [3]Iwate Univ. (Japan)

P-10-11
Dependence of additive-solvent on bulk-heterojunction organic photovoltaic cell fabricated by electrospray deposition method
K. Takagi[1,2], T. Asano[1,2], T. Fukuda[1,2], Z. Honda[1], N. Kamata[1], H. Shirai[1], J. Ju[2], Y. Yamagata[2] and Y. Tajima[2], [1]Saitama Univ and [2]RIKEN (Japan)

P-10-12
Fabrication of the inverted bulk heterojunction organic solar cell on titanium oxide nanosheet
Y. Maruyama and E. Itoh, Shinshu Univ. (Japan)

P-10-13
Relationship between the work function of the hole collection electrode and the temperature dependence of open-circuit voltage in multi layered organic solar cells
T. Shirotori and E. Itoh, Shinshu Univ. (Japan)

P-10-14
Improvement of hole injection characteristics in multilayered organic photovoltaic devices by the insertion of organic interfacial layer
S. Nakagoshi and E. Itoh, Shinshu Univ. (Japan)

P-10-15
Doping Effects of Liquid Crystalline Phthalocyanine in Bulk Heterojunction Polymer Solar Cells
T. Masuda[1], T. Hori[1], N. Fukuoka[1], Y. Miyake[1,2], D. Q. Duy[1], T. Hayashi[1], T. Kamikado[1], H. Yoshida[1], A. Fujii[1], Y. Shimizu[2] and M. Ozaki[1], [1]Osaka Univ. and [2]AIST (Japan)

P-10-16
Fundamental Study on Organic Solar Cells based on Soluble ZnPc
I. Yamada[1,2], M. Umeda[1], Y. Hayashi[1], T. Soga[1] and N. Shibata[1], [1]Nagoya Inst. of Tech. and [2]Suzuka National College of Tech. (Japan)

P-10-17
The examination of the most appropriate size of ZnO nanorods in organic-inorganic hybrid solar cells
T. Ichikawa and S. Shiratori, Keio Univ. (Japan)

P-10-18
Fabrication and Evaluation of Organic Photoelectric Conversion Devices using Electrodeposited Polyaniline Films as a Hole Transporting Layer
K. Inoue, A. Suzuki, T. Oku and T. Akiyama, Univ. of Shiga Prefecture (Japan)

P-10-19 (Late News)
Fullerene Memory Transistors with a Chargeable Polymer
D. T. Toan, H. Sakai, T. Matsushima and H. Murata, JAIST (Japan)

P-10-20 (Late News)
Printed OTFT-backplane for Electrophoretic Display Characterized by High Uniformity of Performance over a Large Area
J. W. Hwang, G. S. Ryu, J. S. Kim and C. K. Song, Dong-A Univ. (Korea)

Area 11: Micro/Nano Electromechanical Systems and Bio/Medical Analyses
(14 Papers)

P-11-1
Quantitative characterization of guided motion of dynein-microtubule system
N. Ashikari[1,2], Y. Shitaka[2], H. Sakaue[1], T. Takahagi[1], H. Kojima[2], K. Oiwa[2] and H. Suzuki[1], [1]Hiroshima Univ. and [2]NICT (Japan)

P-11-2
Label-free detection of creatinine using a disposable poly-N-isopropylacrylamide as an encapsulating enzyme material based on high-κ $Eu_2Ti_2O_7$ EIS devices
T, M, Pan[1], P. Y. Liao[1], K. Y. Chang[1], C. W. Lin[1] and L. Chi[2], [1]Chang Gung University and [2]Westfälische Wilhelms-Univ. Münster (Taiwan)

P-11-3
Development of Implantable Si Neural Probe with Stimulus and Recording Electrodes for Deep Brain Stimulation
Y. Yukita, S. Lee, S. Kanno, K. Lee, T. Fukushima, M. Koyanagi, N. Katayama, H. Mushiake and T. Tanaka, Tohoku Univ. (Japan)

P-11-4
Band-to-Band Tunneling Transistor for Application to Bio Sensor
T. Tabei, K. Shibahara and S. Yokoyama, Hiroshima Univ. (Japan)

P-11-5
Scaling of the Pull-In Voltage in a Novel CMOS-compatible NEMS Switch
D. J. Baek, S. J. Choi, D. I. Moon and Y. K. Choi, KAIST (Korea)

P-11-6
Photoresist Spray Coating Using Aperture toward Trench-type 3D Microdevices
N. Fukuda, S. Kumagai and M. Sasaki, Toyota Technological Inst. (Japan)

P-11-7
Analysis of Sharp Dip Structures on THz Transmission Spectra of Metallic Meshes
T. Hasebe and H. Tabata, Univ. of Tokyo (Japan)

P-11-8
Realization of ion-sensitive field-effect transistor on SOI substrate with engineered sensing membrane for high stability
H. J. Jang and W. J. Cho, Kwangwoon Univ. (Korea)

P-11-9
Acceleration Sensor Based on CMOS Inverter Having Force Balanced Movable Gate Electrode
M. Suzuki[1], J. Kogure[1], K. Kitamura[1], T. Takahashi[1], S. Yokoyama[2], H. Tokunaga[3] and S. Aoyagi, [1]Kansai Univ., [2]Hiroshima Univ. and [3]M. T. C. Corp. (Japan)

P-11-10
Carbon Nanotube Network Conjugated by Nanoparticles with Defined Nanometer-Scaled Gaps
M. Kobayashi[1,2,3], S. Kumagai[3,4], K. Shiba[1,3], Y. Uraoka[2,3] and I. Yamashita[2,3], [1]Japanese Foundation for Cancer Res., [2]NAIST, [3]CREST-JST and [4]Toyota Technological Inst. (Japan)

P-11-11
Plasma Induced Damage Affecting Mechanical Properties of Silicon Microcantilevers and Effects of Thermal Annealing on Their Recovery
A. Wada[1], Y. Yanagisawa[1], M. Tomura[1], C.-H. Huang[1], S. Yamasaki[2], T. Ono[1] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)

P-11-12
Engineering Biocompatibility and Assembly in Carbon Nanotube Electrodes Using the Physicochemical Properties of Chitosan
L. Bugnicourt, S. Trigueros and S. A. Contera, Univ. of Oxford and Ecole Central de Lyon (UK)

P-11-13
Nanoparticle-Induced Crystallization of Amorphous Ge Film Using Ferritin
M. Uenuma[1,2], B. Zheng[1,2], T. Imazawa[1,2], N. Okamoto[1], M. Horita[1,2], T. Nishida[1,2], Y. Ishikawa[1,2], H. Watanabe[2,3], I. Yamashita[1,2] and Y. Uraoka[1,2], [1]NAIST, [2]CREST-JST and [3]Osaka Univ. (Japan)

P-11-14
Extending Rotation Range of Spatial Light Modulator by Metal-Induced Lateral Crystallization of Amorphous Si Using Ni Ferritin Molecules
S. Kumagai[1,3], S. Miyachi[1], H. Murase[1], I. Yamashita[2,3], Y. Uraoka[2,3] and M. Sasaki[1,3], [1]Toyota Technological Institute, [2]NAIST and [3]CREST-JST (Japan)

Area 12: Spintronics Materials and Devices
(16 Papers)

P-12-1
Investigation of Regular Arrangements of Ferromagnetic MnAs Nanoclusters for New Planar Magnetoelectronic Devices
M. T. Elm[1], M. Fischer[3], P. J. Klar[3] and S. Hara[1,2], [1]Hokkaido Univ., [2]PRESTO-JST and [3]Justus-Liebig Univ. (Japan)

P-12-2
Structure and Magnetic Properties of Diluted Magnetic Semiconductor Superlattice GaGdAs/GaAs Grown by MBE
Y. Uda, H. Miyagawa, S. Koshiba, N. Tsurumachi, S. Nakanishi, Y. Tanaka, H. Itoh and N.Takahashi, Kagawa Univ. (Japan)

P-12-3
Magnetic behaviors of (Ga,Mn)As/Co_2FeAl Bilayers grown by molecular-beam epitaxy
S. H. Nie[1,2], L. Chen[1], K. K. Meng[1], X. Z. Yu[1], L. J. Zhu[1], W. S. Yan[3], Y. G. Zhao[2] and J. H. Zhao[1], [1]Chinese Academy of Sci., [2]Tsinghua Univ and [3]Univ. of Sci. & Tech. of China (China)

P-12-4
Magnetoresistance effects in $La_{1-x}Sr_xMnO_3$/Nb-$SrTiO_3$/Co junctions
K. Tozawa, K. Kobayashi, T. Miyawaki, K. Ueda and H. Asano, Nagoya Univ. (Japan)

P-12-5
Anisotropic magnetoresistance in half-metallic Co_2MnSi epitaxial films
F. J. Yang, Y. Sakuraba and K. Takanashi, Tohoku Univ. (Japan)

P-12-6
Fabrication of $MgAl_2O_4$ thin films on ferromagnetic Heusler alloy Fe_2CrSi by reactive magnetron sputtering
N. Fukatani, K. Inagaki, K. Mari, H. Fujita, T. Miyawaki, K. Ueda and H. Asano, Nagoya Univ. (Japan)

P-12-7
Spectroscopic Detection of Double Exchange Magnetism Signatures in Mn $L_{2,3}$ and O-vacancy Spectra in $La_{1-x}Sr_xMnO_3$ Alloys with x = 0.2
G. Lucovsky[1], C. Adamo[2] and D. G. Schlom[2], [1]North Carolina State Univ. and [2]Cornell Univ. (USA)

P-12-8
Formation of Nitrogen Vacancy Adjoining to Gd Ion Doped in GaN
D. Abe, K. Higashi, S. Emura, Y. K. Zhou, S. Hasegawa and H. Asahi, Osaka Univ. (Japan)

P-12-9
Effect of GaAs Surface Structure on Tunneling Anisotropic Magnetoresistance in Epitaxial $Co_{50}Fe_{50}$/n-GaAs Junctions
T. Uemura, T. Akiho, M. Harada, K. Matsuda and M. Yamamoto, Hokkaido Univ. (Japan)

P-12-10
Different magnetic properties of $L1_0$-FePt grown on sputtered and EB deposited MgO / GaAs structures
R. Ohsugi[1], M. Kohda[1,2], T. Seki[3], M. Mizuguchi[3], K. Takanashi[3] and J. Nitta[1], [1]Tohoku Univ. and [2]PRESTO-JST (Japan)

P-12-11
Tight-binding calculation of conductance and magnetoresistance in disordered FM/graphene/FM junctions
S. Honda[1], R. Sato[2], A. Yamamura[2], T. Hiraiwa[2], H. Itoh[1] and J. Inoue[2], [1]Kansai Univ. and [2]Nagoya Univ. (Japan)

P-12-12
High-Speed-Search Nonvolatile TCAM Using MTJ Devices
S. Matsunaga, A. Katsumata, M. Natsui, T. Endoh, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)

P-12-13
Fast Switching in Magnetic Tunnel Junctions with Double Barrier Layer
A. Makarov, V. Sverdlov, D. Osintsev and S. Selberherr, TU Wien (Austria)

P-12-14
Stochastic State Transition of a Spin Torque Nano Oscillator
K. Nakada[1], S. Yakata[1,2] and T. Kimura[1,2], [1]Kyushu Univ. and [2]CREST-JST (Japan)

P-12-15
Spin-Photon Memory and Spin Transistor with Floating Gate
V. Zayets, H. Saito, S. Yuasa and K. Ando, AIST (Japan)

P-12-16 (Late News)
Temperature Dependence of Spin Relaxation Time in InAs Columnar Quantum Dots at 10 to 50 K
S. Nakanishi[1], K. Sasayama[1], Y. Oyanagi[1], R. Yamaguchi[1], S. Lu[2], L. H. Li[3], A. Fiore[4] and A. Tackeuchi[1], [1]Waseda Univ., [2]Chinese Academy of Sci., [3]Ecole Polytechnique Federale de Lausanne and [4]Eindhoven Univ. of Tech. (Japan)

Area 13: Application of Nanotubes, Nanowires, and Graphene
(28 Papers)

P-13-1
Fabrication and Characterization of InP Nanowire Light Emitting Diodes
S. Maeda[1], K. Tomioka[1,2], S. Hara[1] and J. Motohisa[1], [1]Hokkaido Univ. and [2]PRESTO-JST (Japan)

P-13-2
Analysis of Bottom Channel Effect in Silicon Nanowire FET based on Bulk-Silicon: Reduction of Parasitic Capacitance caused by SiGe layer
M. D. Ko[1], S. H. Lee[1], R. H. Baek[1], C. H. Park[1], C. W. Sohn[1], C. K. Baek[1,2], J. S. Lee[1] and Y. H. Jeong[1], [1]POSTECH and [2]NCNT (Korea)

P-13-3
A Multi Switching Current Study of Single-Electron Transistors Using Side Gate Bias Effect
J. E. Lee[1], J. W. Kim[1], J. H. Lee[1], K. C.Kang[1], J. H. Lee[1], H. C. Shin[1], K. J. Yoh[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Hokkaido Univ. (Korea)

P-13-4
Growth of GaAs Nanowires on Poly-Si by Selective-Area MOVPE
K. Ikejiri[1], K. Tomioka[1], S. Imai[2] and T. Fukui[1], [1]Hokkaido Univ. and [2]Sharp Corp. (Japan)

P-13-5
Formation of ohmic contact of InP nanowires without annealing processes
G. Zhang, S. Saito, K. Tateno, H. Gotoh and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-13-6
Suppression of surface nanocrystal nucleation in growth of GaAs nanowire on Si(111) by molecular beam epitaxy
J. K. Kwoen, N. Kumagai, K. Watanabe, S. Ohkouchi, S. Iwamoto and Y. Arakawa, Univ. of Tokyo (Japan)

P-13-7
Thermoelectric power of catalyst-free GaAs nanowires grown by MBE-VLS method
J. H. Paek, M. Yamaguchi and H. Amano, Nagoya Univ. (Japan)

P-13-8
Effect of the Drain Configuration on the Current-Voltage Characteristics of Vertical Nanowire Field Effect Transistors
S. Karmalkar, V. K. Gurugubelli and K. R. K. Maheswaran, Indian Inst. of Tech. (India)

P-13-9
Graphene Gated SiO_2 Core-shell Silicon Nanowire Transistors
J. E. Jin[1], J. H. Lee[1,2], D. H. Hwang[1], D. W. Kim[1], M. J. Kim[1,2], K. S. Son[1,2], D. Whang[1,2] and S. W. Hwang[1], [1]Korea Univ. and [2]Sungkyunkwan Univ. (Korea)

P-13-10
Tunable Magnetic Properties of Rhombohedral Graphite Thin Films
N. T. Cuong[1,3], M. Otani[1,3] and S. Okada[2,3], [1]AIST, [2]Univ. of Tsukuba and [3]CREST-JST (Japan)

P-13-11
Precise control of layer number in graphene grown on Ni(111)
S. Entani, Y. Matsumoto, M. Ohtomo, P.V. Avramov, H. Naramoto and S. Sakai, JAEA (Japan)

P-13-12
Selective-area-grown graphene transistors by thermal chemical vapor deposition method
M. Okai[1], K. Tokumoto[2], T. Kyotani[2], M. Tokuda[2], K. Tsutsui[3] and Y. Wada[3], [1]Hitachi Ltd., [2]Tohoku Univ. and [3]Toyo Univ. (Japan)

P-13-13
Electronic Structure and Energetics of Corrugated Graphene Sheet
S. Okada[1,2] and T. Kawai[1,2], [1]Univ. of Tsukuba and [2]NEC Corp. (Japan)

P-13-14
Ultrafast Synthesis of Nanographene Employing an Ultrahigh-density In-liquid Al-cohol Plasma
T. Hagino, H. Kondo, H. Kano, K. Ishikawa, M. Sekine and M. Hori, Nagoya Univ. (Japan)

P-13-15
RF Transmission Line Characteristics of Graphenes
H. J. Lee, E. Kim and J. Jung, Sejong Univ. (Korea)

P-13-16
Ballistic Current Model for Graphene Nanoribbon Field-Effect Transistors
Y. Li, Y. Zhang, F. Liu, Y. Yang, Y. Wang and X. Liu, Peking Univ. (China)

P-13-17
Formation of quantum dots in monolayer graphene with an energy gap
G. Giavaras[1] and F. Nori[1,2], [1]RIKEN and [2]Univ. of Michigan (Japan)

P-13-18
Optical and electrical properties of graphene layers directly-grown by Alcohol-CVD
A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan)

P-13-19
Crystallographic and Electrical Properties of Semiconducting Graphene Nanoribbon Grown Employing CH_4/H_2 plasma
H. J. Cho, K. Takeda, H. Kondo, K. Ishikawa, M. Sekine and M. Hori, Nagoya Univ. (Japan)

P-13-20
Effect of Plasma Treatment on CVD-grown Graphene/Metal Contact
T. Kwon, H. An and J. Jung, Sejong. Univ. (Korea)

P-13-21
Development of Two-Dimensional Strain-Distribution Sensor Using Carbon Nanotube-Dispersed Resin
K. Suzuki, Y. Suzuki, Y. Ohashi, M. Ohnishi and H. Miura, Tohoku Univ. (Japan)

P-13-22
Improvement of transfer characteristics for PZT-CNT-FET by ionic liquid
S. Kataoka[1], T. Arie[1,2] and S. Akita[1,2], [1]Osaka Prefecture Univ. and [2]CREST-JST (Japan)

P-13-23
Strain Dependence of the Electronic Conductivity of Carbon Nanotubes and Graphene Sheets
M. Ohnishi, K. Suzuki and H. Miura, Tohoku Univ. (Japan)

P-13-24
Analysis of FET Operation Mechanism in SWNT Networks Using Scanning Gate Microscopy
X. Wei[1], K. Maeda[1], T. Yahagi[1], S. Shimozono[1], M. Matsunaga[1], N. Aoki[1], J. P. Bird[2] and Y. Ochiai[1], [1]Chiba Univ. and [2]Univ. at Buffalo (Japan)

P-13-27
Interfaces of High-k Gate Insulator in Carbon Nanotube FETs
K. Suzuki, Y. Ohno, S. Kishimoto and T. Mizutani, Nagoya Univ. (Japan)

P-13-28
Observation of n-type conduction in CNTFETs with Au contacts in vacuum
H. Imaeda, S. Ishii, S. Kishimoto, Y. Ohno and T. Mizutani, Nagoya Univ. (Japan)

Area 14: Photovoltaics & Power Semiconductor Devices
(21 Papers)

P-14-1
Atomic Layer Deposited Aluminum Oxide Passivation Layers for Crystalline Silicon: Effects of Deposition Temperature on Film and Interface Structures
H. Lee[1,5], N. Sawamoto[1,5], T. Tachibana[1,5], N. Ikeno[1,5], K. Arafune[2,5], H. Yoshida[2,5], S. Satoh[2,5], K. Matsumoto[3], K. Takahashi[3], T. Chikyow[4] and A. Ogura[1,5], [1]Meiji Univ., [2]Univ. of Hyogo, [3]Tokyo Electron Ltd., [4]NIMS and [5]CREST-JST (Japan)

P-14-2
Surface Recombination of Crystalline Silicon Substrates Passivated by Atomic Layer Deposited AlO_x
K. Arafune[1,5], S. Miki[1,5], R. Matsutani[1,5], J. Hamano[1,5], H. Yoshida[1,5], T. Tachibana[2,5], A. Ogura[2,5], K. Matsumoto[3], K. Takahashi[3], Y. Ohshita[4,5] and S. Satoh[1,5], [1]Univ. of Hyogo, [2]Meiji Univ., [3]Tokyo Electron Ltd., [4]Toyota Technological Inst. and [5]CREST-JST (Japan)

P-14-3
Optimization of a-Si/c-Si heterojunction solar cells by BF_2 ion implantation
T. H. Tasi, Y. C. Wu and C. H. Chen, National Tsing Hua Univ. (Taiwan)

P-14-4
Amorphous Silicon Thin Film Solar Cell Utilizing ITO Patterned Electrode
H. W. Liu, T. G. Chen, C. H. Chang and P. Yu, National Chiao Tung Univ. (Taiwan)

P-14-5
Patterned Glass Substrates for Enhanced Solar Energy Harvesting in Thin Film Solar Cells
T. G. Chen, Y. L. Tsai, M. A. Tsai, P. Yu, J. M. Shieh and H. C. Kuo, National Chiao Tung Univ. (Taiwan)

P-14-6
Electrode-Contact Enhancement in Silicon Nanowire-Array-Textured Solar Cells
C. Chen[1], R. Jia[1], H. Li[1], Y. Meng[1], S. Kasai[2] and H. Tamotsu[2], [1]Chinese Academy of Sci. and [2]Hokkaido Univ. (China)

P-14-7
Theoretical Study on the Effect of Size and Interface of Si Quantum Dots on Carrier Multiplication
S. Hirose, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, H. Takaba and A. Miyamoto, Tohoku Univ. (Japan)

P-14-8
Enhanced Conversion Efficiency of a Crystalline Silicon Solar Cell with Frustum Nanorod Arrays
Y. L. Tsai, M. A. Tsai, P. C. Tseng, H. C. Chen, H. C. Kuo and P. C. Yu, National Chiao Tung Univ. (Taiwan)

P-14-9
Transfer of $CuInS_2$ Layer by Lift-Off Process and Its Superstrate-Type Solar Cell Applications
Y. Abe, S. Osada, S. Fukamizu, Y. Oda, T. Minemoto, K. Nakanishi, T. Ohta and H. Takakura, Ritsumeikan Univ. (Japan)

P-14-10
First principles study on Cd and Zn doping in $CuInSe_2$ and related compounds
T. Maeda and T. Wada, Ryukoku Univ. (Japan)

P-14-11
N-H structure in GaAsN and interaction between N-H local vibration mode and lower frequency phonon
K. Ikeda, M. Inagaki, S. Wada, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-14-12
Thermally Activated Electron Transport in GaAsN
M. Inagaki, K. Ikeda, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-14-13
Laser Annealing to Form High-Temperature Phase of FeS_2 (pyrite)
M. Umehara, Y. Takeda, H. Azuma and T. Motohiro, Toyota Central R&D Labs. Inc. (Japan)

P-14-14
Photoelectric Conversion Devices based on InP Porous Structures
R. Jinbo, T. Kudo and T. Sato, Hokkaido Univ. (Japan)

P-14-15
Hydrothermal Synthesis of TiO_2 Porous Hollow Nanospheres for Coating on the Photoelectrode of DSSCs
V. M. Mohan and K. Murakami, Shizuoka Univ. (Japan)

P-14-17
Investigation of Hot Carrier Degradation in STI-based High-Voltage LDMOSFETs by a Novel DCIV technique
Y. He and G. Zhang, Peking Univ. (China)

P-14-18
High accurate TCAD calibration methodology realizing smart-design of integrated power devices consisting of lateral-IGBT & Diode in SOI micro-inverters
H. Kato[1], S. Harada[1], C. S. Yun[2], V. Meniailenko[2], Y. Ashida[1], S. Takahashi[1] and N. Tokura[1], [1]DENSO Corp. and [2]Synopsys Inc. (Japan)

P-14-19
Current Transport Characteristics of Quasi-$Al_xGa_{1-x}N$/SiC Heterojunction Bipolar Transistors with Various Band Discontinuities
T. Okuda, H. Miyake, T. Kimoto and J. Suda, Kyoto Univ. (Japan)

P-14-20
Estimation of the Surface Recombination Velocity from Thickness dependence of the carrier Lifetime in n-type 4H-SiC Epilayers
M. Kato, A. Yoshida and M. Ichimura, Nagoya Inst. of Tech. (Japan)

P-14-21 (Late News)
Semi-Quantitative Determination of Radiative Recombination Centers in Silicon Power Devices by Cross-Sectional Cathodoluminescence
R. Sugie, K. Inoue and M. Yoshikawa, Toray Research Center Inc. (Japan)