ADVANCE PROGRAM

2011 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference — September 28-30, 2011

Place — Aichi Industry & Labor Center (WINC AICHI)

Short Course & Workshop — September 27, 2011

Sponsored by
The Japan Society of Applied Physics
Technical-Cosponsored by
IEEE Electron Devices Society
in cooperation with
The Electrochemical Society of Japan
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ssdm 2011

Web Site : http://www.ssdm.jp

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PREFACE

On behalf of the organizing committee, it is my great pleasure and honor to welcome you to the 43rd International Conference on Solid State Devices and Materials (SSDM 2011), held on September 28–30, 2011 in Nagoya, Japan. SSDM 2011 is sponsored by the Japan Society of Applied Physics and technically co-sponsored by the IEEE Electron Devices Society. This year, the venue for SSDM 2011 is the Aichi Industry & Labor Center (WINC AICHI), Nagoya, which is located at the center of Nagoya City. Nagoya City is a castle town established 400 years ago that today is an industrial core of electronic and automotive fields in Japan.

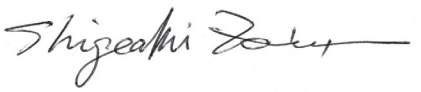
SSDM is one of the most important large-scale conferences in the field of solid state device technologies and materials, presenting the latest scientific achievements and opportunities to exchange technological information. SSDM has been continuously growing and increasing its significance as a unique conference covering a broad spectrum in the field; SSDM covers a very wide scope and includes the physics and processing technology of electron devices, photonic devices and organic devices, as well as their materials and integration into circuits and systems.

In the plenary session, we are pleased to invite three distinguished speakers, Dr. Masao Fukuma (Semiconductor Industry Research Institute Japan, Japan), Dr. Moritaka Yoshida (Toyota Motor Corporation, Japan) and Prof. Tsu-Jae King Liu (University of California at Berkeley, USA), who will speak on future prospects in the semiconductor industry and the application fields of nanoelectronics, respectively. In addition, SSDM 2011 features short courses and workshops. This year, we have planned two short courses related to advanced CMOS technology and carbon-nanotubes/graphenes, and two workshops related to wide gap semiconductor power devices and organic electronics, for stimulating and encouraging students and young researchers and engineers. These short courses and workshops will be held on September 27, the day before the conference.

Reflecting the international nature of SSDM, 966 high quality abstracts were submitted to SSDM 2011 from 24 countries, a record number of submitted abstracts in SSDM history. Great effort by the technical program committee in selecting the abstracts has resulted in an excellent technical program consisting of 55 invited papers, including the three plenary talks, 390 contributed oral papers, 261 poster papers, and 32 late news papers. The papers have been categorized into 14 sub-areas, covering advanced and important topics. We hope all of the papers presented at SSDM 2011 address in depth nearly all the key issues in the field and provide stimulation and new perspectives to all participants.

We wish to express our sincere appreciation to all the committee members for their tremendously significant contribution to SSDM 2011. We also express our heartfelt gratitude for the financial support provided by the supporting corporations and foundations, including MEXT-JSPS. And finally, we sincerely hope SSDM 2011 enhances your research for upcoming years and provides you with an invaluable experience.

September 2011



Shigeaki Zaima
General Chair, SSDM 2011
Professor, Nagoya University

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GENERAL INFORMATION

DATE

Conference: **September 28-30, 2011 (Official language is English)**
Short Courses/Workshops: **September 27, 2011 (in English)**

CONFERENCE VENUE

Aichi Industry & Labor Center (WINC AICHI)
4-4-38 Meieki, Nakamura-ku, Nagoya, Aichi 450-0002, Japan
Phone: +81-52-571-6131 Fax: +81-52-571-6132
http://www.winc-aichi.jp/
SSDM 2011 will be held at WINC AICHI, the main Conference room of WINC AICHI. The access map to the Conference is available in the conference website and also on Page 61 in this booklet. The conference rooms are distributed over the venue. For details, see the map on the conference website and on Page 62-64 in this booklet.

Nagoya Marriott Associa Hotel
1-1-4 Meieki, Nakamura-ku Nagoya, Aichi 450-6002, Japan
Phone: + 81-52-584-1212 Fax: + 81-52-584-1213
http://www.associa.com/english/
Conference Banquet will be held on September 28, 19:00-21:00 at Tower Ball Room, 16F, in Nagoya Marriott Associa Hotel. The hotel is located in five minutes walk from the WINC AICHI. The access map from WINC AICHI to the hotel is available on the conference website and on Page 61 in this booklet. The Banquet fee is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket beforehand. Drinks and appetizers will be served. During the Banquet, SSDM Young Researcher Award ceremony will be held.

TECHNICAL SESSIONS AND EVENTS

Oral and Poster Presentations:
The oral presentations will be held at halls located on 5th, 10th, 11th, and 12th floor in WINC AICHI. during the conference. The poster presentations will be held on September 29, 13:30-15:00, at Exhibition Hall, 6F, in WINC AICHI.

Plenary Sessions:
Plenary Sessions are scheduled on September 28, 9:40-12:15 at WINC HALL, 2F, in WINC AICHI. Non-Technical Plenary Talk-Sep.28, 2011, “Social Contribution and Next Giant Leap of Semiconductors” by Masao Fukuma (Semiconductor Industry Research Institute Japan, Japan) will be held from 9:40-10:25. Technical Plenary Talk-Sep.28, 2011, “A Car Guy’s Expectations for Electronics” by Moritaka Yoshida (Toyota Motor Corporation, Japan) will be held from 10:45-11:30 and “Electronics Proliferation through Diversification” by Tsu-Jae King Liu (University of California at Berkeley, U.S.A) from 11:30-12:15.

Welcome Reception:
The welcome Reception will be held on September 27, 18:00-20:00 at Conference Room 1002, 10F, in WINC AICHI.

Rump Sessions:
SSDM 2011 is organizing Rump Session to be held on September 29, 19:00-21:00 at HALL 1&2, 5F, in WINC AICHI. Details can be found on Page 44.

Short Cources (in English):
On September 27, 10:00-17:30, two short course lectures will be held at “Toyoda Auditorium Nagoya University Symposion” and “Noyori Conference Hall”, in Nagoya University. Two courses are for beginners, young researchers and engineers, and students.
1) Material and Processing for Advanced CMOS – From Fundamental to State-of-the-Art –
2) Fundamentals and Applications of Carbon Nanotube and Graphene
*Registrants for short course are able to attend both courses freely.

Workshops (in English):
Workshop will be held on September 27, 13:00-17:45 at Hall 1 and Hall 2, 5F, in WINC AICHI.
1) Current Status and Future Prospective of Wide Gap Semiconductor Power Devices
2) Advancement in Printed Organic Electronics
*A resistant for one workshop is NOT ABLE to attend another workshop.

Award Ceremony:
Award Ceremony for SSDM Award and SSDM Paper Award will be held in Plenary Sessions, which will start at 9:30 AM on September 28 at WINC HALL,2F, in WINC AICHI.

Exhibition:
Exhibition will be held at the exhibition space, Conference Room 1001, 10F. It will start from 8:30-18:00 on September 28, from 8:30-19:00 on September 29, and from 8:30-14:00 on September 30. For details, see Page 48.

REGISTRATION

The Registration desk will be open September 27 to 30. Open hours are as follows:
September 27 16:00 – 19:00 at conference room (10F)
September 28 08:30 – 12:30 at WINC HALL Area (2F)
September 28 12:30 – 17:30 at conference room (10F)

September 29 08:30 – 17:30 at conference room (10F)
September 30 08:30 – 15:30 at conference room (10F)

SPECIAL ISSUE of JJAP

Authors of SSDM 2011 papers are encouraged to submit their original papers to the Special Issue of Japanese Journal of Applied Physics which will be published in February and April, 2012.

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate's stay. Delegates are therefore encouraged to obtain travel insurances (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Nagoya is warm and sometimes humid in September. The temperature range is 18-30°C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo and 60 Hz in western Japan including Nagoya (conference site), Kyoto and Osaka.

INTERNET ACCESS

Complementary internet connection will be available on Speakers Room, 11F, where you can only use the SSDM PC installed in the room to use internet access freely or check your presentation.

PLENARY SESSION

September 28 (Wednesday) 9:40-12:15
2F WINC HALL, WINC AICHI

Non -Technical Plenary Talk

9:40-10:25

“Social Contribution and Next Giant Leap of Semiconductors”

Masao Fukuma
Semiconductor Industry Research Institute Japan, Japan

Technical Plenary Talk

10:45-11:30

“ A Car Guy’s Expectations for Electronics ”

Moritaka Yoshida
Toyota Motor Corporation, Japan

11:30-12:15

“ Electronics Proliferation through Diversification. ”

Tsu-Jae King Liu
University of California at Berkeley, USA

TECHNICAL PROGRAM

Opening & Plenary Sessions (WINC HALL)

Opening Session
Chair: M. Hori, Nagoya Univ.

9:30
Welcome Address
S. Zaima, Nagoya Univ.

Non-Technical Plenary Session
Chair: T. Fukui, Hokkaido Univ.

9:40 PL-1-1
Social Contribution and Next Giant Leap of Semiconductors M. Fukuma, Semiconductor Industry Research Institute Japan, Japan

SSDM Award / Paper Award Presentation
S. Zaima, Nagoya Univ.

Technical Plenary Sessions
Chair: T. Fukui, Hokkaido Univ.

10:45 PL-2-1
A Car Guy's Expectations for Electronics M. Yoshida, Toyota Motor Corporation, Japan

11:30 PL-2-2
Electronics Proliferation through Diversification.
Tsu-Jae King Liu, University of California at Berkeley, USA

12:15-13:30 Lunch

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
A-1: GaN FET Technologies (Area 6) (13:30-15:15) Chairs: T. Tanaka (Panasonic Corp.) S. Tanaka (Shibaura Institute of Tech.)	**BL-1: Organic Photovoltaics (1) (Area 10&14)** (13:30-15:15) Chairs: A. Masuda (AIST) E. Itoh (Shinshu Univ.)	**B-1: OLEDs (Area 10)** (13:30-15:15) Chairs: K. Takimoto (Canon Inc.) T. Lee (GIST)	**C-1: Future Interconnect (Area 2)** (13:30-15:15) Chairs: S. Ogawa (AIST) M. Sato (AIST)	**D-1: Modeling and Circuits (Area 3)** (13:30-15:10) Chairs: E.Yoshida (Fujitsu Semiconductor Ltd.) N. Mori (Osaka Univ.)	**E-1: Ge-MOS (Area 1)** (13:30-15:20) Chairs: T. Nabatame (NIMS) B. H. Lee (GIST)	**F-1: STT-RAM (Area 4)** (13:30-15:00) Chairs: G. H. Koh (Samsung Electronics Co., Ltd) S. Miura (NEC Corp.)
13:30 A-1-1 (Invited) **InAlN/GaN HEMTs: Recent Progress and Challenges for the Future** *J. Kuzmik[1,2], [1]Slovak Academy of Sciences and [2]TU Vienna (Slovakia)*	**13:30 BL-1-1** **Determination of Carrier Lifetime in Bulk-heterojunction Solar Cells by Continuous-wave Photoinduced Absorption Spectroscopy** *Y. Terada[1], W. Shinke[1], T. Kobayashi[1], T. Nagase[1] and H. Naito[1,2], [1]Osaka Prefecture Univ. and [2]CREST-JST (Japan)*	**13:30 B-1-1** **Solution-processed small molecular phosphorescent organic light emitting devices with a mixed single layer** *Z. Wang, S. Naka and H. Okada, Univ. of Toyama (Japan)*	**13:30 C-1-1 (Invited)** **TSV and Cu-Cu direct bonding: two key technologies for High Density 3D** *N. Sillon, H. Ben Jamaa, P. Leduc, L. Di Cioccio, S. Cheramy and T. Signamarcheix, CEA-Leti, Minatec campus (France)*	**13:30 D-1-1** **Simple and Efficient MASTAR Threshold Voltage and Subthreshold Slope Models for Double Gate Structures** *J. Lacord[1,2], J. L. Huguenin[1,2], G. Ghibaudo[2], T. Skotnicki[1] and F. Boeuf[1], [1]STMicroelectronics and [2]IMEP-LAHC (France)*	**13:30 E-1-1 (Invited)** **Investigation of the Electrical Properties of Ge/High-k Gate Stack: GeO_2 VS Si-cap** *J. Mitard, F. Bellenger, L. Witters, B. De Jaeger, B. Vincent, L. Nyns, K. Martens, E. Vrancken, G. Wang, D. Lin, R. Loo, M. Caymax, K. De Meyer, M. Heyns and N. Horiguchi, IMEC (Belgium)*	**13:30 F-1-1 (Invited)** **Magnetoresistive Random Access Memory with Spin Transfer Torque Write (Spin RAM) -Present and Future-** *H. Ohno, Tohoku Univ. (Japan)*
14:00 A-1-2 **High-Power and High-Gain S-band AlGaN/GaN HFETs with Source Field Plates on Si Substrate** *S. Nakazawa, N. Tsurumi, M. Nishijima, Y. Anda, M. Ishida, T. Ueda and T. Tanaka, Panasonic Corp. (Japan)*	**13:45 BL-1-2** **Analysis of anomalous discharging processes in pentacene/C_{60} double-layer organic solar cell** *X. Chen, D. Taguchi, K. Lee, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)*	**13:45 B-1-2** **Hole Injection Enhancement in Organic Light-emitting Diodes by Introducing an Au Nanoparticle Layer** *D. Wang and K. Fujita, Kyushu Univ. (Japan)*	**14:00 C-1-2** **Fabrication of Graphene Directly on SiO_2 without Transfer Processes by Annealing Sputtered Amorphous Carbon** *M. Sato[1], M. Inukai[2], E. Ikenaga[2], T. Muro[2] S. Ogawa[3], Y. Takakuwa[3], H. Nakano[1], A. Kawabata[1], M. Nihei[1] and N. Yokoyama[1], [1]AIST/GNC, [2]JASRI/SPring-8 and [3]Tohoku Univ. (Japan)*	**13:50 D-1-2** **Accurate and Ready-to-use Parasitic Capacitances Models for Advanced 2D/3D CMOS Device Structure Comparison** *J. Lacord[1,2], D. Hoguet[1], D. Rideau[1], G. Ghibaudo[2] and F. Boeuf[1], [1]STMicroelectronics and [2]IMEP-LAHC (France)*	**14:00 E-1-2** **1.2 nm-EOT Al_2O_3/Ge Gate Stack with GeO_x-free Interface** *T. Tabata[1,2], C. H. Lee[1,2], T. Nishimura[1,2], S. K. Wang[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]CREST-JST (Japan)*	**14:00 F-1-2** **Studies on Static Noise Margin and Scalability for Low-Power and High-Density Nonvolatile SRAM using Spin-Transfer-Torque (STT) MTJs** *T. Ohsawa, F. Iga, S. Ikeda, T. Hanyu, H. Ohno and T. Endoh, Tohoku Univ. (Japan)*
14:15 A-1-3 **RF power characteristics of high-thermal-efficiency AlGaN/GaN HEMTs on diamond** *K. Hirama, M. Kasu and Y. Taniyasu, NTT Basic Res. Labs. NTT Corp. (Japan)*	**14:00 BL-1-3** **Probing electric field distribution of P3HT in ITO/PI/P3HT/Au by using EFISHG measurement** *R. Miyazawa, D. Taguchi, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)*	**14:00 B-1-3** **Improvement on Electroluminescence of Red Organic Light Emitting Diode by Doping with Sensitizers** *S. H. Yang, C. H. Chuang, S. C. Huang and P. J. Shih, National Kaohsiung Univ. of Applied Sciences (Taiwan)*	**14:20 C-1-3** **Initial Growth Observation of Multilayer Graphene on SiO_2/Si substrates Using Raman Spectroscopy and XPS** *Y. Ojiro[1], S. Ogawa[1], M. Inukai[2], M. Sato[1,3], E. Ikenaga[2], T. Muro[2], M. Nihei[3], Y. Takakuwa[1] and N. Yokoyama[3], [1]Tohoku Univ., [2]JASRI/SPring-8 and [3]AIST/GNC (Japan)*	**14:10 D-1-3** **An Accurate Prediction Model of Temperature Dependent Current Mismatch in All Inversion and Influence of Subthreshold Hump on Mismatch Characteristics** *K. Sakakibara and K. Arimoto, Renesas Electronics Corp. (Japan)*	**14:20 E-1-3** **Effective Passivation of Interface Dipole in TiN-Gate Ge-MOS Capacitor with Ultrathin SiO_2/GeO_2 Bilayer by Nitrogen Incorporation** *K. Sakamoto, Y. Iwamura, K. Yamamoto, H. Yang, D. Wang and H. Nakashima, Kyushu Univ. (Japan)*	**14:20 F-1-3** **A Study for Adopting PMOS Memory Cell for 1T1R STT-RAM with Asymmetric Switching Current MTJ** *H. Koike and T. Endoh, Tohoku Univ. (Japan)*

Opening & Plenary Sessions (WINC HALL)

Opening Session
Chair: M. Hori, Nagoya Univ.

9:30
Welcome Address
S. Zaima, Nagoya Univ.

Non-Technical Plenary Session
Chair: T. Fukui, Hokkaido Univ.

9:40 PL-1-1
Social Contribution and Next Giant Leap of Semiconductors M. Fukuma, Semiconductor Industry Research Institute Japan, Japan

SSDM Award / Paper Award Presentation
S. Zaima, Nagoya Univ.

Technical Plenary Sessions
Chair: T. Fukui, Hokkaido Univ.

10:45 PL-2-1
A Car Guy's Expectations for Electronics M. Yoshida, Toyota Motor Corporation, Japan

11:30 PL-2-2
Electronics Proliferation through Diversification.
Tsu-Jae King Liu, University of California at Berkeley, USA

12:15-13:30 Lunch

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
GH-1: Image Sensor and MEMS Technology (1) (Area 5&11) (13:30-15:10) Chairs: S. Sugawa (Tohoku Univ.) T. Tokuda (NAIST)		**I-1: Optical Link and Related Devices (Area 7)** (13:30-15:15) Chairs: Y. Ishikawa (Univ. of Tokyo) N. Iizuka (Toshiba Corp.)		**K-1: CNT Property (Area 13)** (13:30-15:15) Chairs: S. Akita (Osaka Prefecture Univ.) Y. Ohno (Nagoya Univ.)	**L-1: Quantum Well& III-V Solar Cell (Area 14)** (13:30-15:15) Chairs: F. Finger (FZ Julich) N. Kojima (Toyota Technological Inst.)	**M-1: Nitrides (Area 8)** (13:30-15:15) Chairs: T. Nagata (NIMS) K. Hara (Shizuoka Univ.)	
13:30 GH-1-1 (Invited) **High Speed Vision for Gesture UI, Dynamic Image Control and Visual Feedback** *M. Ishikawa, Univ. of Tokyo (Japan)*		**13:30 I-1-1 (Invited)** **Lens-integrated surface-emitting DFB laser arrays for short-reach optical links** *K. Adachi[1,2], K. Shinoda[1,2], T. Kitatani[1,2], Y. Matsuoka[1], T. Sugawara[1] and S. Tsuji[1,2], [1]Hitachi.Ltd. and [2]PETRA (Japan)*		**13:30 K-1-1 (Invited)** **Carbon Nanotube Clamped Metal Atomic Chain: Fabrication, Structure and Property** *D. M. Tang, L. C. Yin, C. Liu and H. M. Cheng, Chinese Academy of Sciences (China)*	**13:30 L-1-1 (Invited)** **Quantum Well Solar Cells** *(UK)*	**13:30 M-1-1 (Invited)** **Progress in Nonpolar and Semipolar GaN-base Materials and Devices** *J.S. Speck, Univ. of California, Santa Barbara (USA)*	
14:00 GH-1-2 **A 2-D Optical Pulse Receiver/ Imager with Two-Port Pixels for Simultaneously Producing Image and Communication Signals** *S. Kawahito[1], S. Itoh[1], Y. Iwama[1], I. Takai[2], M. Andoh[2], K. Yasutomi[1] and K. Kagawa[1], [1]Shizuoka Univ. and [2]Toyota Central R&D Labs, Inc. (Japan)*		**14:00 I-1-2** **Performance of Low-Loss and Low-Cost Optoelectronic Module with Polynorbornene Waveguide for 10-Gbps Data Transmission.** *Y. Ito[1], S. Terada[1], S. Arai[1], M. Fujiwara[1], T. Mori[1], K. Choki[1], T. Fukushima[2] and M. Koyanagi[2], [1]Sumitomo Bakelite Co., Ltd. and [2]Tohoku Univ. (Japan)*		**14:00 K-1-2** **Fabrication of Carbon Nanowalls on Carbon Fiber Paper** *S. Mitsuguchi[1], M. Hiramatsu[1], H. Kondo[2], M. Hori[2] and H. Kano[3], [1]Meijo Univ., [2]Nagoya Univ. and [3]NU Eco Eng. Co., LTD. (Japan)*	**14:00 L-1-2** **Non-Radiative Carrier Recombination in the Strain-Balanced InGaAs/ GaAsP Multiple Quantum Wells for Solar Cell Application** *T. Aihara[1], Y. Nakano[1], A. Fukuyama[1], Y. Wang[2], M. Sugiyama[2], Y. Nakano[2] and T. Ikari[1], [1]Univ. of Miyazaki and [2]Univ. of Tokyo (Japan)*	**14:00 M-1-2** **Tilted domain and indium content of MOVPE-grown InGaN layer on *m*-plane GaN substrate** *K. Shojiki[1], T. Hanada[1,2], T. Shimada[1], Y. Liu[1,2], R. Katayama[1,2] and T. Matsuoka[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)*	
14:20 GH-1-3 **Improved Near-Infrared Sensitivity for a Side-Illuminated Photo Sensor** *T. Ariyoshi, N. Uryu, A. Baba and Y. Arima, Kyushu Inst. of Tech. (Japan)*		**14:15 I-1-3** **Low Voltage InGaAs/InAlAs Quantum Well Mach-Zehnder Modulator with Single Microring Resonator** *H. Kaneshige, Y. Ueyama, H. Yamada, T. Arakawa and Y. Kokubun, Yokohama National Univ. (Japan)*		**14:15 K-1-3** **Alignment of Carbon Nanotubes on Sapphire Surfaces with Strong Interactions** *S. Jeong[1] and A. Oshiyama[2], [1]Chonbuk Nat. Univ. and [2]Univ. of Tokyo (Korea)*	**14:15 L-1-3** **Kinetics of strain relaxation in lattice-mismatched III-V heteroepitaxy** *T. Sasaki[1], K. Shimomura[1], H. Suzuki[2], M. Takahasi[3], I. Kamiya[1], Y. Ohshita[1] and M. Yamaguchi[1], [1]Toyota Tech. Inst., [2]Univ. of Miyazaki and [3]JAEA (Japan)*	**14:15 M-1-3** **Effect of Phase Purity on Dislocation Density of PR-MOVPE-Grown InN** *T. Iwabuchi[1], Y. Liu[1,2], T. Kimura[1,2], Y. Zhang[1,2], K. Prasertsuk[1], R. Katayama[1,2] and T. Matsuoka[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)*	

Wednesday, September 28

5F Hall 1

A-1: GaN FET Technologies (Area 6)

14:30 A-1-4
Improvement of Current Collapse in Deeply Recessed Gate AlGaN/GaN High Electron Mobility Transistors without Field Modulating Structure
A. Imai, K. Yamanaka, Y. Suzuki, T. Nanjo, M. Suita, K. Shiozawa, Y. Abe, E. Yagyu and A. Shima, Mitsubishi Electric Corp. (Japan)

14:45 A-1-5
Temperature Dependence and Current Collapse of AlGaN/GaN Super Heterojunction Field Effect Transistor
S. Yagi[1], S. Hirata[1], Y. Sumida[1], A. Nakajima[2], H. Kawai[1] and E. M. Sankara Narayanan[2], [1]POWDEC. K. K. and [2]Univ. Sheffield (Japan)

15:00 A-1-6
Sputtered amorphous AlN gate dielectric for AlGaN/GaN metal-insulator-semiconductor heterojunction field-effect transistor
H. A. Shih, M. Kudo, M. Akabori and T. Suzuki, JAIST (Japan)

A-2: III-V HBTs and FETs (Area 6)
(15:40-16:55)
Chairs: K. Maezawa (Univ. of Toyama)
Y. Miyamoto (Tokyo Tech)

15:40 A-2-1 (Invited)
Extending the Bandwidth and Functionality of High Performance InP HBT Technologies
M. Urteaga[1], R. Pierson[1], J. Bergman[1], D. H. Kim[1], P. Rowell[1], B. Brar[1] and M. Rodwell[2], [1]Teledyne Scientific Corp. and [2]Univ. of California, Santa Barbara (USA)

16:10 A-2-2
Low-turn-on voltage heterojunction bipolar transistors with a C-doped $In_xGa_{1-x}As_{1-y}Sb_y$ base grown by metalorganic chemical vapor deposition
T. Hoshi, H. Sugiyama, H. Yokoyama, K. Kurishima and M. Ida, NTT Corp. (Japan)

5F Hall 2

BL-1: Organic Photovoltaics (1) (Area 10&14)

14:15 BL-1-4
Designing of Organic Solar Cell Module for Obtaining Maximum Performance
H. Ogo, T. Miyadera, T. Taima, A. Masuda and Y. Yoshida[1], AIST (Japan)

14:30 BL-1-5
In situ monitoring of organic solar cells during thermal annealing
K. T. Hung, C. Y. Hsiao, H. T. Wu, S. W. Fu, H. J. Chen and C. F. Shih, National Cheng Kung Univ. (Taiwan)

14:45 BL-1-6
RF-Sputtered High-Mobility Indium Molybdenum Thin Films for Organic Solar Cell Applications
H. J. Chang, W. F. Chen, S. S. Cheng, K. M. Huang, T. H. Huang, C. L. Ho and M. C. Wu, National Tsing Hua Univ. (Taiwan)

15:00 BL-1-7
Comprehensive Studies of Solvent Annealing on Organic Photovoltaics
H. T. Wu, C. Y. Hsiao, K. T. Hung, H. J. Chen, S. W. Fu, S. H. Wu and C. F. Shih, National Cheng Kung Univ. (Taiwan)

BL-2: Organic Photovoltaics (2) (Area 10&14)
(15:40-17:25)
Chairs: S. H. Su (I-Shou Univ.)
N.Kojima (Toyota Technological Inst.)

15:40 BL-2-1
Optimization of Carrier Collection Structure in Graded Organic Solar Cells
T. Horioka[1], Z. Wang[1], S. Naka[1] and H. Okada[1,2], [1]Univ. of Toyama and [2]Center for Basic Res. and Development in Natural Sciences (Japan)

15:55 BL-2-2
Solution Processable Thin Film Organic Photovoltaic Cells based on Far Red Sensitive Soluble Squaraine Dyes
S. S. Pandey, T. Mizuno, S. K. Das, Y. Ogomi and S. Hayase, Kyushu Inst. of Tech. (Japan)

10F 1002

B-1: OLEDs (Area 10)

14:15 B-1-4
White Organic Light-Emitting Diodes Combining Blue Organic Light-Emitting Diodes with a $Sr_2SiO_4:Eu^{3+}$ Color Conversion Layer
S. H. Su, W. Y. Wang and M. Yokoyama, I-Shou Univ. (Taiwan)

14:30 B-1-5
Pattern Formation of Phosphorescent Polymer Thin Films by Spin-Coated Photoreactive Monomer Films
D. Miyagawa, M. Muroyama, K. Tanaka and H. Usui, Tokyo Univ. of Agri. and Tech. (Japan)

14:45 B-1-6
Device Parameters Determination by Novel Schottky Model Fitting for Organic Light-Emitting Diodes (OLEDs)
T. Hirai, K. Weber, M. Bown and K. Ueno, CSIRO (Australia)

15:00 B-1-7 (Late News)
Three Terminal Nano-Scale Electrode for Molecular Transistor Evaluation
K. Tsutsui, M. Morita, M. Tokuda, H. Takagi, Y. Ito and Y. Wada, Toyo Univ. (Japan)

B-2: Organic device fabrication process and interface control (Area 10)
(15:40-17:25)
Chairs: H. Usui (Tokyo Univ. of Agri. & Tech.)
K. Takimoto (Canon Inc.)

15:40 B-2-1 (Invited)
Nanotransfer Direct Printing Methods
M. M. Sung, Hanyang Univ. (Korea)

16:10 B-2-2
Work Function controlled Zn:Cu electrode for all-printed polymer diode
M. Yoshida, S. Uemura, H. Tokuhisa, N. Takada and T. Kamata, AIST (Japan)

10F 1003

C-1: Future Interconnect (Area 2)

14:40 C-1-4
STC: Single-Tube Characterization Methodology for Experimental and Analytical Evaluation of Carbon Nanotube Synthesis
H. Y. Chen, A. Lim, L. S. Liyanage, C. Beasley, N. Patil, H. Wei, S. Mitra and H. S. P. Wong, Stanford Univ. (USA)

15:00 C-1-5 (Late News)
Effect of H_2 gas addition on Si Oxidation Process with Ar and O_2 Mixture Surface Wave Plasma
K. Takeda and M. Hori, Nagoya Univ. (Japan)

11F 1101

D-1: Modeling and Circuits (Area 3)

14:30 D-1-4
A Stacked Inverter-based CMOS Power Amplifier in 65nm CMOS Process
H. Kiumarsi, Y. Mizuochi, H. Ito, N. Ishihara and K. Masu, Tokyo Tech (Japan)

14:50 D-1-5
Design of Power-Efficient 130GHz Common-Source Amplifiers
K. Katayama[1], M. Motoyoshi[2], K. Takano[2] and M. Fujishima[1], [1]Hiroshima Univ. and [2]Univ. of Tokyo (Japan)

D-2: Device & Characteristics (Area 3)
(15:40-17:00)
Chairs: K. Okano (Toshiba Corp.)
F. Boeuf (STMicroelectronics)

15:40 D-2-1
Current Drive Enhancement of Strained Ge nMISFET with SiGe Stressors by Uniaxial Tensile Stress
Y. Kamimuta, Y. Moriyama, K. Ikeda, M. Oda and T. Tezuka, MIRAI-Toshiba (Japan)

16:00 D-2-2
Experimental Study of Si Monolayers for Future Extremely-Thin SOIs (ETSOIs): Phonon Confinement Effects and Strain due to Si Bending
T. Mizuno[1], K. Tobe[1], Y. Maruyama[1] and T. Sameshima[2], [1]Kanagawa Univ. and [2]Tokyo Univ. of Agri. and Tech. (Japan)

11F 1102

E-1: Ge-MOS (Area 1)

14:40 E-1-4
Defect Control in Germanium Oxide Film Thermally Grown on Germanium Substrate
Y. Oniki and T. Ueno, Tokyo Univ. of Agri. and Tech. (Japan)

15:00 E-1-5
High-Electron-Mobility Ge n-MOSFET with TiN Metal Gate
T. Yamanaka, K. Yamamoto, K. Sakamoto, H. Yang, D. Wang and H. Nakashima, Kyushu Univ. (Japan)

E-2: Characterization in Gate Stacks (Area 1)
(15:45-17:15)
Chairs: S. Tsujikawa (Sony Corp.)
H. Nohira (Tokyo City Univ.)

15:45 E-2-1 (Invited)
In depth characterization of electrical effects of dopants (Al, La, Mg, N) in high-k/metal gate stacks
G. Reimbold[1], M. Cassé[1], X. Garros[1], C. Leroux[1], M. Charbonnier[1], L. Brunet[2,1], S. Baudot[2,1], P. Caubet[2], C. Fenouillet-Béranger[1,2], F. Andrieu[1], O. Weber[1], P. Perreau[1,2] and F. Martin[1], [1]CEA-LETI/MINATEC and [2]STMicroelectronics (France)

16:15 E-2-2
Role of Al atoms in $(TaC)_{1-x}Al_x$ gate electrode on V_{fb} for HfO_2 gate stack
M. Kimura[1], T. Nabatame[2], H. Yamada[1], A. Ohi[2], T. Chikyow[2] and T. Ohishi[1], [1]Shibaura Inst. of Tech. and [2]MANA Foundry and MANA Advanced Device Materials Group, National Inst. for Materials Sci. (Japan)

11F 1103

F-1: STT-RAM (Area 4)

14:40 F-1-4
Novel 2step Writing Method for STT-RAM to Improve Switching Probability and Write Speed
F. Iga, Y. Suzuki, T. Ohsawa, S. Ikeda, T. Hanyu, H. Ohno and T. Endoh, Tohoku Univ. (Japan)

F-2: FeRAM/DRAM/SRAM (Area 4)
(15:40-17:30)
Chairs: K. Hamada (Elpida Memory, Inc.)
T. Eshita (Fujitsu Semiconductor Ltd.)

15:40 F-2-1 (Invited)
An Overview of Embedded Ferroelectric Memory Technology
K. R. Udayakumar, T. S. Moise, S. R. Summerfelt, J. Rodriguez, M. Ball, L. Wang, H. McAdams and S. Madan, Texas Instruments Inc. (USA)

16:10 F-2-2
Data Disturbance-free NAND-type Ferroelectric-gate Thin Film Transistor Array using Solution-processed ITO and Stacked (BLT/PZT) Gate Insulator
B. N. Q. Trinh[1], T. Miyasako[1], T. Kaneda[1], P. V. Thanh[2], P. T. Tue[2], E. Tokumitsu[1,3] and T. Shimoda[1,2], [1]JST, [2]JAIST and [3]Tokyo Tech (Japan)

Coffee Break

Wednesday, September 28

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
GH-1: Image Sensor and MEMS Technology (1) (Area 5&11)		**I-1: Optical Link and Related Devices (Area 7)**		**K-1: CNT Property (Area 13)**	**L-1: Quantum Well& III-V Solar Cell (Area 14)**	**M-1: Nitrides (Area 8)**	
14:40 GH-1-4 (Invited) **RF MEMS Switch Technology in OMRON** *T. Seki, Y. Uno, K. Narise, T. Masuda, K. Inoue and F. Sato, OMRON Corp. (Japan)*		**14:30 I-1-4** **Magnetically Controllable Optical Intensity and Mode Redistribution in Semiconductor Active Optical Isolators** *H. Shimizu, K. Uehara and K. Tazawa, Tokyo Univ. of Agri. & Tech. (Japan)*		**14:30 K-1-4** **Sensing Property of Horizontally Aligned Carbon Nanotube Field-Effect Transistor on Quartz Substrate** *S. Okuda, S. Okamoto, Y. Ohno, K. Maehashi, K. Inoue and K. Matsumoto, Osaka Univ. (Japan)*	**14:30 L-1-4** **InGaN/GaN solar cells grown on wet-etched patterned sapphire substrates** *C. H. Yang, Y. C. Yao, C. M. Cheng, M. H. Lee and Y. J. Lee, National Taiwan Normal Univ. (Taiwan)*	**14:30 M-1-4** **Surface Supersaturation in Nucleus and Spiral Growth of GaN in MOVPE** *T. Akasaka, Y. Kobayashi and M. Kasu, NTT Basic Res. Labs. (Japan)*	
		14:45 I-1-5 **An inverted InAlAs/InGaAs avalanche photodiode with low-high-low field profile** *M. Nada, Y. Muramoto, H. Yokoyama, N. Shigekawa, T. Ishibashi and S. Kodama, NTT Photonics Labs. (Japan)*		**14:45 K-1-5** **Estimation of height of defect-induced barriers in metallic CNTs** *Y. Okigawa, Y. Ohno, S. Kishimoto and T. Mizutani, Nagoya Univ. (Japan)*	**14:45 L-1-5** **Effect of Thermal Stress on a N-related Recombination Center in GaAsN Grown by Chemical Beam Epitaxy** *B. Bouzazi, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Tech. Inst. (Japan)*	**14:45 M-1-5** **Growth of Nitrogen-Polar 2H-AlN on Step-Height-Controlled 6H-SiC (000-1) Substrate by Molecular-Beam Epitaxy** *H. Okumura, T. Kimoto and J. Suda, Kyoto Univ. (Japan)*	
		15:00 I-1-6 **Responsivity Characteristics of InP/InGaAs Heterojunction Phototransistors with Strained InAs/InGaAs Multiquantum Well Absorption Layers** *H. Egusa[1], H. Fukano[1], S. Taue[1], T. Sato[1] and M. Mitsuhara[2], [1]Okayama Univ. and [2]NTT Photonics Labs. (Japan)*		**15:00 K-1-6** **Room Temperature Single Charge Memory by Carbon Nanotube Transistor With SiN_x /Al_2O_3 Wrapped Double Gate Insulator Layers** *T. Kamimura[1, 2, 3], Y. Hayashi[2, 3] and K. Matsumoto[1, 2, 3], [1]Osaka Univ., [2]CREST-JST and [3]AIST (Japan)*	**15:00 L-1-6** **2-dimensional mapping of power consumption due to series resistance evaluated by simulator for concentrator photovoltaic module** *Y. Ota and K. Nishioka, Univ. of Miyazaki (Japan)*	**15:00 M-1-6** **A Novel Chemical Lift-Off Process based on Embedded Nano-rods Template** *S. S. Yen, W. Y. Chen, J. R. Chang, S. P. Chang, P. M. Tu, Y. C. Hsu, Y. J. Li, Y. C. Chen, K. P. Sou and C. Y. Chang, National Chiao Tung Univ. (Taiwan)*	

Coffee Break

GH-2: Image Sensor and MEMS Technology (2) (Area 5&11) (15:40-17:20) Chairs: K. Sawada (Toyohashi Univ. of Tech.) H. Morimura (NTT Microsystem Integration Labs.)		**I-2: Photonic Crystals (Area 7)** (15:40-17:10) Chairs: M. Tokushima (AIST) S. Saito (Hitachi Ltd.)		**K-2: CNT Device (Area 13)** (15:40-17:25) Chairs: K. Maehashi (Osaka Univ.) S. Sato (AIST)	**L-2: Thin-Film Silicon Solar Cells (Area 14)** (15:40-17:25) Chairs: A. Masuda (AIST) K. Ohdaira (JAIST)	**M-2: Oxides (Area 8)** (15:40-17:25) Chairs: K. Hara (Shizuoka Univ.) T. Nagata (NIMS)	
15:40 GH-2-1 (Invited) **WLAN(IEEE 802.11n)/m-WiMAX(IEEE 802.16e) 2x2 MIMO FRONT-END MODULE USING MEMS & LTCC TECHNOLOGY** *K. Chun[1], S. Kang[1], Y. Jang[1], J. C. Kim[2], C. S. Kim[3] and I. S. Song[3], [1]Soeul National Univ., [2]Korea Electronics Tech. Inst. and [3]Samsung Advanced Inst. of Tech. (Korea)*		**15:40 I-2-1 (Invited)** **Photonic Crystal Devices Fabricated by CMOS-Compatible Process** *T. Baba[1, 2], [1]Yokohama National Univ. and [2]CREST-JST (Japan)*		**15:40 K-2-1** **Resistance distribution of CNT network measured by conductive atomic force microscopy** *K. Housayama, Y. Okigawa, S. Kishimoto, Y. Ohno and T. Mizutani, Nagoya Univ. (Japan)*	**15:40 L-2-1 (Invited)** **Materials for thin film silicon solar cells** *F. Finger, R. Carius, T. Chen, A. Lambertz and V. Sminov, IEK5 - Photovoltaik, Forschungszentrum Jülich (Germany)*	**15:40 M-2-1 (Invited)** **Multi-dimensional Nanostructured Oxide Devices** *H. Taknaka, A. Ono, T. Kusizaki, K. Fujiwara and A. Hattori, Osaka Univ. (Japan)*	
16:10 GH-2-2 **Manipulation of Dispersed Magnetic Beads for On-chip Immunoassay** *T. Ishikawa[1, 2], J. S. Lee[1] and R. Miyake[1, 2], [1]Hiroshima Univ. and [2]CREST-JST (Japan)*		**16:10 I-2-2** **An Epitaxially Regrown GaAs Based Photonic Crystal Surface Emitting Laser** *D. M. Williams[1], K. M. Groom[1], B. J. Stevens[1], Q. Jiang[1], D. T. D. Childs[1], R. J. Taylor[1], S. Khamas[1], R. A. Hogg[1], N. Ikeda[2] and Y. Sugimoto[2], [1]Univ. of Sheffield and [2]NIMS (UK)*		**15:55 K-2-2** **Theoretical Study of AC Response of Defective Carbon Nanotubes:Tube Diameter Dependence** *D. Hirai[1], T. Yamamoto[1,2] and S. Watanabe[1], [1]Univ. of Tokyo and [2]Tokyo Univ. of Sci. (Japan)*	**16:10 L-2-6** **Effect of Hydrogen Radical-Injection on Growth Property and Crystallinity of Microcrystalline Silicon Thin Film** *Y. Abe, A. Fukushima, Y. Lu, K. Takeda, H. Kondo, K. Ishikawa, M. Sekine and M. Hori, Nagoya Univ. (Japan)*	**16:10 M-2-2** **Crystal growth and optical characterizations of nonpolar m-plane ZnO on the m-plane sapphire substrate by PLD** *C. C. Kuo[1], B. H. Lin[1,2], W. R. Liu[2], C. H. Hsu[1,2] and W. F. Hsieh[1], [1]National Chiao Tung Univ. and [2]National Synchrotron Radiation Research Center (Taiwan)*	

Wednesday, September 28

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
A-2: III-V HBTs and FETs (Area 6)	**BL-2: Organic Photovoltaics (2) (Area 10&14)**	**B-2: Organic device fabrication process and interface control (Area 10)**		**D-2: Device & Characteristics (Area 3)**	**E-2: Characterization in Gate Stacks (Area 1)**	**F-2: FeRAM/DRAM/SRAM (Area 4)**
16:25 A-2-3 **Effects of Plasma-PH_3 passivation on Mobility Degradation Mechanisms and Current Conduction Mechanisms of $In_{0.53}Ga_{0.47}As$ N-MOSFET** *A. B. S Sumarlina[1,2], H. J. Oh[1], A. Du[2] and S. J. Lee[1], [1]National Univ. of Singapore and [2]GLOBALFOUNDRIES Singapore Pte.Ltd. (Singapore)*	**16:10 BL-2-3** **Highly Efficient Organic Solar Cell Employing a Solution Processed Hole Transporting Layer** *W. K. Lin, S. H. Su, Y. F. Lin, J. R. Wang, J. L. Huang and M. Yokoyama, I-shou Univ. (Taiwan)*	**16:25 B-2-3** **Interface Control of ITO and Spin-Coated Polymer by Reactive Self-Assembled Monolayer** *S. H. Kim[1], H. Ohtsuka[1], M. C. Tria[2], R. C. Advincula[2] and H. Usui[1], [1]Tokyo Univ. of Agri. and Tech. and [2]Univ. Houston (Japan)*		**16:20 D-2-3** **Lateral Source Relaxed/Strained Layer Heterostructures for Ballistic CMOS: Physical Relaxation Mechanism for Strained Layers by O^+ Ion Implantation** *T. Mizuno, J. Takehi and S. Tanabe, Kanagawa Univ. (Japan)*	**16:35 E-2-3** **Impurity Profile Extraction of Semiconductor Devices from STM Tunneling Currents by Current Continuity Based Simulation** *K. Fukuda[1], M. Nishizawa[1], T. Tada[1], L. Bolotov[2], K. Suzuki[3], S. Sato[3], H. Arimoto[1] and T. Kanayama[1], [1]AIST, [2]Univ. of Tsukuba and [3]Fujitsu Semiconductor Ltd. (Japan)*	**16:30 F-2-3** **Process Development of ALD-Rutile-TiO_2/Ru(O_x) for DRAM MIMcap Application and its Leakage Mechanism Analysis** *K. Tomida[1], M. Popovici[1], J. Swerts[1], W. C. Wang[2], B. Kaczer[1], M. A. Pawlak[1], S. Van Elshocht[1], M. S. Kim[1], I. Debusschere[1], V. V. Afanasiev[2], L. Altimime[1] and J. A. Kittl[1], [1]IMEC and [2]Catholic Univ. of Leuven (Belgium)*
16:40 A-2-4 **$In_{0.53}Ga_{0.47}As$ Channel N-MOSFETs with Shallow Metallic S/D Extension** *Z. Zhu, X. Gong, Ivana and Y. C. Yeo, National Univ. of Singapore (Singapore)*	**16:25 BL-2-4** **Sodium Doping at CuPc/C60 Interface for Photovoltaic Application** *H. J. Chen, K. T. Hung, C. Y. Hsiao, S. W. Fu, H. T. Wu, S. H. Wu and C. F. Shih, National Cheng Kung Univ. (Taiwan)*	**16:40 B-2-4** **Field induced selective growth of organic conductive wires and molecular break junction by Joule heating** *M. Sakai[1], Y. Urabe[1], H. Yamauchi[1], M. Nakamura[1,2] and K. Kudo[1], [1]Chiba Univ. and [2]NAIST (Japan)*		**16:40 D-2-4** **Recovery Characteristic of Anomalous Stress Induced Leakage Current of 5.6nm Oxide Films** *T. Inatsuka, Y. Kumagai, R. Kuroda, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)*	**16:55 E-2-4** **Influence of channel area scaling on Weibull distribution of TDDB for poly-Si channel FET** *I. Hirano, M. Saito, T. Numata and Y. Mitani, Toshiba Corp. (Japan)*	**16:50 F-2-4** **Optimization and Variation Studies of BJT-based Ultra Thin Body Capacitorless DRAM Cell** *M. H. Cho, C. Shin and T. J. King Liu, UC, Berkeley (USA)*
	16:40 BL-2-5 **Charge trapping in organic solar cells with plasmonic silver nanoparticles** *M. Weis[1], K. Vegso[1], P. Siffalovic[1], M. Jergel[1], E. Majkova[1], K. Lee[2], X. Chen[2], L. Zhang[2], D. Taguchi[2], T. Manaka[2] and M. Iwamoto[2], [1]Slovak Academy of Sci. and [2]Tokyo Tech (Slovakia)*	**16:55 B-2-5** **Bulk crystal growth of organic semiconductors for thermoelectric applications** *Y. Ikuta, Y. Tsuchida, N. Muraya, T. Nagahama and T. Shimada, Hokkaido Univ. (Japan)*				**17:10 F-2-5** **A Compact Half Select Disturb Free SRAM Cell with Stacked Vertical MOSFET** *H. Na[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)*
	16:55 BL-2-6 **Effects of the Film Thickness on the Photocurrent Generation from Polythiophene-fullerene Thin films Containing of Silver Nanoparticles** *J. You[1], Y. Takahashi[1], H. Yonemura[1], T. Akiyama[2] and S. Yamada[1], [1]Kyushu Univ. and [2]Univ. of Shiga Prefecture (Japan)*	**17:10 B-2-6** **Geometric characterization of superoleophobic film** *K. Tsuji and S. Shiratori, Keio Univ. (Japan)*				
	17:10 BL-2-7 **Improvement of Short-Circuit Current in Plasmonic Organic Solar Cells Based on Grating Structures** *A. Baba, D. Murashima, N. Aoki, K. Shinbo, K. Kato and F. Kaneko, Niigata Univ. (Japan)*					

Banquet/Young Researcher Award (16F, Tower Ball Room, Marriott Associa Hotel)

Wednesday, September 28

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
GH-2: Image Sensor and MEMS Technology (2) (Area 5&11)		**I-2: Photonic Crystals (Area 7)**		**K-2: CNT Device (Area 13)**	**L-2: Thin-Film Silicon Solar Cells (Area 14)**	**M-2: Oxides (Area 8)**	
16:30 GH-2-3 **In-pixel type small-scale integrated C-V converter with chopper stabilized CMOS inverter** *R. Kodama[1], H. Miyao[1], M. Ishida[1] and H. Takao[1,2], [1]Toyohashi Univ. of Tech. and [2]Kagawa Univ. (Japan)*		**16:25 I-2-3** **Photonic Crystal Band-edge Laser on a Flexible Substrate** *K. S. Hsu[1,2], T. T. Chiu[1,2] and M. H. Shih[1,2], [1]RCAS and [2]National Chiao Tung Univ. (Taiwan)*		**16:10 K-2-3** **Argon Ion Bombardment to Improve Contacts in Solution-Processed Single-Walled Carbon Nanotube Thin Film Transistor** *X. Yi, G. Nakagawa, H. Ozawa, T. Fujigaya, N. Nakashima and T. Asano, Kyushu Univ. (Japan)*	**16:25 L-2-3** **Development of the TCO Layer for Nanocrystalline Cubic Silicon Carbide / Silicon Heterojunction Solar Cells with Aluminum Oxide Passivation Layers** *J. Irikawa, S. Miyajima, T. Watahiki and M. Konagai, Tokyo Tech (Japan)*	**16:25 M-2-3** **Processing Induced *Pre-Existing Vacated (Empty) O-atom* Defect Sites in Remote Plasma Deposited GeO_2 and SiO_2 Gate Dielectrics** *G. Lucovsky, J. Kim, K. Wu, D. Zeller, B. Papas and J. L. Whitten, North Carolina State Univ. (USA)*	
16:50 GH-2-4 **A Monolithically-Integrated, Batch Post-Processed 17.8 V Silicon Solar Cell for Remote MEMS Driving** *I. Mori, S. Morishita, M. Kubota, K. Watanabe and Y. Mita, Univ. of Tokyo (Japan)*		**16:40 I-2-4** **Large Area of Ultraviolet GaN-based Photonic Quasicrystal Laser** *C. C. Chen[1], M. Y. Kuo[2], C. H. Chiu[1], P. M. Tu[1], M. H. Shih[2], S. P. Chang[1], J. K. Huang[1], H. C. Kuo[1], H. W. Zan[1] and C. Y. Chang[1], [1] National Chiao Tung Univ. and [2]RCAS (Taiwan)*		**16:25 K-2-4** **Optimization of Source/Drain Doping Concentration of Carbon Nanotube FETs to Suppress Off-state Leakage Current while Keeping Ideal On-state Current** *B. P. Algul and K. Uchida, Tokyo Tech (Japan)*	**16:40 L-2-4** **Embedded Biomimetic Nanostructures for Enhanced Optical Absorption in Thin-Film Solar Cells** *H. W. Han[1], M. A. Tsai[1], Y. L. Tsai[1], P. C. Tesng[1], P. Yu[1], H. C. Kuo[1], C. H. Shen[2], J. M. Shieh[1,2], S. H. Lin[1] and C. C. Lin[1], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*	**16:40 M-2-4** **Epitaxy of Spinel Zn_2TiO_4 (111) on GaN (001) for MOS Application** *S. W. Fu, J .C. Wu, C. Y. Hsiao, K. T. Hung, S. H. Wu, H. J. Chen, H. T. Wu and C. F. Shih, National Cheng Kung Univ. (Taiwan)*	
17:05 GH-2-5 **A novel CMOS image sensor with on-chip micro LED array for spaciotemporally controlled light stimulation and on-chip imaging of a neuronal tissue** *A. Nakajima[1], T. Kobayashi[1,2], T. Noda[1,2], K. Sasagawa[1,2], T. Tokuda[1,2], Y. Ishikawa[1,2], S. Shiosaka[1,2] and J. Ohta[1,2], [1]NAIST and [2]CREST-JST (Japan)*		**16:55 I-2-5** **Optical Characteristics Improvement of High Q Microcavity Light Emitting Diodes with Buried AlN Current Blocking Apertures** *Y. L. Wu, B. S. Cheng, T. C. Lu, C. H. Chiu, C. H. Chen, P. M. Tu, H. C. Kuo and S. C. Wang, National Chiao Tung Univ. (Taiwan)*		**16:40 K-2-5** **Spin-Related Novel Optical Phenomena in Single-Walled Carbon Nanotubes** *S. Konabe[1,2] and S. Okada[1,2], [1]Univ. of Tsukuba and [2]CREST-JST (Japan)*	**16:55 L-2-5** **Photovoltaic Property of Wide-Gap Nanocrystalline Silicon Layers** *R. Mentek, B. Gelloz and N. Koshida, Tokyo Univ. of Agri. and Tech. (Japan)*	**16:55 M-2-5** **Functional Oxides Integrated Epitaxially onto Semiconductors** *R. Droopad, G. Radhakrishnan, R. Contreras-Guererro, W. Priyantha and N. Theodoropoulou, Texas State Univ. (USA)*	
				16:55 K-2-6 **Carbon Nanotube Photonics: Light emission in silicon and optical gain** *N. Izard[1], E. Gaufres[1,2], A. Beck[1], A. Noury[1], X. L. Roux[1] and L. Vivien[1], [1]Univ. Paris-Sud and [2]Univ. Montréal (France)*	**17:10 L-2-2** **Medium Range Order (MRO) in Hydrogenated Amorphous Si Detected by a Non-Vanishing Ligand Field Splitting, Δ LF, in Si $L_{2,3}$ Core Level X-ray Spectra** *G. Lucovsky[1], G.N. Parsons[1], D. Zeller[1], R. Lujan[2] and R.A. Stree[2], [1]North Carolina State Univ. and [2]Palo Alto Research Center (USA)*		

Banquet/Young Researcher Award (16F, Tower Ball Room, Marriott Associa Hotel)

Thursday, September 29

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
		B-3: Novel structure and fabrication process for OTFT (Area 10) (9:00-10:15) Chairs: H. Maeda (Dai Nippon Printing Co. Ltd.) H. Usui (Tokyo Univ. of Agri. & Tech.)	**C-3: Memory Application (Area 2)** (9:00-10:00) Chairs: A. Ikeda (Panasonic Corp.) M. Ueki (Renesas Electronics Corp.)		**E-3: Process Technology and Analysis (Area 1)** (9:00-10:20) Chairs: H. Nohira (Tokyo City Univ.) S. Tsujikawa (Sony Corp.)	**F-3: NAND (Area 4)** (9:00-10:00) Chairs: E. Yang (eMemory Technology Inc.) M. Moniwa (Renesas Electronics Corp.)
		9:00 B-3-1 **Room temperature fabrication of HfON gate insulator for low-voltage operating pentacene-based organic field-effect transistors** *M. Liao[1], H. Ishiwara[1, 2] and S. Ohmi[1], [1]Tokyo Tech and [2]Konkuk Univ. (Japan)*	**9:00 C-3-1** **Improvement of thermal stability in High Density Ta_2O_5 3D capacitor by additional thin SiO_2 layer** *M. Detalle, H. Dekkers, G. Potoms, A. Phommahaxay, D. S. Tezcan, P. Soussan and G. Beyer, IMEC (Belgium)*		**9:00 E-3-1** **Soft X-ray Photoelectron Spectroscopy on Chemical Bonding States of Boron Doped in Si Fin Structures** *Y. Miyata[1], J. Kanehara[1], H. Nohira[2], Y. Izumi[3], T. Muro[3], T. Kinoshita[3], P. Ahmet[1], K. Kakushima[1], K. Tsutsui[1], T. Hattori[1] and H. Iwai[1], [1]Tokyo Tech, [2]Tokyo City Univ. and [3]JASRI/SPring-8 (Japan)*	**9:00 F-3-1** **First 64kb Ferroelectric-NAND Flash Memory Array with 7.5 V Program, 10^8 Endurance and Long Data Retention** *X. Zhang[1], M. Takahashi[1], K. Takeuchi[2] and S. Sakai[1], [1]AIST and [2]Univ. of Tokyo (Japan)*
			9:20 C-3-2 **Pico-Ampere Switching ReRAM with Vertically Contacted 5 nm-diameter Carbon Nanotube Electrodes for BEOL-Based Memory** *H. Nakano, M. Takahashi, T. Murakami, A. Kawabata, M. Sato, M. Nihei and N. Yokoyama, AIST (Japan)*		**9:20 E-3-2** **Concentration Depth Profiling of Heavily Doped Boron at and near SiO_2/Si Interface by Angle-resolved Soft X-ray Photoelectron Spectroscopy** *K. Kakushima[1], J. Kanehara[1], Y. Izumi[2], T. Muro[2], T. Kinoshita[2], P. Ahmet[1], K. Tsutsui[1], T. Hattori[1] and H. Iwai[1], [1]Tokyo Tech and [2]JASRI/SPring-8 (Japan)*	**9:20 F-3-2** **Assessment of Erase-Verify Function in NAND Arrays with Charge-Based Capacitance Measurement** *L. H. Chong, Y. W. Chang, K. F. Chen, Y. J. Chen, S. H. Ku, N. K. Zous, I. J. Huang, T. T. Han, M. S. Chen, W. P. Lu, K. C. Chen and C. Y. Lu, Macronix Int. Co., Ltd. (Taiwan)*
		9:30 B-3-3 **UV-Ozone Effect of the Organic Thin Film Transistor with PVP Gate Dielectric in Low Temperature** *H. J. Yun[1], K. H. Baek[2], L. M. Do[2], S. Y. Lee[1], K. S. Jeong[1], Y. M. Kim[1], S. D. Yang[1], H. D. Lee[1] and G. W. Lee[1], [1]Chungnam National Univ. and [2]ETRI (Korea)*	**9:40 C-3-3** **Performance Evaluation of a Logic-IP Compatible (LIC) Embedded DRAM with Cylinder Capacitors in Low-k/Cu BEOL Layers** *I. kume, N. inoue, K. Hijioka, J. Kawahra, K. Takeda, N. Furutake, H. Shirai, K. Kazama, S. Kuwabara, M. Watarai, T. Sakoh, T. Takahashi, T. Ogura, T. Taiji, K. Kasama, M. Sakamoto, M. Hane and Y. Hayashi, Renesas Electronics Corp. (Japan)*		**9:40 E-3-3** **On the Si Surface Flattening Effect and Gate Insulator Breakdown Characteristic of Radical Reaction Based Insulator Formation Technology** *R. Kuroda, A. Teramoto, X. Li, T. Suwa, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)*	**9:40 F-3-3** **Disturb-free 3D vertical FG NAND with Separated-Sidewall Control Gate** *M. S. Seo[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)*
		9:45 B-3-4 **Spatial Control of the Threshold Voltage of Low-Voltage Organic Transistors by Microcontact Printing of Alkyl- and Fluoroalkyl-phosphonic Acids** *I. Hirata[1], U. Zschieschang[2], F. Ante[2], T. Yokota[1], K. Kuribara[1], T. Yamamoto[3], K. Takimiya[3], M. Ikeda[4], H. Kuwabara[4], H. Klauk[2], T. Sekitani[1] and T. Someya[1], [1]Univ. of Tokyo, [2]Max Planck Inst. for Solid State Res., [3]Hiroshima Univ. and [4]Nippon Kayaku Corp., Ltd. (Japan)*			**10:00 E-3-4** **High Quality and Low Thermal Budget Silicon Nitride Deposition Using PECVD for Gate Spacer, Silicide Block and Contact Etch Stopper** *Y. Nakao, R. Kuroda, H. Tanaka, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)*	
		10:00 B-3-5 **Air-Stable Polymer and Blade Coating Technique for High-Performance Vertical Polymer Transistors** *H. W. Zan, Y. C. Chao, C. H. Chung, , Y. H. Hsu and H. F. Meng, National Chiao Tung Univ. (Taiwan)*				

Coffee Break

Short Presentation (10:45-12:00)

Short Presentation P-6 (10:45-12:00) Chairs: T. Suzuki (JAIST) S. Sasa (Osaka Inst. of Tech.)		Short Presentation P-10 (10:45-12:00) Chairs: T. Shimada (Hokkaido Univ.) S. Naka (Univ. of Toyama)	Short Presentation P-2 (10:45-12:00) Chairs: M. Ueki (Renesas Electronics Corp.) A. Ikeda (Panasonic Corp.)	Short Presentation P-3 (10:45-12:00) Chairs: H. Fujimoto (Panasonic Corp.) O.Weber (CEA-LETI/MINATEC)	Short Presentation P-1 (10:45-12:00) Chairs: K. Kita (Univ. of Tokyo) E. Nishimura (Tokyo Electron Ltd.)	Short Presentation P-4 (10:45-12:00) Chairs: T. Eshita (Fujitsu Semiconductor Ltd.) T. Endoh (Tohoku Univ.)

12:00-13:30 Lunch

Thursday, September 29

11F 1104

G-3: Variation and Reliability (Area 5)
(9:00-10:15)
Chairs: H. Takao (Kagawa Univ.)
S. Sugawa (Tohoku Univ.)

9:00 G-3-1
Multi-core LSI Lifetime Extension by NBTI-Recovery-based Self-healing
T. Matsumoto[1], H. Makino[1], K. Kobayashi[2,3] and H. Onodera[1,3], [1]Kyoto Univ., [2]Kyoto Inst. of Tech. and [3]CREST-JST (Japan)

9:20 G-3-2
Experimental Comparison of Process Variation in 65nm and 180nm CMOS Using Ring Oscillators with Adjustable Delay
T. Ansari, W. Imafuku, M. Yasuda, S. Sasaki, H. J. Mattausch and T.Koide, Hiroshima Univ. (Japan)

9:40 G-3-3
Effect of Resin-Molded Package Structure on Silicon Chip Surface Stress Distribution
N. Ueda, E. Nishiyama and H. Watanabe, RICOH Co., Ltd. (Japan)

10:00 G-3-4 (Late News)
Investigation of Subthreshold Drain Current Mismatch Characteristics for Nanoscale MOSFETs
J. J. Y. Kuo and P. Su, National Chiao Tung Univ. (Taiwan)

11F 1107

H-3: Electric, Magnetic and Optical Biosensing (Area 11)
(9:00-10:15)
Chairs: Y. S. Yang (National Chiao Tung Univ.)
H. Suzuki (Hiroshima Univ.)

9:00 H-3-1 (Invited)
Bio-particles Detection based on Dielectrophoretic Microfluidic Chip Combined with Optical Method
H. C. Chang, C. C. Chung and I. F. Cheng, National Cheng Kung Univ. (Taiwan)

9:30 H-3-2
Study on Micro Optical Diffusion Sensor using Laser-induced Dielectrophoresis
Y. Ishii, Y. Taguchi and Y. Nagasaka, Keio Univ. (Japan)

9:45 H-3-3
Development and Evaluation of Local Illumination Device beyond Diffraction Limit using Polymeric Nanohole Array
T. Ono[1,2], R. Iizuka[1,2], T. Akagi[1,2], T. Funatsu[1,2] and T. Ichiki[1,2], [1]Univ. of Tokyo and [2]CREST-JST (Japan)

10:00 H-3-4
Point of care biosensing protocol based on magnetically induced self-assembly of functionalized particles dispersed in colloids
Y. Yang[1,2], T. Takamura[1] and A. Sandhu[1,3], [1]Tokyo Tech, [2]Tsinghua Univ. and [3]Toyohashi Univ. of Tech. (Japan)

12F 1201

I-3: Plasmonics and Nonlinear Devices (Area 7)
(9:00-10:15)
Chairs: H. Isshiki (The Univ. of Electro-Communications)
J. Fujikata (NEC Corp.)

9:00 I-3-1 (Invited)
Plasmonic Nanophotonic Structures for Future Communications and Energy Applications
H. A. Atwater, California Inst. of Tech. (USA)

9:30 I-3-2
Femtosecond Two-photon Fluorescence Microscopy of Surface Plasmon Polariton
T. Hattori[1], A. Kubo[1], K. Oguri[2], H. Nakano[2] and H. T. Miyazaki[3], [1]Univ. of Tsukuba, [2]NTT Basic Res. Labs. and [3]NIMS (Japan)

9:45 I-3-3
Modal phase matcing in ZnO channel waveguide for highly efficient second harmonic generation
Y. Taira, T. Kita, Y. Morales and H. Yamada, Tohoku Univ. (Japan)

10:00 I-3-4
$MgO:LiNbO_3$ Waveguide Second-Harmonic Generation Devices with Domain-Inverted Gratings Formed by 2-Step Voltage Application under UV Light
M. Fujimura, E. Kitado, T. Inoue and T. Suhara, Osaka Univ. (Japan)

12F 1202

J-3: Graphene Quantum Transport (Area 9)
(9:00-10:15)
Chairs: T. Machida (Univ. of Tokyo)
A. Kanda (Univ. of Tsukuba)

9:00 J-3-1 (Invited)
Electronic transport in graphene nanostructures
T. Ihn, S. Dröscher, J. Güttinger, A. Jacobsen, H. Knowles, F. Molitor, S. Schnez, P. Simonet, C. Stampfer and K. Ensslin, Solid State Physics Lab. (Switzerland)

9:30 J-3-2
Introducing Nonuniform Strain to Graphene: Toward Strain Engineering
H. Tomori[1,2], H. Goto[1,2], Y. Nukui[1,2], Y. Toyota[1,2], Y. Ootuka[1], K. Tsukagoshi[2,3], S. Moriyama[3], E. Watanabe[3], D. Tsuya[3] and A. Kanda[1,2], [1]Univ. of Tsukuba, [2]CREST-JST and [3]NIMS (Japan)

9:45 J-3-3
Device Performance of Graphene Nanoribbon MOSFET and Tunneling FET with Phonon Scattering: A Computation Study
K. T. Lam[1], S. K. Chin[2] and G. Liang[1,2], [1]National Univ. of Singapore and [2]Inst. of High Performance Computing (Singapore)

10:00 J-3-4
Mobility Difference in Top and Bottom Surfaces of Multilayer Graphene Placed on Silicon Dioxide
Y. Nukui[1,2], H. Tomori[1,2], H. Goto[1,2], Y. Toyota[1,2], Y. Ootuka[1], K. Tsukagoshi[2,3] and A. Kanda[1,2], [1]Univ. of Tsukuba, [2]CREST-JST and [3]NIMS (Japan)

12F 1203

K-3: Nanowire/Nanotube FET (Area 13)
(9:00-10:00)
Chairs: J. Motohisa (Hokkaido Univ.)
C. Liu (Chinese Academy of Sciences)

9:00 K-3-1
Electron mobility calculations of free-standing Si-nanowires with atomistic electron-phonon interactions
Y. Yamada, H. Tsuchiya and M. Ogawa, Kobe Univ. (Japan)

9:15 K-3-2
Charge transfer by multiple donors in a Si nanowire
G. P. Lansbergen, Y. Ono and A. Fujiwara, NTT Basic Res. Labs. (Japan)

9:30 K-3-3
High-performance Carbon Nanotube Thin-film Transistors with $>600\ cm^2V^{-1}s^{-1}$ Mobility and $>10^7$ On/off Ratio
D. M. Sun[1], M. Y. Timmermans[2], Y. Tian[2], A. G. Nasibulin[2], S. Kishimoto[1], T. Mizutani[1] and E. I. Kauppinen[2], Y. Ohno[1], [1]Nagoya Univ. and [2]Aalto Univ. (Japan)

9:45 K-3-4
Ambipolar Conversion of Polymer-Coated All Single-Walled Carbon Nanotube Field-Effect Transistors
S. Aikawa[1,2], E. Einarsson[1], S. Chiashi[1], E. Nishikawa[2] and S. Maruyama[1], [1]Univ. of Tokyo and [2]Tokyo Univ. of Sci. (Japan)

12F 1204

L-3: Compound Thin Film Solar Cells. (Area 14)
(9:00-10:15)
Chairs: N. J. Ekins-Daukes (Imperial College London)
H. Katagiri (NNCT)

9:00 L-3-1 (Invited)
Hetero Junction Engineering for High Efficiency $Cu(In,Ga)Se_2$ Solar Cells
T. Minemoto, Ritsumeikan Univ. (Japan)

9:30 L-3-2
$Cu(In,Al)S_2$ thin film solar cells prepared from sulfurization of Cu-In-Al precursors
Y. Oda, R. Hamazaki, S. Fukamizu, A. Yamamoto, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan)

9:45 L-3-3
Effect of Solid-Phase-Epitaxy Si Layers on Suppression of Sb Diffusion from Sb-Doped n^+-$BaSi_2$/p^+-Si Tunnel Junction to Undoped $BaSi_2$ Overlayers
W. J. Du[1], T. Saito[1], M. A. Khan[1], K. Nakamura[1], M. Baba[1], K. Toh[1], K. Toko[1], N. Usami[2,3] and T. Suemasu[1,3], [1]Univ. of Tsukuba, [2]Tohoku Univ. and [3]CREST-JST (Japan)

10:00 L-3-4
Annealing of the $BaSi_2$ Epitaxial Films Implanted with BF_2 Ions
K.O. Hara[1,4], N. Usami[1,4], Y. Hoshi[2], Y. Shiraki[2], M. Suzuno[3], K. Toko[3,4] and T. Suemasu[3,4], [1]Tohoku Univ., [2]Tokyo City Univ., [3]Univ. of Tsukuba and [4]CREST-JST (Japan)

12F 1207

M-3: III-V Compounds (Area 8)
(9:00-10:15)
Chairs: M. Kondow (Osaka Univ.)
T. Suemasu (Univ. of Tsukuba)

9:00 M-3-1 (Invited)
Morphological and compositional interface stability of metastable ternary and quaternary (Ga,In)(As,Sb) quantum wells
A. Trampert, Paul-Drude-Institute (Germany)

9:30 M-3-2
High-speed three-dimentional reciprocal-space mapping during MBE growth of InGaAs
W. Hu[1], H. Suzuki[2], T. Sasaki[3], M. Kozu[4] and M. Takahasi[1,4], [1]JAEA, [2]Univ. of Miyazaki, [3]Toyota Technological Inst. and [4]Univ. of Hyogo (Japan)

9:45 M-3-3
Effect of Initial In Coverage for Preparation of InSb Bilayer on Electrical Properties of InSb Films Grown By Surface Reconstruction Controlled Epitaxy
M. Mori[1], Y. Yasui[1], K. Nakayama[1], K. Nakatani[1] and K. Maezawa[1], Univ. of Toyama (Japan)

10:00 M-3-4
Characteristics of Nitrogen δ-doped AlGaAs/GaAs Quantum Wells grown by Molecular Beam Epitaxy
S. Furuse, K. Sumiya, M. Morifuji and F. Ishikawa, Osaka Univ. (Japan)

12F 1208

Coffee Break

Short Presentation (10:45-12:00)

Short Presentation
P-5 (10:45-12:00)
Chairs: K. Kagawa (Shizuoka Univ.)
T. Koide (Hiroshima Univ.)

Short Presentation
P-11 (10:45-12:00)
Chairs: K.Sawada (Toyohashi University of Tech.)
T.Tanaka (Tohoku Univ.)

Short Presentation
P-7 (10:45-12:00)
Chairs: H. Isshiki (The Univ. of Electro-Communications)
N. Iizuka (Toshiba Corp.)

Short Presentation
P-9 (10:45-12:00)
Chairs: K. Ono (RIKEN)
H. Gotoh (NTT Basic Res. Labs.)

Short Presentation
P-13 (10:45-12:00)
Chairs: Y. Ohno (Nagoya Univ.)
J. Motohisa (Hokkaido Univ.)

Short Presentation
P-14 (10:45-12:00)
Chairs: M. Ishiko (Toyota Central R&D Labs., Inc)
Y. Kurokawa (Tokyo Tech)

Short Presentation
P-8 (10:45-12:00)
Chairs: H. Hibino (NTT Basic Res. Labs.)
T. Iwai (Fujitsu Labs. Ltd.)

Short Presentation
P-12 (10:45-12:00)
Chairs: M. Yamamoto (Hokkaido Univ.)
H. Munekata (Tokyo Tech.)

12:00-13:30 Lunch

POSTER SESSION (13:30-15:00, 6F Exhibition Hall)

Area 1: Advanced LSI Processing & Materials Science (20 Papers)

P-1-1
High Quality Germanium Dioxide Formation using Damage-Free and Low-Temperature Neutral Beam Oxidation Process
A. Wada[1], K. Endo[2], M. Masahara[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)

P-1-2
Passivation of Ge(100) and (111) Surfaces by Termination of Nonmetal Elements
D. H. Lee, K. Kubo, T. Kanashima and M. Okuyama, Osaka Univ. (Japan)

P-1-3
First-Principles Study on Interface Properties of GeO_2/Ge System
S. Saito and T. Ono, Osaka Univ. (Japan)

P-1-4
Evaluation of Thermally-Grown Ge Oxide on Ge(100) and Ge(111) Surfaces
S. K. Sahari[1], A. Ohta[1], M. Matsui[1], H. Murakami[1], S. Higashi[1] and S. Miyazaki[2], [1]Hiroshima Univ. and [2]Nagoya Univ. (Japan)

P-1-5
Control of Defect Properties in Ge Heteroepitaxial Layers by Sn Incorporation and H_2-Annealing
M. Adachi, Y. Shimura, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)

P-1-6
Formation of Ohmic Contacts with Shallow NiGe/n^+ Ge Junction
M. Miura[1,2], M. Noguchi[1,2], J. Fujikata[1,2], T. Horikawa[1,3], M. Takahashi[1,3], Y. Noguchi[1,3] and Y. Arakawa[1,4], [1]PECST, [2]PETRA, [3]AIST and [4]Univ. of Tokyo (Japan)

P-1-7
Estimation of breakdown electric-field strength reflecting local structures of SiO_2 by using first-principles molecular orbital calculation technique
H. Seki[1], Y. Shibuya[2], D. Kobayashi[3], H. Nohira[2], K. Yasuoka[1] and K. Hirose[3], [1]Keio Univ., [2]Tokyo City Univ. and [3]ISAS/JAXA (Japan)

P-1-8
Clear Difference between Chemical Structure of SiO_2/Si Interface Formed Using Oxygen Radicals and That Formed Using Oxygen Molecules
T. Suwa[1], Y. Kumagai[1], A. Teramoto[1], T. Muro[2], T. Kinoshita[2], S. Sugawa[1], T. Hattori[1] and T. Ohmi[1], [1]Tohoku Univ. and [2]Japan Synchrotron Radiation Res. Inst. (Japan)

P-1-9
Thermal Stability of Single and Alloy Noble Metals as for PMOS Gate Electrode
C. Choi[1], J. Ahn[1] and R. Choi[2], [1]Hanyang Univ. and [2]Inha Univ. (Korea)

P-1-10
Analysis of Raman Spectra from Offset Spacer Region of Si-MOSFET Structure using Simulated Stress Tensor and Absorbed Light Intensity by FDTD Simulation
A. Satoh[1], T. Tada[1], V. Poborchii[1], T. Kanayama[1], S. Satoh[2] and H. Arimoto[1], [1]AIST and [2]Fujitsu Semiconductor Ltd. (Japan)

P-1-11
Chemical Bonding States of As in Si Shallow Junctions Detected by Soft X-ray Photoelectron Spectroscopy and their Profiles
J. Kanehara[1], Y. Miyata[1], H. Nohira[2], Y. Izumi[3], T. Muro[3], T. Kinoshita[3], P. Ahmet[1], K. Kakushima[1], K. Tsutsui[1], T. Hattori[1] and H. Iwai[1], [1]Tokyo Tech, [2]Tokyo City Univ. and [3]JASRI/SPring-8 (Japan)

P-1-12
Comprehensive Understanding of Flatband Voltage Shift Based on Energy Band Alignment of the Whole Metal/high-k/SiO_2/Si Stack
X. Wang[1], W. Wang[1], K. Han[1], J. Zhang[2], X. Ma[1], J. Xiang[1], D. Chen[1] and T. Ye[1], [1]Chinese Academy of Sci. and [2]North China Univ.of Tech. (China)

P-1-13
Lateral Large-Grained Low-Temperature Polycrystalline Silicon-Germanium Thin-Film Transistors on Glass Substrate
Y. Okabe[1], K. Kondo[1], J. Suzuki[2], K. Kitahara[2] and A. Hara[1], [1]Tohoku Gakuin Univ. and [2]Shimane Univ. (Japan)

P-1-14
Enhanced Sidewall Growth (ESG) process: towards PEALD with conformality above 100%
S. Ueda, A. Fukazawa, H. Fukuda and N. Kobayashi, ASM Japan K.K. (Japan)

P-1-15
Mean time to failure distribution in thin oxide film: Observation at nano and devices scale and modelling using a filamentary growth model
P. Delcroix[1,2], S. Blonkowski[1], M. Kogelschatz[2] and M. Rafik[1], [1]STMicroelectronics and [2]CNRS (France)

P-1-16
Electrical Characteristics of Back Gated FET on a Wrinkle Free Graphene Channel
C. H. Cho, S. K. Lim, C. G. Kang, Y. G. Lee, H. J. Hwang, E. Park and B. H. Lee, Gwangju Inst. of Sci. and Tech. (Korea)

P-1-17
Novel activation method of B by soft X-ray undulator
T. Fukuoka[1], A. Heya[1], N. Matsuo[1], K. Kanda[1] and T. Noguchi[2], [1]Univ. of Hyogo and [2]Univ. of the Ryukyus (Japan)

P-1-18
Impact of Zirconia addition for ALD Hafina in HKMG Device Fabricated GF vs. GL
C. K. Chiang[1,3], C. H. Wu[2], H. Y. Huang[1], J. F. Lin[3], C. L. Yang[3], J. Y. Wu[3] and S. J. Wang[1], [1]National Cheng Kung Univ., [2]Chung Hua Univ. and [3]United Microelectronics Corp. (Taiwan)

P-1-19 (Late News)
Fermi Level Depinning for Metal/Germanium Schottky Junction by CF_4 Plasma Treatment
J. R. Wu, C. Y. Hou, M. L. Wu, C. C. Lin and Y. H. Wu, National Tsing-Hua Univ. (Taiwan)

Area 2: Advanced Interconnect / Materials Technology and Characterization (18 Papers)

P-2-1
Direct wafer bonding technology of 300mm wafer
S. Hongo, K. Tanida, N. Yamaguchi and K. Takahashi, Toshiba Corp. (Japan)

P-2-2
Thinning Process Induced Surface Defects in Ultra-Thin Si Wafer
M. Murugesan[1], H. Nohira[2], C. Miyazaki[3], H. Shimamoto[3], H. Kobayashi[3], T. Fukushima[1], T. Tanaka[1] and M. Koyanagi[1], [1]Tohoku Univ., [2]Tokyo City Univ. and [3]ASET (Japan)

P-2-3
Mn_2O_3 Slurry Reuse for SiO_2 Film CMP
S. Kishii[1, 3], K. Nakamura[1], K. Hanawa[2], S. Watanabe[1], Y. Arimoto[1], S. Kurokawa[3] and T. K. Doi[3], [1]Fujitsu Labs. Ltd., [2]Showa Denko K. K. and [3]Kyushu Univ. (Japan)

P-2-4
Optimum Design of MEMS Resonator Array to Measure the Young's Modulus of Nano-Scale Thin Films for the Reliability of Semiconductor Devices
H. Yamagiwa[1], S. Ito[1], T. Namazu[1,2], T. Takeuchi[3], K. Murakami[3], Y. Kawashimo[3] and T. Takano[4], [1]Univ. of Hyogo, [2]PRESTO-JST, [3]Shinko Seiki Co. Ltd. and [4]The New Industry Research Organization (Japan)

P-2-5
A New Technique for in-Plane Poisson's Ratio Measurement of Thin Films - Cases of Single-Crystal Silicon and Aluminum Thin Films -
T. Fujii[1], T. Namazu[1,2], M. Takahashi[1], M. Tanaka[1], K. Yoshiki[1] and S. Inoue[1], [1]Univ. of Hyogo and [2]PRESTO-JST (Japan)

P-2-6
Evolution of Wafer Shape and Localized Stress of Silicon Surrounded by Through Silicon Via Patterns along Various Process Integration Steps
C. H. Lee[1], S. H. Jie[1], S. H. Son[1], J. T. Kim[1], H. W. Yoo[1], I. K. Han[1] and W. S. Yoo[2], [1]Hynix Semiconductor Inc. and [2]WaferMasters, Inc. (Korea)

P-2-7
Improvement of the BCB Adhesion on Cr/Au Metal Layer for RF Packaging Module
N. Jeon, Y. H. Oh, Y. Ryoo and K. S. Seo, Seoul National Univ. (Korea)

P-2-8
Testkey Design of Through Silicon Vias (TSVs) for Accurate De-embedding and RF Model Parameters Extraction
J. Y. Wang[1], T. K. Huang[1], Y. C. Wu[1], S. S. H. Hsu[1], Z. H. Lin[2], C. S. Lin[2], S. S. Sheu[2], T. K. Ku[2] and C. H. Lin[2], [1]National Tsing Hua Univ. and [2]ITRI (Taiwan)

P-2-9
Study of Local Charging Phenomena during SiO_2 Contact Hole Etching
T. Yagisawa[1], T. Tatsumi[2] and T. Makabe[1], [1]Keio Univ. and [2]Sony Corp. (Japan)

P-2-10
Thermal Cycling Reliability of ChipArray® Thin Core Ball Grid Array assemblies with Fast Cure and Reworkable Capillary Flow Underfill
H. Shi and T. Ueda, Waseda Univ. (Japan)

P-2-11
Selective Heating of Microbumps Using Microwave for Low Strain Heterogeneous Chip Stack Integration
L. Qiu and T. Asano, Kyushu Univ. (Japan)

P-2-12
Room temperature fabrication of silver nanowire transparent electrodes
T. Tokuno, M. Nogi, M. Karakawa, J. T. Jiu and K. Suganuma, Osaka Univ. (Japan)

P-2-13
Low-Energy Ion-Beam-Assisted Sputtering for Si Nanocrystals
C. Y. Hsiao, K. W. Su, K. T. Hung, H. T. Wu, H. J. Chen, S. W. Fu, S. H. Wu and C. F. Shih, National Cheng Kung Univ. (Taiwan)

P-2-14
Highly Accurate Lattice-Strain mapping near Interfaces of Hetero-Structures by Convergent-Beam and Nano-Beam Electron Diffraction
K. Saitoh, H. Nakahara, Y. Daikyo and N. Tanaka, Nagoya Univ. (Japan)

P-2-15
Multi-layer Graphene for High-Frequency Interconnect
H. J. Lee, E. Kim and J. W. Jung, Sejong Univ. (Korea)

P-2-16
Investigation of Electrical Properties of HfN/HfSiON Gate Stacks In-situ Formed on Si(100) and Si(110)
T. Sano and S. Ohmi, Tokyo Tech (Japan)

P-2-18 (Late News)
MIM Capacitors with High Capacitance Density and Low Quadratic Voltage Coefficient by Employing Crystalline-TiO_2/SiO_2 Stacked Dielectric
C. C. Lin, W. Y. Ou, J. R.Wu, M. L.Wu, L. L.Chen and Y. H. Wu, National Tsing Hua Univ. (Taiwan)

Area 3: CMOS Devices / Device Physics (22 Papers)

P-3-1
Impact of Aspect Ratio on the Subthreshold RTN Amplitude of Multi-Gate MOSFETs
B. K. Lu, M. L. Fan and P. Su, National Chiao Tung Univ. (Taiwan)

P-3-2
Saturation Behavior in the Generation of Interface Traps by Hot-Carrier Stress in Nanoscale MOSFETs
M. Hu, T. Yamane and T. Tsuchiya, Shimane Univ. (Japan)

P-3-3
Investigation of Temperature Dependence on DC and Low-Frequency Noise Characteristics in Uniaxial Tensile Strained nMOSFETs
S. C. Tsai[1], S. L. Wu[2], J. F. Chen[1], S. J. Chang[1], C. Y. Chang[1], P. C. Huang[1], C. Y. Wu[2], M. S. Chen[3], Y. C. Cheng[3] and O. Cheng[3], [1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]United Microelectronics Corp. (Taiwan)

P-3-5
The Effect of La_2O_3 Capping Layer Thickness on Hot Carrier Degradation of *n*-MOSFETs with High-*k*/Metal Gate Stack
D. W. Kim[1], S. H. Lee[1], C. G. Kim[1], T. K. Oh[2] and B. K. Kang[1], [1]Pohang Univ. Sci. Tech. and [2]Hynix Semiconductor Inc. (Korea)

P-3-6
Characterization of Oxide Traps in 28 nm pMOSFETs with Σ-Shaped SiGe-S/D by Utilizing Random Telegraph Noise (RTN)
B. C. Wang[1], S. L. Wu[2], S. J. Chang[1], C. T. Huang and O. Cheng, [1]National Cheng Kung Univ. and [2]Univ. of Cheng Shiu (Taiwan)

P-3-7
Hot-Carrier Effects on High-frequency Characteristics of RF LDMOS Transistors
K. M. Chen[1], Z. W. Mou[2], H. C. Kuo[2], C. S. Chiu[1], B. Y. Chen[1], W. D. Liu[1], M. Y. Chen[3], Y. C. Yang[3], K. L. Wang[3] and G. W. Huang[1, 2], [1]National Nano Device Labs., [2]National Chiao Tung Univ. and [3]United Microelectronics Corp. (Taiwan)

P-3-8
Impact of OFF-state Degradation under Dynamic Stress on Reliability of Nanoscale n-Channel Metal-Oxide-Semiconductor Field-Effect Transistors at Elevated Temperature
N. H. Lee[1], K. J. Kim[1], H. W. Kim[2] and B. K. Kang[1], [1]POSTECH and [2]Samsung Electronics Corp. Ltd. (Korea)

P-3-9
Modeling Subthreshold Current and Threshold Voltage of Fully-Depleted Double-gate Junctionless(J-less) Transistors
Z. M. Lin[1], H. C. Lin[1,2], K. M. Liu[3] and T. Y. Huang[1], [1]National Chiao Tung Univ., [2]Labs of National Nano Device and [3]National Dong Hwa Univ. (Taiwan)

P-3-10
Integration of InGaAs Nanowire Vertical Surrounding-Gate Transistors on Si
K. Tomioka[1,2], M. Yoshimura[1] and T. Fukui[1], [1]Hokkaido Univ. and [2]PREST-JST (Japan)

P-3-11
Body Channel Type Vertical MOSFET to Suppress Gate Leakage Current
T. Sasaki[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)

P-3-12
Investigation of Short-Channel Effects in Junctionless Nanowire Transistors
P. Razavi, N. Dehdashti-Akhavan, R. Yu, G. Fagas, I. Ferain and J.P. Colinge, Univ. College Cork (Ireland)

P-3-13
Stack Gate Technique for Feasible Bulk FinFETs
Y. B. Liao[1], M. H. Chiang[2], W. C. Hsu[1], Y. S. Lai[3] and H. Li[2], [1]National Cheng Kung Univ., [2]National Ilan Univ. and [3]National Nano Device Lab. (Taiwan)

P-3-14
Strain Effects on Ballistic Currents of Silicon Nanowire pFETs with Different Orientations
J. Qin, X. Liu, H. Xu, J. Zhang and G. Du, Peking Univ. (China)

P-3-16
Evidence of the universality of the hole mobility in accumulation MOS transistors
P. Gaubert, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)

P-3-17
Simulation of Electron Transport in Source and Drain Electrodes of Ultrathin Body III-V Channel MOSFETs
Y. Maegawa[1], S. Koba[1], H. Tsuchiya[1,2] and M. Ogawa[1], [1]Kobe Univ. and [2]CREST-JST (Japan)

P-3-18
Evaluation of Drain Current Fluctuations of Si MOSFETs using BSIM3-like Current Model and TCAD
A. Satoh[1], T. Tada[1], T. Kanayama[1], S. Satoh[2] and H. Arimoto[1], [1]AIST and [2]Fujitsu Semiconductor Ltd. (Japan)

P-3-20 (Late News)
Critical Parameters for Accurate Calculation of Si Nanowire MOSFET Current
K. Natori, Tokyo Tech (Japan)

P-3-21 (Late News)
Impact of Poly Depletion on Accurate Evaluation of Self-Heating Effects in SOI MOSFETs with Four-point Gate Resistance Measurement Method
N. Beppu, T. Takahashi, T. Ohashi and K. Uchida, Tokyo Tech (Japan)

P-3-22 (Late News)
Random Interface-Traps-Induced Characteristic Fluctuation in 16-nm High-k/Metal Gate CMOS Device and Digital Circuit
Y. Y. Chiu, Y. Li and H. W. Cheng, National Chiao Tung Univ. (Taiwan)

Area 4: Advanced Memory Technology

(16 Papers)

P-4-1
Pushing Scaling Limit Due to Short Channel Effects and Channel Boosting Leakage from 13nm to 8nm with SOI NAND Flash Memory Cells
K. Miyaji, C. Hung and K. Takeuchi, Univ. of Tokyo (Japan)

P-4-4
Electrical Property of DNA FET —Charge Retention Property—
S. Takagi[1], N. Matsuo[1], K. Yamana[1], A. Heya[1], T. Takada[1] and S. Yokoyama[2], [1]Univ. of Hyogo and [2]Hiroshima Univ. (Japan)

P-4-5
Areal and Structural Effect on Oxide based RRAM cell for Improving Resistive Switching Characteristics
K. C. Ryoo[1,2], J. H. Oh[1,2], S.H. Jung[1], G. T. Jeong[2], H. S. Jeong[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics. Co., Ltd. (Korea)

P-4-6
Investigation of Switching Behavior of 2-terminal Devices on VO_2
I. P. Radu[1,2], K. Martens[1], B. Govoreanu[1], S. Mertens[1], X. Shi[1], M. Cantoro[1], M. Schaekers[1], M. Jurczak[1], S. De Gendt[1,2], A. Stesmans[1,2], M. Heyns[1,2] and J. A. Kittl[1], [1]IMEC and [2]Univ. of Leuven (Belgium)

P-4-7
Evaluation of the WO_x Film Properties for ReRAM Application
Y. Y. Chen[1,2], W. C. Chien[2], M. H. Lee[2], Y. C. Chen[2], A. T. H. Chuang[2], T. J. Hong[1], S. J. Lin[1], T. B. Wu[1] and C. Y. Lu[2], [1]National Tsing Hua Univ. and [2]Macronix International Corp., Ltd. (Taiwan)

P-4-8
Characterization and improved endurance for HfO_2 resistive memory with CMP treated TiN bottom electrode
P. S. Chen[1], Y. S. Chen[2,3], H. Y. Lee[2], T. Y. Wu[2], W. H. Liu[2], P. Y. Gu[2], F. Chen[2] and M. J. Tsai[2], [1]MingShin Univ. Sci. and Eng., [2]Industrial Tech. Res. Inst. and [3]National Tsing Hua Univ. (Taiwan)

P-4-9
Study of Bipolar Multilevel Memristive Mechanism and Characterizations in a Thin FeO_x Transition Layer Device
G. Y. Wu[1], Y. F. Chang[1], L. W. Feng[1], C. Y. Chang[1] and T. C. Chang[2], [1]National Chiao Tung Univ. and [2]National Sun Yat-Sen Univ. (Taiwan)

P-4-10
Multi-Level Phase-Change Memory Cells with SiN or Ta_2O_5 Barrier Layers
A. Gyanathan and Y. C. Yeo, National Univ. of Singapore (Singapore)

P-4-11
Endurance enhancement of elevated-confined phase change random access memory
*H. X. Yang[1,2], L. P. Shi[1], H. K. Lee[1], R. Zhao[1] and T. C. Chong[3], [1]A*STAR, [2]National Univ. of Singapore and [3]Singapore Univ. of Tech. and Design (Singapore)*

P-4-12
Simulation of Retention Behavior for the Phase Change Memory
J. Chen, D. Song, G. Du, G. Lian, J. Kang and X. Liu, Peking Univ. (China)

P-4-13 (Late News)
Filament Formation by Cu and Ag Ions for Memory Applications Utilizaing Oxide Dielectrics With Pre-existing Vacated O-atom Sites
Z. Zhang[1], E. Katz[1], D. Zeller[2], G. Lucovsky[2] and L. F. Brillson[1], [1]Ohio State Univ. and [2]North Carolina State Univ. (USA)

P-4-14 (Late News)
Effect of Oxidation Amount on Gradual Switching Behavior in Reset Transition of Al/TiO_2 based Resistive Switching Memory and its Mechanism for MLC Operation
J. H. Oh[1,2], K. C. Ryoo[1,2], S. Jung[1], Y. Park[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)

P-4-15 (Late News)
Design and Optimization of Program and Restore Operations in CMOS-Compatible Nonvolatile Latch
J. G. Lee and S. Masui, Tohoku Univ. (Japan)

P-4-16 (Late News)
SET polarity dependent resistive switching memory characteristics using IrOx/GdOx/WOx/W structure
D. Jana[1], S. Maikap[1], T. C. Tien[2], H. Y. Lee[2], W. S. Chen[2], F. T. Chen[2], M. J. Kao[2] and M. J. Tsai[2], [1]Chang Gung Univ. and [2]ITRI (Taiwan)

Area 5: Advanced Circuits and Systems

(17 Papers)

P-5-1
Wireless Charge Based Capacitance Measurement Circuits with On-chip Spiral Inductor for RFID Biosensor
B. Kim[1], S. Uno[2] and K. Nakazato[1], [1]Nagoya Univ. and [2]Ritsumeikan Univ. (Japan)

P-5-2
SPICE MOSFET Analog Model Parameter Verification and Re-optimization Based on g_m/I_D Lookup Table Design Methodology
T. Konishi[1], B. Patrick[1], T. Kaho[2] and S. Masui[1], [1]Tohoku Univ. and [2]NTT Network Innovation Labs. (Japan)

P-5-3
Write Speed Evaluation of Reconfigurable Spin Logic Block with SPRAM for 3D-Stacked Reconfigurable Spin Processor
R. Nakazawa[1], H. Kino[1], K. Kiyoyama[1,2], M. Koyanagi[1] and T. Tanaka[1], [1]Tohoku Univ. and [2]Nagasaki Inst. of Applied Science (Japan)

P-5-4
Nonvolatile Low Power 16-bit/32-bit MTJ Based Binary Counter and its Scaling
S. Togashi, T. Ohsawa and T. Endoh, Tohoku Univ. (Japan)

P-5-5
Evaluation of Reconfigurable Processor Test Chip for Dependable 3D Stacked Multicore Processor
H. Hashimoto, T. Fukushima, K. W. Lee, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)

P-5-6
A High-Voltage Tolerant Interface Circuit for Embedded CMOS Non-volatile Memories
C. Y. Huang and H. Lin, National Chung Hsing Univ. (Taiwan)

P-5-7
The Integrated a-Si Gate Driver Circuit using Voltage Controlled Capacitance Modeling for HDTV/XGA
S. K. Han[1], J. Y. Kim[1], H. Choi[1], K. H. M. Choi[1], Y. S. Choi[1], K. M. Park[2] and S. Y. Choi[2], [1]LG Display Co. Ltd. and [2]Kyungpook National Univ. (Korea)

P-5-8
A Fully-Parallel Self-Learning Analog Support Vector Machine Employing Compact Gaussian-Generation Circuits
R. Zhang and T. Shibata, Univ. of Tokyo (Japan)

P-5-9
Current Compensation Circuit for Precise Nano-Ampere Current Reference
K. Isono, T. Hirose, Y. Osaki, N. Kuroki and M. Numa, Kobe Univ. (Japan)

P-5-10
A Wide-Range Tunable Level-Keeper using Vertical MOSFETs for Current-Reuse Systems
S. Tanoi[1,2] and T. Endoh[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)

P-5-11
A Reduced-Ripple PMOS Charge Pump Circuit with Small Filtering Capacitors
B. Y. Jaw and H. Lin, National Chung Hsing Univ. (Taiwan)

P-5-12
CMOS Op-amp Offset Calibration Technique Using a Closed Loop Offset Amplifier and Compact Resistor String DAC
H. Morimoto[1], H. Goto[1], H. Fujiwara[2] and K. Nakamura[1], [1]Kyushu Inst. of Tech. and [2]New Japan Radio Co. Ltd. (Japan)

P-5-13
A Twistedly-Cascaded Time Difference Amplifier for High Robustness Against Process Variation
N. Harigai, K. Niitsu, D. Oki, M. Sakurai, T. J. Yamaguchi and H. Kobayashi, Gunma Univ. (Japan)

P-5-14
An Experimental Verification of the Design Margin Analysis Method for Even-Stage Ring Oscillators with CMOS Latch
Y. Hirakawa, N. Mimura, A. Motomura and K. Nakamura, Kyushu Inst. of Tech. (Japan)

P-5-15
Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS
Q. Bu, N. Li, H. Asada, K. Okada and A. Matsuzawa, Tokyo Tech (Japan)

P-5-16
MOS Power Cells for Output Power Levels of 17 to 23 dBm
R. L. Wang[1], C. H. Liu[2], C. C. Chuang[2], C. H. Tu[3], Y. Z. Juang[3] and Y. K. Su[2], [1]National Kaohsiung Normal Univ., [2]National Cheng Kung Univ. and [3]National Chip Implementation Center (Taiwan)

P-5-17
Power Amplifier for E-band Wireless Link Using 0.1μm GaAs pHEMT
M. Kang, B. Kim, K. Kim and W. Byun, ETRI (Korea)

Area 6: Compound Semiconductor Electron Devices and Related Technologies
(12 Papers)

P-6-1
Hot Carrier Effect on RF Characteristics of High-k/Metal Gate SiGe Channel pMOSFETs
E. Y. Jeong[1], H. C. Sagong[1], D. Y. Choi[1], C. W. Sohn[1], J. S. Lee[1], C. Y. Kang[2] and Y. H. Jeong[1], [1]POSTECH and [2]SEMATECH (Korea)

P-6-2
Effect of Etch Damage on Device performance in Trench-gate and Mesa-gate GaN Vertical MOSFET
K. W. Kim[1], S. D. Jung[1], M. K. Kwon[1], R. H. Kim[1], D. S. Kim[1], K. S. Im[1], H. S. Kang[1], C. H. Won[1], K. I. Jang[1], J. H. Lee[2], K. S. Kim[2] and J. H. Lee[1], [1]Kyungpook National Univ. and [2]Samsung LED (Korea)

P-6-3
Electrical and Photo-response Properties of Titanium Contacts on n-type N-face and Ga-face GaN Layer for Vertical Power Devices Prepared by ELOG and Laser Lift-off
D. K. Kim[1], C. J. Lee[1], Y. J. Kwon[1], J. Y. Yun[1], D. S. Kim[1], H. B. Lee[2], J. H. Lee[1] and S. H. Hahm[1], [1]Kyungbook National Univ. and [2]Samsung LED (Korea)

P-6-4
Plasma-Induced Damage of GaN and Its Recovery by Atomic Hydrogens at a Room Temperature
Y. Lu[1], S. Chen[1], R. Kometani[1], K. Takeda[1], H. Kondo[1], T. Egawa[2], K. Ishikawa[1], H. Amano[1], M. Sekine[1] and M. Hori[1], [1]Nagoya Univ. and [2]Nagoya Inst. of Tech. (Japan)

P-6-5
Temperature Dependent Characteristics of Fe/n-GaN Schottky Diodes
R. Adari[1], B. Sarkar[1], T. Patil[1], D. Banerjee[1,2], P. Suggisetti[1], S. Ganguly[1] and D. Saha[1], [1]Center of Excellence in Nanoelectronics and [2]IITB-Monash Research Academy (India)

P-6-6
Air-Gap Capacitance-Voltage Analyses of InP Surfaces after Wet and Dry Processes
T. Yoshida, Shimane Univ. (Japan)

P-6-7
High-Voltage AlGaN/GaN HEMTs on Si Substrate with Implant Isolation
C. J. Yu[1], C. F. Huang[1], P. J. Chu[1], K. Y. Chen[1], S. S. H. Hsu[1], H. C. Chiu[2] and F. Zhao[3], [1]National Tsing Hua Univ., [2]Chang Gung Univ. and [3]Univ. of South Carolina (Taiwan)

P-6-8
Investigation of Plasma-Induced Damages in GaN with Different Processing
C. Y. Lee, H. Sekiguchi, H. Okada and A. Wakahara, Toyohashi Univ. of Tech. (Japan)

P-6-10
2D Device Simulation of AlGaN/GaN HFET Current Collapse Caused by Deep Levels in GaN Buffer Layer
Y. Ikawa, T. Hosokawa, Y. Kio, J. P. Ao and Y. Ohno, Univ. of Tokushima (Japan)

P-6-11
Deep levels in n-GaN Doped with Carbon Studied by Deep Level and Minority Carrier Transient Spectroscopies
U. Honda[1], Y. Yamada[1], Y. Tokuda[1] and K. Shiojima[2], [1]Aichi Inst. of Tech. and [2]Univ. of Fukui (Japan)

P-6-12 (Late News)
An Al_2O_3/InSb/Si MOS Diode Having an Ultra-Thin InSb Layer
A. Kadoda[1], T. Iwasugi[1], K. Nakatani[1], K. Nakayama[1], M. Mori[1], K. Maezawa[1], E. Miyazaki[2] and T. Mizutani[2], [1]Univ. of Toyama and [2]Nagoya Univ. (Japan)

Area 7: Photonic Devices and Optoelectronic Integration
(30 Papers)

P-7-1
GaN-based LED with embedded air voids array structure
D. S Kuo, S. J. Chang, T. K. Ko[2], W. Y. Yen[2] and S. J. Hon[2], National Cheng Kung Univ. (Taiwan)

P-7-2
Investigation of Efficiency Droop for UV-LED with N-type AlGaN Layer
Y. C. Chen[1], C. C Tu[2], J. R. Chang[1], P. M. Tu[1], S. P. Chang[1], S. S. Yen[1], Y. C. Chen[1], H. C. Kuo[1] and C. Y. Chang[1], [1]National Chiao Tung Univ. and [2]Chung Yuan Christian Univ. (Taiwan)

P-7-3
Nanoscale epitaxial lateral overgrowth of GaN-based light-emitting diodes on a SiO_2 nanorod-array patterned sapphire template
C. H. Chiu[1], C. C. Lin[1], C. H. Wang[1], S. P. Chang[1,2], C. Y. Jang[1], Z. Y. Li[1], H. C. Yang[2], H. C. Kuo[1], T. C. Lu[1] and S. C. Wang[1], [1]National Chiao Tung Univ. and [2]Epistar Co. Ltd. (Taiwan)

P-7-4
Enhanced Light Output of Vertical GaN-Based LEDs with Surface Roughening Using IZO Nano Roughened
P. R. Wang, S. J. Wang, D. M. Kuo, C. H. Kuo, H. R. Kuo, T. H. Lin and P. H. Wang, National Cheng Kung Univ. (Taiwan)

P-7-5
Elucidating the electrical characteristics of an inversion domain boundary in p-type GaN of light-emitting diodes
Y. S. Wang[1], M. C. Hsieh[1], J. F. Chen[1], J. B. Huang[2] and N. C. Chen[3], [1]National Chiao Tung Univ., [2]National Taiwan Univ. of Sci. and Tech. and [3]Chang Gung Univ. (Taiwan)

P-7-6
Deep UV Light Emitting Diodes on AlN Templates Grown by Commercialized MOCVD (‹1200℃)
M. Kurouchi, T. Takeuchi and Y. Aoyagi, Ritsumeikan Univ. (Japan)

P-7-7
An *n*-ZnO/*p*-GaN Ultraviolet Light Emitting Diode Prepared Using Radio-Frequency Magnetron Cosputtering System
N. J. Wu[1], C. P. Hsu[2], Y. J. Tsai[2], B. T. Lai[1] and D. S. Liu[1], [1]National Formosa Univ. and [2]ITRI (Taiwan)

P-7-8
Low efficiency droop of InGaN/GaN blue LEDs with super-lattice active structure
S. P. Chang[1,2], J. R. Chang[1], B. M. Tu[1], Y. C. Chen[1], K. P. Sou[1], Y. C. Hsu[1], S. S. Yen[1], Y. J. Li[1], H. C. Yang[2], T. C. Hsu[2], H. C. Kuo[1] and C. Y. Chang[1], [1]National Chiao Tung Univ. and [2]Epistar Corp. Ltd. (Taiwan)

P-7-9
Design of Optically Pumped PbS-Based Mid-Infrared Surface Emitting Lasers
Y. Sugiyama, K. Kodama, Y. Isaji, T. Yokoyama, S. Kobayashi, Y. Takano and A. Ishida, Shizuoka Univ. (Japan)

P-7-10
The Fabrication of a multiple Outputs Semiconductor Ring Laser Diode and its Output Characteristics
M. C. Shih, C. S. Chen and W. H. Lan, National Univ. of Kaohsiung (Taiwan)

P-7-12
Strudy on Structure Dependent Optical Characteristics of GaAs-related Photonic Crystal Cavities
K. Nakano, R. Nakao, H. Nagatomo, K. Kukita, K. Uwai, F. Ishikawa, M. Morifuji and M. Kondow, Osaka Univ. (Japan)

P-7-13
Enhanced localized surface plasmon resonance in a stacked structure
H. H. Chen, Y. T. Chang, C. W. Yu, S. Y. Huang, F. T. Chuang and S. C. Lee, National Taiwan Univ. (Taiwan)

P-7-14
Low-temperature Photoluminescence Characteristics of GaAs Quantum-well Waveguides
Y. Nagao, Y. Kuwamura, A. Nizamuddin, T. Nakahora, T. Hotani, N. Katsuki and T. Katsuyama, Univ. of Fukui (Japan)

P-7-15
Band-pass Optical Filter in Light-induced Self-written Waveguide
H. Watanabe[1], M. Tomiki[1], H. Sakata[1], T. Yamashita[2], A. Kawasaki[2] and M. Kagami[2], [1]Shizuoka Univ. and [2]Toyota Central R&D Labs. (Japan)

P-7-16
Basic Study of Coupling on 3D Cross of Si Photonic Wire waveguide for Optical Interconnection on Inter/inner-chip
K. Furuya[1,2], T. Takei[1,2], T. Kamei[1,2], Y. Sakakibara[1,2] and M. Mori[1,2], [1]AIST and [2]PECST (Japan)

P-7-17
Fabrication and Characterization of InGaAs/InAlAs Multiple FACQW Structures with Larger Tolerance to Impurity in Intrinsic Layer
Y. Amma and T. Arakawa, Yokohama National Univ. (Japan)

P-7-18
Numerical Demonstration of InP 1xN Planar Optical Switch Based on Beam Deflection
S. Che, M. Zaitsu, A.Higo, T. Tanemura and Y. Nakano, Univ. of Tokyo (Japan)

P-7-19
Effect of Plasma Processes on the Characteristics of GaAs Related Optical Device Structure
A. Watanabe, F. Ishikawa and M. Kondow, Osaka Univ. (Japan)

P-7-20
Characterization of the Oxide Film Obtained by Wet Oxidation of $Al_xGa_{1-x}As$ with x=0.55-0.99
Y. Hirai, T. Yamada, M. Kondow and F. Ishikawa, Osaka Univ. (Japan)

P-7-21
Structural and luminescence properties of highly crystalline ZnO nanoparticles prepared by sol-gel method
W. Bousslama[1], H. Elhouichet[1,2], B. Gelloz[3], B. Sieber[4], M. Moreau[4], M. Férid[1] and N. Koshida[3], [1]Centre National de Recherches en Sciences des Matériaux, [2]Faculté des Sciences de Tunis, [3]Tokyo Univ. of Agri. and Tech. and [4]Université Lille 1 (Tunisia)

P-7-22
Reduction of Hydrogen Annealing Temperature for Shape Transformation of Si Surface by Very Short Water Rinse
M. Fukuyama, Y. Amemiya and S. Yokoyama, Hiroshima Univ. (Japan)

P-7-23
Optical fiber sensor with multimode interference structure
Y. Matsumoto, S. Taue, K. Tsuruta and H. Fukano, Okayama Univ. (Japan)

P-7-24
Periodic Arrangement of Au Nanoparticles on SOI Photodiode for Absorption Enhancement
A. Ono, H. Satoh, R. Kawai and H. Inokawa, Shizuoka Univ. (Japan)

P-7-25
Enhanced Light Sensitivity of Thin SOI Photodiode by Metal Line-and-Space Grating of Various Materials
H. Satoh, H. Inokawa and A. Ono, Shizuoka Univ. (Japan)

P-7-26
Wavelength Sensitive PIN Photodetector Using Guided Mode Resonance
K. W. Lai, S. D. Lin, Y. J. Fu and Y. S. Li, National Chiao Tung Univ. (Taiwan)

P-7-27
Active Layer Thickness Dependence of the Bandwidth of Amorphous Silicon Photoconductors
T. Maruyama, H. Otosaka and K. Iiyama, Kanazawa Univ. (Japan)

P-7-28
A Visible Light Blinded Photo-detector With an ITO/ZST/Si MIS Device Structure
K. E. Chiu, Y. Y. Lin, Y. C. Sun, M. C. Shih and W. H. Lan, National Univ. of Kaohsiung (Taiwan)

P-7-29
GaN-based MIS Ultra-violet Photodetectors with the CsF current suppressing Layer
C. H. Chen, C. M. Tsai, C. F. Cheng, S. F. Yen and P. Y. Su[1], Cheng Shiu Univ. (Taiwan)

P-7-30
Performance Improvement of 850nm Si Photodiodes by Symmetric Layout in Standard 0.18 µm CMOS Technology
F. P. Chou[1], G. Y. Chen[1], C. W. Wang[1], Z. Y. Li[1], Y. C. Liu[2], W. K. Huang[3] and Y. M. Hsin[1], [1]National Central Univ., [2]HTC Corp. and [3]Novatek Microelectronics Corp. (Taiwan)

Area 8: Advanced Material Synthesis and Crystal Growth Technology
(24 Papers)

P-8-1
Selective-area growth of 4-color InAs-QD ensembles for broadband light source
K. Takeuchi[1], N. Ozaki[1], S. Ohkouchi[2], N. Ikeda[3], Y. Sugimoto[3], K. Asakawa[4] and R. A. Hogg[5], [1]Wakayama Univ., [2]NEC Corp., [3]NIMS, [4]Univ. of Tsukuba and [5]Univ. of Sheffield (Japan)

P-8-2
Characterization of highly stacked InGaAs quantum dots structures grown with ultrahigh-rate MBE growth technique
F. Tanoue[1,2], H. Sugawara[1], K. Akahane[2] and N. Yamamoto[2], [1]Tokyo Metropolitan Univ. and [2]NICT (Japan)

P-8-3
Field Emission Properties of 10-nm Pillars of Organics Fabricated by Pt particles and Plasma Etching
T. Suzuki[1], K. Takeda[1,4], H. Kondo[1], K. Ishikawa[1], Y. Setsuhara[2,4], M. Shiratani[3,4], M. Sekine[1,4] and M. Hori[1,4], [1]Nagoya Univ., [2]Osaka Univ., [3]Kyushu Univ. and [4]CREST-JST (Japan)

P-8-4
Self-induced InAs nanowires grown on natural-oxide-covered Si(111) by molecular-beam epitaxy
S. Wang, X. Yu, H. Wang and J. Zhao, Chinese Academy of Sci. (China)

P-8-5
Epitaxial graphene produced by thermal decomposition of TiC
W. Norimatsu[1,2], K. Kimura[1] and M. Kusunoki[1,2], [1]Nagoya Univ. and [2]JFCC (Japan)

P-8-6
Forms of CVD-grown graphene layers on polycrystalline nickel
K. Kanzaki, H. Hibino and T. Makimoto, NTT Basic Res. Labs. (Japan)

P-8-7
Influence of Annealing Atmosphere on the Epitaxial Graphene Growth on 3C-SiC (111)/Si (111)
H. R. Aryal, K Fujita and T. Egawa, Nagoya Inst. of Tech. (Japan)

P-8-8
Graphene Synthesis on Cu-Ni alloy by Chemical Vapor Deposition
E. Kim[1], Y. S. Kim[1], S. H. Chun[1], W. G. Lee[2] and J. Jung[1], [1]Sejong Univ. and [2]National Nano Fab Center (Korea)

P-8-9
Quantum Chemical Molecular Dynamics Simulation on Si Thin-film Crystal Growth for Solar Cells
T. Kuwahara, Y. Higuchi, N. Ozawa, T. Shimazaki and M. Kubo, Tohoku Univ. (Japan)

P-8-10
Growing high crystallinity Ge NCs on patterned Si substrate by post thermal annealing
C. W. Chiu, T. W. Liao and C. H. Kuan, National Taiwan Univ. (Taiwan)

P-8-11
Polytype transformation path on 4H-SiC during top-seeded solution growth
S. Harada, Alexander, K. Seki, Y. Yamamoto and T. Ujihara, Nagoya Univ. (Japan)

P-8-12
Alignment of In-plane Crystallographic Grain Orientations in Polycrystalline Si Films by Normal and Oblique-Angle Ion-Implantations
A. Nakajima[1], S. Kuroki[2], S. Fujii[2] and T. Ito[1], [1]Hiroshima Univ. and [2]Tohoku Univ. (Japan)

P-8-13
Novel Direct Patterning Technique of Vapor-Deposited Si Thin Films by Laser-Induced Si/Ag Layer Exchange
M. Kiyooka and H. Ikenoue, Kochi National College of Tech. (Japan)

P-8-14
Excimer laser crystallization of a-Ge nanowires on Si substrate
T. W. Liao, Y. K. Wu, C. W. Chiu, H. M. Chen and C. H. Kuan, National Taiwan Univ. (Taiwan)

P-8-15
Characterization of GaGdN/AlGaN/GaGdN Triple-layer Structures with High Gd Concentration for Tunneling Magnetoresistance Devices
K. Higashi, D. Abe, Y. Mitsuno, S. Komori, S. Sano, S. Hasegawa and H. Asahi, Osaka Univ. (Japan)

P-8-16
Molecular Beam Epitaxy of AlGaPN alloys for Optical Confinement structure of Monolithic Optoelectyonic Integrated Circuits on Si Substrate.
K. Kumagai, T. Kawai, K. Yamane, H. Sekiguchi, H. Okada and A. Wakahara, Toyohashi Univ. of Tech. (Japan)

P-8-17
Improving Si Doping Efficiency in GaAsN Epilayers by Using (211)B and (311)B GaAs Substrates
X. Han, M. Inagaki, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-8-18
Quality improvement of GaN grown on Si (111) using metal-organic vapor-phase epitaxy
C. W. Hsu, J. H. Lin, Y. F. Chen and Y. K. Su, National Cheng Kung Univ. (Taiwan)

P-8-19
Controlling the Immobilized process of Au NPs onto TiO_2(110) through Electrostatic Interaction of Ionic Liquids
S. Suzuki[1], Y. Ohta[1], T. Kurimoto[1], S. Kuwabata[2,3] and T. Torimoto[1,3], [1]Nagoya Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)

P-8-22
The bias-crystallization mechanism on structural characteristics and electrical properties of Zn-In-Sn-O film
K. J. Chen, F. Y. Hung, S. J. Chang, T. S. Lui, S. P. Chang, Z. S. Hu, T. P. Chen and T. Y. Liao, National Cheng Kung Univ. (Taiwan)

P-8-23
Growth of ZnMgTe/ZnTe Waveguide Structures and Analysis of the Light Polarization with the Electric Field
Y. Kumagai and M. Kobayashi, Waseda Univ. (Japan)

P-8-24
Optical Properties of Ordered arrays of Silica-Metal Core-Shell Nanoparticles
K. Sugawa[1], T. Sakai[1], D. Tanaka[1], J. Otsuki[1] and T. Akiyama[2], [1]Nihon Univ. and [2]Univ. of Shiga Prefecture (Japan)

P-8-25
Photoluminescence and conduction type of $Mg_xZn_{1-x}O$:(N,Cu) films
S. K. Mohanta, A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan)

Area 9: Physics and Application of Novel Functional Devices and Materials
(19 Papers)

P-9-1
Photo-rechargeable Battery Based on Photo-induced Copper Intercalation into Quasi-One-Dimensional Compound $KFeS_2$
S. Takenoshita, R. Yatabe, M. Kozaki, H. Kuriyaki and K. Toko, Kyushu Univ. (Japan)

P-9-2
Gap Plasmon Enhancement on a Silver Nanowire with AFM Metal Tip
Y. C. Wang[1,2], C. T. Yuan[1], M. Y. Kuo[1], M. C. Wu[2], J. Tang[1] and M. H. Shih[1], [1]National Tsing Hua Univ. and [2]Academia Sinica (Taiwan)

P-9-3
Observation of cavity polaritons in one-dimensional photonic crystal with organic dye J-aggregates
K. Ishii, M. Yamashima, Y. Kondo, S. Nakanishi and N. Tsurumachi, Kagawa Univ. (Japan)

P-9-4
Phonon-Assisted Band-to-Band Luminescence and Carrier Recombination Processes in $SrTiO_3$
Y. Yamada and Y. Kanemitsu, Kyoto Univ. (Japan)

P-9-5
Effects of Interface Grading on Electronic States in Columnar Type-II Quantum Dots
T. Kawazu, NIMS (Japan)

P-9-6
Dynamic Nuclear Polarization Induced by Breakdown of Even-integer Quantum Hall Effect
S. Umezawa[1], R. Moriya[1], T. Yamashita[1], M. Kawamura[1,2,3], S. Masubuchi[1,3], Y. Hashimoto[1], S. Katsumoto[4] and T. Machida[1], [1]Univ. of Tokyo, [2]RIKEN and [3]PRESTO-JST (Japan)

P-9-7
A Multi-purpose Electrostatically Defined Silicon Quantum Dot Structure
M. A. Sulthoni, T. Kodera, Y. Kawano and S. Oda, Tokyo Tech (Japan)

P-9-8
Time-resolved observation of carrier and coherent phonon in 4H-SiC under off-resonant excitation
K. Kato, K. Oguri, A. Ishizawa, H. Nakano and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-9-9
First-Principles Study of Electronic Structures of AlN/GaN Superlattices
K. Kamiya[1], M. Kasu[2] and K. Shiraishi[1], [1]Univ. of Tsukuba and [2]NTT Basic Res. Labs. (Japan)

P-9-11
Effect of Capping Layer Growth on Bound Exciton Luminescence in Nitrogen δ-Doped GaAs
Y. Harada, T. Kubo, T. Inoue, O. Kojima and T. Kita, Kobe Univ. (Japan)

P-9-12
Electron emission properties of GaAsN/GaAs quantum well containing N-related localized states: the influence of illuminance
M. C. Hsieh, J. F. Wang, K. H. Tseng, C. H. Chao, Y. C. Chi, R. C. C. Chen, C. H. Yang, Y. S. Wang, C. H. Chiang and J. F. Chen, National Chiao Tung Univ. (Taiwan)

P-9-13
Electrical Characteristics and TDDB Reliability of $ZrO_2/Al_2O_3/ZrO_2$ Stack High-κ Gate Dielectric
C. L. Lin[1], S. C. Wu[1], C. C. Tang[1] and M. Y. Li[2], [1]Feng Chia Univ. and [2]ProMOS Tech. Inc. (Taiwan)

P-9-14
Retention characteristics of resistance switching memory using $Si/CaF_2/CdF_2$ quantum-well structures
M. Watanabe and K. Uryu, Tokyo Tech (Japan)

P-9-15
Two Terminal Switching Device for Spin Transfer Torque (STT) MRAM
G. H. Kil, H. J. Yang, S. H. Lee and Y. H. Song, Hanyang Univ. (Korea)

P-9-16
P-type Tunneling Transistors with Poly-Si by Sequential Lateral Solidification (SLS) Growth Technique
M. H. Lee, T. H. Wu and S. C. Weng, National Taiwan Normal Univ. (Taiwan)

P-9-17
***In-situ* TEM Observation for Formation of Au Nanowires and Nanogaps caused by Electromigration**
Y. Murakami, M. Arita, K. Hamada and Y. Takahashi, Hokkaido Univ. (Japan)

P-9-18
Optical selection rules for graphene nanoribbons
K. Sasaki, K. Kato, Y. Tokura and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-9-19
Tunnel Spin Injection into Graphene Using Al_2O_3/PTCA Barrier Grown by Atomic Layer Deposition
T. Yamaguchi[1], S. Masubuchi[1], K. Iguchi[1], R. Moriya[1] and T. Machida[1,2], [1]Univ. of Tokyo and [2]PRESTO-JST (Japan)

P-9-20 (Late News)
Si-Nanowire-Based Memristors Constructed Using Top-Down Methods for Flexible Electronic Systems
T. Moon[1], J. Kang[1], Y. Han[1], C. Kim[2], Y. Jeon[1], H. Kim[1] and S. Kim[1], [1]Korea Univ. and [2]Lawrence Berkeley National Laboratory (Korea)

Area 10: Organic Materials Science, Device Physics, and Applications
(20 Papers)

P-10-1
Formation of Organic Nanodots Using Diamine Derivative and Self-Assembled Monolayer
T. Morimoto[1], S. G. Park[1], T. Inden[1], T. Nishikawa[2] and T. Mori[1], [1]Nagoya Univ. and [2]Iwate Univ. (Japan)

P-10-2
Thermal Annealing Effects on Aligned π-Conjugated Polymer Films Fabricated by Capillary Action
T. Higashi, N. Yamasaki, H. Utsumi, H. Yoshida, A. Fujii and M. Ozaki, Osaka Univ. (Japan)

P-10-3
Fabrication and Characterization of Uniaxially Oriented Vinylidene Fluoride Oligomer Thin Films
Y. Kuroda, Y. Koshiba, M. Misaki, S. Horie, K. Ishida and Y. Ueda, Kobe Univ. (Japan)

P-10-4
Enhancing the performance of pentacene-based organic thin film transistors by inserting alternately stacked NPB and Alq_3 buffer layers
C. M. Wu, S. H. Su, W. C. Weng, H. L. Tsai and M. Yokoyama, I-Shou Univ. (Taiwan)

P-10-5
Charge transport through film surface and substrate interface in solution-processed polymer field-effect transistors
K. Takagi[1], T. Nagase[1,2], T. Kobayashi[1,2], T. Kushida[3] and H. Naito[1,2], [1]Osaka Prefecture Univ. and [2]Teijin Ltd. (Japan)

P-10-6
Light-Emitting Field-Effect Transistors Having Metal Electrodes Modified with an Organic Thin Film
A. Okada, Y. Fukaya, S. Hotta and T. Yamao, Kyoto Inst. of Tech. (Japan)

P-10-7
High Transparent Conductive Film by Self-Assembled Silver Nanoparticles Network Electrode with Anti-Reflective Coating
K. Fujimoto[1], S. Shiratori[1], K. Yamane[2], K. Nakata[2] and K. Tamari[2], [1]Keio Univ. and [2]Toda Kogyo Corp. (Japan)

P-10-8
Crystalline quality variations in epitaxial-grown C_{60} thin films by magnesium atoms doping.
C. Morales, N. Kojima, S. Nishi, N. Ogata and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-10-9
Metal patterning for organic electronics based on metal undeposition effect on soft polymer surfaces
K. Tsuji and T. Tsujioka, Osaka Kyoiku Univ. (Japan)

P-10-10
Change in Capacitance of Organic Light-Emitting Diodes
T. Inden[1], T. Satoh[2], S. G. Park[1], T. Morimoto[1], T. Nishikawa[3] and T. Mori[1], [1]Nagoya Univ., [2]Toyota Central Research & Development Labs. and [3]Iwate Univ. (Japan)

P-10-11
Dependence of additive-solvent on bulk-heterojunction organic photovoltaic cell fabricated by electrospray deposition method
K. Takagi[1,2], T. Asano[1,2], T. Fukuda[1,2], Z. Honda[1], N. Kamata[1], H. Shirai[1], J. Ju[2], Y. Yamagata[2] and Y. Tajima[2], [1]Saitama Univ and [2]RIKEN (Japan)

P-10-12
Fabrication of the inverted bulk heterojunction organic solar cell on titanium oxide nanosheet
Y. Maruyama and E. Itoh, Shinshu Univ. (Japan)

P-10-13
Relationship between the work function of the hole collection electrode and the temperature dependence of open-circuit voltage in multi layered organic solar cells
T. Shirotori and E. Itoh, Shinshu Univ. (Japan)

P-10-14
Improvement of hole injection characteristics in multilayered organic photovoltaic devices by the insertion of organic interfacial layer
S. Nakagoshi and E. Itoh, Shinshu Univ. (Japan)

P-10-15
Doping Effects of Liquid Crystalline Phthalocyanine in Bulk Heterojunction Polymer Solar Cells
T. Masuda[1], T. Hori[1], N. Fukuoka[1], Y. Miyake[1,2], D. Q. Duy[1], T. Hayashi[1], T. Kamikado[1], H. Yoshida[1], A. Fujii[1], Y. Shimizu[2] and M. Ozaki[1], [1]Osaka Univ. and [2]AIST (Japan)

P-10-16
Fundamental Study on Organic Solar Cells based on Soluble ZnPc
I. Yamada[1,2], M. Umeda[1], Y. Hayashi[1], T. Soga[1] and N. Shibata[1], [1]Nagoya Inst. of Tech. and [2]Suzuka National College of Tech. (Japan)

P-10-17
The examination of the most appropriate size of ZnO nanorods in organic-inorganic hybrid solar cells
T. Ichikawa and S. Shiratori, Keio Univ. (Japan)

P-10-18
Fabrication and Evaluation of Organic Photoelectric Conversion Devices using Electrodeposited Polyaniline Films as a Hole Transporting Layer
K. Inoue, A. Suzuki, T. Oku and T. Akiyama, Univ. of Shiga Prefecture (Japan)

P-10-19 (Late News)
Fullerene Memory Transistors with a Chargeable Polymer
D. T. Toan, H. Sakai, T. Matsushima and H. Murata, JAIST (Japan)

P-10-20 (Late News)
Printed OTFT-backplane for Electrophoretic Display Characterized by High Uniformity of Performance over a Large Area
J. W. Hwang, G. S. Ryu, J. S. Kim and C. K. Song, Dong-A Univ. (Korea)

Area 11: Micro/Nano Electromechanical Systems and Bio/Medical Analyses
(14 Papers)

P-11-1
Quantitative characterization of guided motion of dynein-microtubule system
N. Ashikari[1,2], Y. Shitaka[2], H. Sakaue[1], T. Takahagi[1], H. Kojima[2], K. Oiwa[2] and H. Suzuki[1], [1]Hiroshima Univ. and [2]NICT (Japan)

P-11-2
Label-free detection of creatinine using a disposable poly-N-isopropylacrylamide as an encapsulating enzyme material based on high-κ $Eu_2Ti_2O_7$ EIS devices
T, M, Pan[1], P. Y. Liao[1], K. Y. Chang[1], C. W. Lin[1] and L. Chi[2], [1]Chang Gung University and [2]Westfälische Wilhelms-Univ. Münster (Taiwan)

P-11-3
Development of Implantable Si Neural Probe with Stimulus and Recording Electrodes for Deep Brain Stimulation
Y. Yukita, S. Lee, S. Kanno, K. Lee, T. Fukushima, M. Koyanagi, N. Katayama, H. Mushiake and T. Tanaka, Tohoku Univ. (Japan)

P-11-4
Band-to-Band Tunneling Transistor for Application to Bio Sensor
T. Tabei, K. Shibahara and S. Yokoyama, Hiroshima Univ. (Japan)

P-11-5
Scaling of the Pull-In Voltage in a Novel CMOS-compatible NEMS Switch
D. J. Baek, S. J. Choi, D. I. Moon and Y. K. Choi, KAIST (Korea)

P-11-6
Photoresist Spray Coating Using Aperture toward Trench-type 3D Microdevices
N. Fukuda, S. Kumagai and M. Sasaki, Toyota Technological Inst. (Japan)

P-11-7
Analysis of Sharp Dip Structures on THz Transmission Spectra of Metallic Meshes
T. Hasebe and H. Tabata, Univ. of Tokyo (Japan)

P-11-8
Realization of ion-sensitive field-effect transistor on SOI substrate with engineered sensing membrane for high stability
H. J. Jang and W. J. Cho, Kwangwoon Univ. (Korea)

P-11-9
Acceleration Sensor Based on CMOS Inverter Having Force Balanced Movable Gate Electrode
M. Suzuki[1], J. Kogure[1], K. Kitamura[1], T. Takahashi[1], S. Yokoyama[2], H. Tokunaga[3] and S. Aoyagi, [1]Kansai Univ., [2]Hiroshima Univ. and [3]M. T. C. Corp. (Japan)

P-11-10
Carbon Nanotube Network Conjugated by Nanoparticles with Defined Nanometer-Scaled Gaps
M. Kobayashi[1,2,3], S. Kumagai[3,4], K. Shiba[1,3], Y. Uraoka[2,3] and I. Yamashita[2,3], [1]Japanese Foundation for Cancer Res., [2]NAIST, [3]CREST-JST and [4]Toyota Technological Inst. (Japan)

P-11-11
Plasma Induced Damage Affecting Mechanical Properties of Silicon Microcantilevers and Effects of Thermal Annealing on Their Recovery
A. Wada[1], Y. Yanagisawa[1], M. Tomura[1], C.-H. Huang[1], S. Yamasaki[2], T. Ono[1] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)

P-11-12
Engineering Biocompatibility and Assembly in Carbon Nanotube Electrodes Using the Physicochemical Properties of Chitosan
L. Bugnicourt, S. Trigueros and S. A. Contera, Univ. of Oxford and Ecole Central de Lyon (UK)

P-11-13
Nanoparticle-Induced Crystallization of Amorphous Ge Film Using Ferritin
M. Uenuma[1,2], B. Zheng[1,2], T. Imazawa[1,2], N. Okamoto[1], M. Horita[1,2], T. Nishida[1,2], Y. Ishikawa[1,2], H. Watanabe[2,3], I. Yamashita[1,2] and Y. Uraoka[1,2], [1]NAIST, [2]CREST-JST and [3]Osaka Univ. (Japan)

P-11-14
Extending Rotation Range of Spatial Light Modulator by Metal-Induced Lateral Crystallization of Amorphous Si Using Ni Ferritin Molecules
S. Kumagai[1,3], S. Miyachi[1], H. Murase[1], I. Yamashita[2,3], Y. Uraoka[2,3] and M. Sasaki[1,3], [1]Toyota Technological Institute, [2]NAIST and [3]CREST-JST (Japan)

Area 12: Spintronics Materials and Devices
(16 Papers)

P-12-1
Investigation of Regular Arrangements of Ferromagnetic MnAs Nanoclusters for New Planar Magnetoelectronic Devices
M. T. Elm[1], M. Fischer[3], P. J. Klar[3] and S. Hara[1,2], [1]Hokkaido Univ., [2]PRESTO-JST and [3]Justus-Liebig Univ. (Japan)

P-12-2
Structure and Magnetic Properties of Diluted Magnetic Semiconductor Superlattice GaGdAs/GaAs Grown by MBE
Y. Uda, H. Miyagawa, S. Koshiba, N. Tsurumachi, S. Nakanishi, Y. Tanaka, H. Itoh and N.Takahashi, Kagawa Univ. (Japan)

P-12-3
Magnetic behaviors of (Ga,Mn)As/Co_2FeAl Bilayers grown by molecular-beam epitaxy
S. H. Nie[1,2], L. Chen[1], K. K. Meng[1], X. Z. Yu[1], L. J. Zhu[1], W. S. Yan[3], Y. G. Zhao[2] and J. H. Zhao[1], [1]Chinese Academy of Sci., [2]Tsinghua Univ and [3]Univ. of Sci. & Tech. of China (China)

P-12-4
Magnetoresistance effects in $La_{1-x}Sr_xMnO_3$/Nb-$SrTiO_3$/Co junctions
K. Tozawa, K. Kobayashi, T. Miyawaki, K. Ueda and H. Asano, Nagoya Univ. (Japan)

P-12-5
Anisotropic magnetoresistance in half-metallic Co_2MnSi epitaxial films
F. J. Yang, Y. Sakuraba and K. Takanashi, Tohoku Univ. (Japan)

P-12-6
Fabrication of $MgAl_2O_4$ thin films on ferromagnetic Heusler alloy Fe_2CrSi by reactive magnetron sputtering
N. Fukatani, K. Inagaki, K. Mari, H. Fujita, T. Miyawaki, K. Ueda and H. Asano, Nagoya Univ. (Japan)

P-12-7
Spectroscopic Detection of Double Exchange Magnetism Signatures in Mn $L_{2,3}$ and O-vacancy Spectra in $La_{1-x}Sr_xMnO_3$ Alloys with x = 0.2
G. Lucovsky[1], C. Adamo[2] and D. G. Schlom[2], [1]North Carolina State Univ. and [2]Cornell Univ. (USA)

P-12-8
Formation of Nitrogen Vacancy Adjoining to Gd Ion Doped in GaN
D. Abe, K. Higashi, S. Emura, Y. K. Zhou, S. Hasegawa and H. Asahi, Osaka Univ. (Japan)

P-12-9
Effect of GaAs Surface Structure on Tunneling Anisotropic Magnetoresistance in Epitaxial $Co_{50}Fe_{50}$/n-GaAs Junctions
T. Uemura, T. Akiho, M. Harada, K. Matsuda and M. Yamamoto, Hokkaido Univ. (Japan)

P-12-10
Different magnetic properties of $L1_0$-FePt grown on sputtered and EB deposited MgO / GaAs structures
R. Ohsugi[1], M. Kohda[1,2], T. Seki[3], M. Mizuguchi[3], K. Takanashi[3] and J. Nitta[1], [1]Tohoku Univ. and [2]PRESTO-JST (Japan)

P-12-11
Tight-binding calculation of conductance and magnetoresistance in disordered FM/graphene/FM junctions
S. Honda[1], R. Sato[2], A. Yamamura[2], T. Hiraiwa[2], H. Itoh[1] and J. Inoue[2], [1]Kansai Univ. and [2]Nagoya Univ. (Japan)

P-12-12
High-Speed-Search Nonvolatile TCAM Using MTJ Devices
S. Matsunaga, A. Katsumata, M. Natsui, T. Endoh, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)

P-12-13
Fast Switching in Magnetic Tunnel Junctions with Double Barrier Layer
A. Makarov, V. Sverdlov, D. Osintsev and S. Selberherr, TU Wien (Austria)

P-12-14
Stochastic State Transition of a Spin Torque Nano Oscillator
K. Nakada[1], S. Yakata[1,2] and T. Kimura[1,2], [1]Kyushu Univ. and [2]CREST-JST (Japan)

P-12-15
Spin-Photon Memory and Spin Transistor with Floating Gate
V. Zayets, H. Saito, S. Yuasa and K. Ando, AIST (Japan)

P-12-16 (Late News)
Temperature Dependence of Spin Relaxation Time in InAs Columnar Quantum Dots at 10 to 50 K
S. Nakanishi[1], K. Sasayama[1], Y. Oyanagi[1], R. Yamaguchi[1], S. Lu[2], L. H. Li[3], A. Fiore[4] and A. Tackeuchi[1], [1]Waseda Univ., [2]Chinese Academy of Sci., [3]Ecole Polytechnique Federale de Lausanne and [4]Eindhoven Univ. of Tech. (Japan)

Area 13: Application of Nanotubes, Nanowires, and Graphene
(28 Papers)

P-13-1
Fabrication and Characterization of InP Nanowire Light Emitting Diodes
S. Maeda[1], K. Tomioka[1,2], S. Hara[1] and J. Motohisa[1], [1]Hokkaido Univ. and [2]PRESTO-JST (Japan)

P-13-2
Analysis of Bottom Channel Effect in Silicon Nanowire FET based on Bulk-Silicon: Reduction of Parasitic Capacitance caused by SiGe layer
M. D. Ko[1], S. H. Lee[1], R. H. Baek[1], C. H. Park[1], C. W. Sohn[1], C. K. Baek[1,2], J. S. Lee[1] and Y. H. Jeong[1], [1]POSTECH and [2]NCNT (Korea)

P-13-3
A Multi Switching Current Study of Single-Electron Transistors Using Side Gate Bias Effect
J. E. Lee[1], J. W. Kim[1], J. H. Lee[1], K. C.Kang[1], J. H. Lee[1], H. C. Shin[1], K. J. Yoh[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Hokkaido Univ. (Korea)

P-13-4
Growth of GaAs Nanowires on Poly-Si by Selective-Area MOVPE
K. Ikejiri[1], K. Tomioka[1], S. Imai[2] and T. Fukui[1], [1]Hokkaido Univ. and [2]Sharp Corp. (Japan)

P-13-5
Formation of ohmic contact of InP nanowires without annealing processes
G. Zhang, S. Saito, K. Tateno, H. Gotoh and T. Sogawa, NTT Basic Res. Labs. (Japan)

P-13-6
Suppression of surface nanocrystal nucleation in growth of GaAs nanowire on Si(111) by molecular beam epitaxy
J. K. Kwoen, N. Kumagai, K. Watanabe, S. Ohkouchi, S. Iwamoto and Y. Arakawa, Univ. of Tokyo (Japan)

P-13-7
Thermoelectric power of catalyst-free GaAs nanowires grown by MBE-VLS method
J. H. Paek, M. Yamaguchi and H. Amano, Nagoya Univ. (Japan)

P-13-8
Effect of the Drain Configuration on the Current-Voltage Characteristics of Vertical Nanowire Field Effect Transistors
S. Karmalkar, V. K. Gurugubelli and K. R. K. Maheswaran, Indian Inst. of Tech. (India)

P-13-9
Graphene Gated SiO_2 Core-shell Silicon Nanowire Transistors
J. E. Jin[1], J. H. Lee[1,2], D. H. Hwang[1], D. W. Kim[1], M. J. Kim[1,2], K. S. Son[1,2], D. Whang[1,2] and S. W. Hwang[1], [1]Korea Univ. and [2]Sungkyunkwan Univ. (Korea)

P-13-10
Tunable Magnetic Properties of Rhombohedral Graphite Thin Films
N. T. Cuong[1,3], M. Otani[1,3] and S. Okada[2,3], [1]AIST, [2]Univ. of Tsukuba and [3]CREST-JST (Japan)

P-13-11
Precise control of layer number in graphene grown on Ni(111)
S. Entani, Y. Matsumoto, M. Ohtomo, P.V. Avramov, H. Naramoto and S. Sakai, JAEA (Japan)

P-13-12
Selective-area-grown graphene transistors by thermal chemical vapor deposition method
M. Okai[1], K. Tokumoto[2], T. Kyotani[2], M. Tokuda[2], K. Tsutsui[3] and Y. Wada[3], [1]Hitachi Ltd., [2]Tohoku Univ. and [3]Toyo Univ. (Japan)

P-13-13
Electronic Structure and Energetics of Corrugated Graphene Sheet
S. Okada[1,2] and T. Kawai[1,2], [1]Univ. of Tsukuba and [2]NEC Corp. (Japan)

P-13-14
Ultrafast Synthesis of Nanographene Employing an Ultrahigh-density In-liquid Al-cohol Plasma
T. Hagino, H. Kondo, H. Kano, K. Ishikawa, M. Sekine and M. Hori, Nagoya Univ. (Japan)

P-13-15
RF Transmission Line Characteristics of Graphenes
H. J. Lee, E. Kim and J. Jung, Sejong Univ. (Korea)

P-13-16
Ballistic Current Model for Graphene Nanoribbon Field-Effect Transistors
Y. Li, Y. Zhang, F. Liu, Y. Yang, Y. Wang and X. Liu, Peking Univ. (China)

P-13-17
Formation of quantum dots in monolayer graphene with an energy gap
G. Giavaras[1] and F. Nori[1,2], [1]RIKEN and [2]Univ. of Michigan (Japan)

P-13-18
Optical and electrical properties of graphene layers directly-grown by Alcohol-CVD
A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan)

P-13-19
Crystallographic and Electrical Properties of Semiconducting Graphene Nanoribbon Grown Employing CH_4/H_2 plasma
H. J. Cho, K. Takeda, H. Kondo, K. Ishikawa, M. Sekine and M. Hori, Nagoya Univ. (Japan)

P-13-20
Effect of Plasma Treatment on CVD-grown Graphene/Metal Contact
T. Kwon, H. An and J. Jung, Sejong. Univ. (Korea)

P-13-21
Development of Two-Dimensional Strain-Distribution Sensor Using Carbon Nanotube-Dispersed Resin
K. Suzuki, Y. Suzuki, Y. Ohashi, M. Ohnishi and H. Miura, Tohoku Univ. (Japan)

P-13-22
Improvement of transfer characteristics for PZT-CNT-FET by ionic liquid
S. Kataoka[1], T. Arie[1,2] and S. Akita[1,2], [1]Osaka Prefecture Univ. and [2]CREST-JST (Japan)

P-13-23
Strain Dependence of the Electronic Conductivity of Carbon Nanotubes and Graphene Sheets
M. Ohnishi, K. Suzuki and H. Miura, Tohoku Univ. (Japan)

P-13-24
Analysis of FET Operation Mechanism in SWNT Networks Using Scanning Gate Microscopy
X. Wei[1], K. Maeda[1], T. Yahagi[1], S. Shimozono[1], M. Matsunaga[1], N. Aoki[1], J. P. Bird[2] and Y. Ochiai[1], [1]Chiba Univ. and [2]Univ. at Buffalo (Japan)

P-13-27
Interfaces of High-k Gate Insulator in Carbon Nanotube FETs
K. Suzuki, Y. Ohno, S. Kishimoto and T. Mizutani, Nagoya Univ. (Japan)

P-13-28
Observation of n-type conduction in CNTFETs with Au contacts in vacuum
H. Imaeda, S. Ishii, S. Kishimoto, Y. Ohno and T. Mizutani, Nagoya Univ. (Japan)

Area 14: Photovoltaics & Power Semiconductor Devices
(21 Papers)

P-14-1
Atomic Layer Deposited Aluminum Oxide Passivation Layers for Crystalline Silicon: Effects of Deposition Temperature on Film and Interface Structures
H. Lee[1,5], N. Sawamoto[1,5], T. Tachibana[1,5], N. Ikeno[1,5], K. Arafune[2,5], H. Yoshida[2,5], S. Satoh[2,5], K. Matsumoto[3], K. Takahashi[3], T. Chikyow[4] and A. Ogura[1,5], [1]Meiji Univ., [2]Univ. of Hyogo, [3]Tokyo Electron Ltd., [4]NIMS and [5]CREST-JST (Japan)

P-14-2
Surface Recombination of Crystalline Silicon Substrates Passivated by Atomic Layer Deposited AlO_x
K. Arafune[1,5], S. Miki[1,5], R. Matsutani[1,5], J. Hamano[1,5], H. Yoshida[1,5], T. Tachibana[2,5], A. Ogura[2,5], K. Matsumoto[3], K. Takahashi[3], Y. Ohshita[4,5] and S. Satoh[1,5], [1]Univ. of Hyogo, [2]Meiji Univ., [3]Tokyo Electron Ltd., [4]Toyota Technological Inst. and [5]CREST-JST (Japan)

P-14-3
Optimization of a-Si/c-Si heterojunction solar cells by BF_2 ion implantation
T. H. Tasi, Y. C. Wu and C. H. Chen, National Tsing Hua Univ. (Taiwan)

P-14-4
Amorphous Silicon Thin Film Solar Cell Utilizing ITO Patterned Electrode
H. W. Liu, T. G. Chen, C. H. Chang and P. Yu, National Chiao Tung Univ. (Taiwan)

P-14-5
Patterned Glass Substrates for Enhanced Solar Energy Harvesting in Thin Film Solar Cells
T. G. Chen, Y. L. Tsai, M. A. Tsai, P. Yu, J. M. Shieh and H. C. Kuo, National Chiao Tung Univ. (Taiwan)

P-14-6
Electrode-Contact Enhancement in Silicon Nanowire-Array-Textured Solar Cells
C. Chen[1], R. Jia[1], H. Li[1], Y. Meng[1], S. Kasai[2] and H. Tamotsu[2], [1]Chinese Academy of Sci. and [2]Hokkaido Univ. (China)

P-14-7
Theoretical Study on the Effect of Size and Interface of Si Quantum Dots on Carrier Multiplication
S. Hirose, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, H. Takaba and A. Miyamoto, Tohoku Univ. (Japan)

P-14-8
Enhanced Conversion Efficiency of a Crystalline Silicon Solar Cell with Frustum Nanorod Arrays
Y. L. Tsai, M. A. Tsai, P. C. Tseng, H. C. Chen, H. C. Kuo and P. C. Yu, National Chiao Tung Univ. (Taiwan)

P-14-9
Transfer of $CuInS_2$ Layer by Lift-Off Process and Its Superstrate-Type Solar Cell Applications
Y. Abe, S. Osada, S. Fukamizu, Y. Oda, T. Minemoto, K. Nakanishi, T. Ohta and H. Takakura, Ritsumeikan Univ. (Japan)

P-14-10
First principles study on Cd and Zn doping in $CuInSe_2$ and related compounds
T. Maeda and T. Wada, Ryukoku Univ. (Japan)

P-14-11
N-H structure in GaAsN and interaction between N-H local vibration mode and lower frequency phonon
K. Ikeda, M. Inagaki, S. Wada, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-14-12
Thermally Activated Electron Transport in GaAsN
M. Inagaki, K. Ikeda, N. Kojima, Y. Ohshita and M. Yamaguchi, Toyota Technological Inst. (Japan)

P-14-13
Laser Annealing to Form High-Temperature Phase of FeS_2 (pyrite)
M. Umehara, Y. Takeda, H. Azuma and T. Motohiro, Toyota Central R&D Labs. Inc. (Japan)

P-14-14
Photoelectric Conversion Devices based on InP Porous Structures
R. Jinbo, T. Kudo and T. Sato, Hokkaido Univ. (Japan)

P-14-15
Hydrothermal Synthesis of TiO_2 Porous Hollow Nanospheres for Coating on the Photoelectrode of DSSCs
V. M. Mohan and K. Murakami, Shizuoka Univ. (Japan)

P-14-17
Investigation of Hot Carrier Degradation in STI-based High-Voltage LDMOSFETs by a Novel DCIV technique
Y. He and G. Zhang, Peking Univ. (China)

P-14-18
High accurate TCAD calibration methodology realizing smart-design of integrated power devices consisting of lateral-IGBT & Diode in SOI micro-inverters
H. Kato[1], S. Harada[1], C. S. Yun[2], V. Meniailenko[2], Y. Ashida[1], S. Takahashi[1] and N. Tokura[1], [1]DENSO Corp. and [2]Synopsys Inc. (Japan)

P-14-19
Current Transport Characteristics of Quasi-$Al_xGa_{1-x}N$/SiC Heterojunction Bipolar Transistors with Various Band Discontinuities
T. Okuda, H. Miyake, T. Kimoto and J. Suda, Kyoto Univ. (Japan)

P-14-20
Estimation of the Surface Recombination Velocity from Thickness dependence of the carrier Lifetime in n-type 4H-SiC Epilayers
M. Kato, A. Yoshida and M. Ichimura, Nagoya Inst. of Tech. (Japan)

P-14-21 (Late News)
Semi-Quantitative Determination of Radiative Recombination Centers in Silicon Power Devices by Cross-Sectional Cathodoluminescence
R. Sugie, K. Inoue and M. Yoshikawa, Toray Research Center Inc. (Japan)

Thursday, September 29

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
A-4: Novel III-V Devices and Applications (Area 6) (15:25-16:25) Chairs: S. Tanaka (Shibaura Inst. of Tech.) J. H. Lee (Kyungpook National Univ.)	**KM-4: Nanowire Growth and Characterization (Area 8&13)** (15:25-16:40) Chairs: T. Iwai (Fujitsu Labs. Ltd.) K. Tateno (NTT & Basic Res. Labs.)	**B-4: Organic memory and photonic devices (1) (Area 10)** (15:25-16:40) Chairs: K. Kato (Niigata Univ.) T. Shimada (Hokkaido Univ.)	**C-4: Characterization (1) (Area 2)** (15:25-16:35) Chairs: K. Ito (Kyoto Univ.) M. Kodera (Toshiba Corp.)	**D-4: Tunnel-FET (Area 3)** (15:25-16:45) Chairs: Y. Nishida (Renesas Electronics Corp.) F. L.Yang (National Nano Device Labs.)	**E-4: Junction Technology and Physics (Area 1)** (15:25-16:55) Chairs: S. Migita (AIST) T. Aoyama (Toshiba Corp.)	**F-4: e-Flash (Area 4)** (15:25-16:25) Chairs: T. Endoh (Tohoku Univ.) E. Yang (eMemory Technology Inc.)
15:25 A-4-1 **GaAsSb/InGaAs Vertical Tunnel FET with a 25 nm-wide Channel Mesa Structure** *M. Fujimatsu, H. Saito and Y. Miyamoto, Tokyo Tech (Japan)*	**15:25 KM-4-1 (Invited)** **Analysis of Nanowire Dopant Incorporation and Distribution with Atom Probe Tomography and Nano Probe Scanning Auger Microscopy** *J. Connell[1], U. Givan[1,2], J. S. Hammond[3], D. F. Paul[3], Y. Rosenwaks[2] and L. J. Lauhon[1], [1]Northwestern Univ., [2]Tel Aviv Univ. and [3]Physical Electronics Inc. (USA)*	**15:25 B-4-1 (Invited)** **Organic resistive memory device composed of hyperbranched polystyrene and gold nanoparticles** *K. Fujita[1], K. Yasui[2], M. Ozawa[2], K. Odoi[2] and H. Ichikawa[1], [1]Kyushu Univ. and [2]Nissan Chemical Industries, Ltd. (Japan)*	**15:25 C-4-1 (Invited)** **1X nm Copper and Low-k reliability** *A. Tökei and K. Croes, IMEC (Belgium)*	**15:25 D-4-1** **Device characteristics of planar-type $In_{0.53}Ga_{0.47}As$ channel band-to-band tunneling MOSFETs** *R. Iida, S. H. Kim, M. Yokoyama, N. Taoka, S. H. Lee, M. Takenaka and S. Takagi, Univ. of Tokyo (Japan)*	**15:25 E-4-1 (Invited)** **Challenges to Strained Source/Drain and Advanced Silicide for High Performance Transistors** *T. Yamaguchi, Renesas Electronics Corp. (Japan)*	**15:25 F-4-1** **A Zero Additional Process to Standard CMOS, 8F^2, Scalable Embedded Flash Memory with Drain-side Assisted Erase Scheme** *Y. Shinozuka, K. Miyaji and K. Takeuchi, Univ. of Tokyo (Japan)*
15:40 A-4-2 ***Pnp* AlGaN/InGaN Heterojunction Bipolar Light-Emitting Transistors with a Quantum Well in the Base** *K. Kumakura, T. Makimoto and H. Yamamoto, NTT Basic Res. Labs. (Japan)*	**15:55 KM-4-2** **Heteroepitaxy of Vertical InAs Nanowires on Thin Graphitic Films** *Y. J. Hong and T. Fukui, Hokkaido Univ. (Japan)*	**15:55 B-4-2** **Organic Ferroelectric FET Memory using Flat P(VDF-TeFE) thin film** *T. Kanashima, K. Yabe and M. Okuyama, Osaka Univ. (Japan)*	**15:55 C-4-2** **Characterization of Patterned SiOC film by STEM-VEELS at Lower (80kV) Acceralation Energy** *Y. Otsuka[1], Y. Shimizu[1], T. Naijou[1] and S. Ogawa[2], [1]Toray Research Center Inc. and [2]AIST (Japan)*	**15:45 D-4-2** **Design of Thin-Body Double-Gated Vertical-Channel Tunneling Field-Effect Transistors for Ultra-Low Power Logic Circuits** *M. C. Sun[1,2], S. W. Kim[1], H. W. Kim[1], G. Kim[1], H. Kim[1], J. H. Lee[1], H. Shin[1] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)*	**15:55 E-4-2** **Reduction of NiGe/*n*Ge Schottky Barrier Height by S and P Co-introduction for Metal Source/Drain in Ge *n*MOSFETs** *M. Koike, Y. Kamimuta and T. Tezuka, MIRAI-Toshiba (Japan)*	**15:45 F-4-2** **Practical Consideration of Endurance and Performance for sub-90 nm Embedded 2T-FN Flash Memory beyond Smart Card IC** *Y. K. Lee, B. Seo, J. Park, C. Jeon, Y. Jeong, S. B. Ryu, H. Yoo, Y. Kim, J. U. Han and E. Jung, Samsung Electronics Co. (Korea)*
15:55 A-4-3 **Fluidic Self-Assembly for Heterogeneous Integration of High Performance Resonant Tunneling Diodes Using Low-Melting Point Alloy Bumps** *J. Nakano, T. Shibata, T. Okatsu, M. Mori and K. Maezawa, Univ. of Toyama (Japan)*			**16:15 C-4-3** **Nano-scale Boron Mapping in Silicon Devices Using C_s-corrected STEM-EELS** *N. Nakanishi, H. Arie, Y. Kunimune, T. Ide, Y. Hirose, N. Hattori and T. Koyama, Renesas Electronics Corp. (Japan)*	**16:05 D-4-3** **Tunnel Field-Effect Transistor using InAs Nanowire/Si Heterojunction** *K. Tomioka[1,2] and T. Fukui[1], [1]Hokkaido Univ. and [2]PRESTO-JST (Japan)*	**16:15 E-4-3** **Improvement of Phosphorus Activation in In-Situ Phosphorus Doped Silicon Epitaxial Film by Cryogenic Silicon Ion-Implantation and Recrystallization Annealing** *H. Itokawa[1], S. Teehan[2], J. Li[2], P. W. DeHaven[3], N. C. Berliner[2], J. J. Demarest[2], N. R. Klymko[3], P. Ronsheim[3] and V. Paruchuri[2], [1]Toshiba America Electronic Components, Inc., [2]IBM Research at Albany Nanotech Center and [3]IBM Semiconductor Research and Development Center (USA)*	**16:05 F-4-3** **Direct Comparison of Electrical Characteristics for Double-Gate and Tri-Gate Flash Memories** *Y. X. Liu[1], T. Kamei[2], T. Matsukawa[1], K. Endo[1], S. O'uchi[1], J. Tsukada[1], H. Yamauchi[1], Y. Ishikawa[1], T. Hayashida[2], K. Sakamoto[1], A. Ogura[2] and M. Masahara[1,2], [1]AIST and [2]Meiji Univ. (Japan)*
16:10 A-4-4 **Operating Principle and Integration of In-Plane Gate Logic Devices** *Y. Komatsuzaki[1], K. Saba[1], K. Onomitsu[2], , H. Yamaguchi[2] and Y. Horikoshi[1], [1]Waseda Univ. and [2]NTT Basic Res. Labs. (Japan)*	**16:25 KM-4-4** **Low voltage operable field emission triodes with high transconductance based on laterally grown ZnO nanowires** *T. H. lin, F. S. Tsai, Y. C. Tu, R. M. Ko and S. J. Wang, National Cheng Kung Univ. (Taiwan)*	**16:25 B-4-4** **ADE-FDTD Analysis of Lasing Dynamics in Cholesteric Liquid Crystal as a Chiral Photonic Media** *T. Matsui and M. Kitaguchi, Mie Univ. (Japan)*		**16:25 D-4-4** **Tunnel Field-Effect Transistor with L-shaped Germanium Source: Device Physics and Design** *K. L. Low[1], C. Zhan[1], G. Han[1], Y. Yang[1], K. H. Goh[1], P. Guo[1], E. H. Toh[2] and Y. C. Yeo[1], [1]National Univ. of Singapore and [2]GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)*	**16:35 E-4-4** **A Study of Fermi-level Pinning in Ge Schottky and MIS Tunnel Junctions** *T. Nishimura[1,2], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]CREST-JST (Japan)*	

Coffee Break

Thursday, September 29

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
G-4: Circuits for 3D Structure (Area 5) (15:25-16:35) Chairs: H. C. Lin (National Chung Hsing Univ.) T. Koide (Hiroshima Univ.)	**H-4: Neural Interface Technology (Area 11)** (15:25-16:40) Chairs: T. Tanaka (Tohoku Univ.) Y. Taguchi (Keio Univ.)	**I-4: Novel Optical Devices (Area 7)** (15:25-16:25) Chairs: J. Fujikata (NEC Corp.) Y. Ishikawa (Univ. of Tokyo)	**J-4: Advanced MOSFETs and Transport (Area 9)** (15:25-16:40) Chairs: Y. Uraoka (NAIST) S. Kuroki (Tohoku Univ.)				
15:25 G-4-1 (Invited) **Challenges and Trends of Resistive Memory (Memristor) Based Circuits for 3D-IC Applications** *M. F. Chang[1], P. F. Chiu[2], C. H. Chuang[1], C. W. Wu[1], M. S. Ho[3], P. C. Chen[4], S. S. Sheu[2], M. J. Tsai[2] and T. K. Ku[2], [1]National Tsing Hua Univ., [2]ITRI, [3]National Chung Hsing Univ. and [4]I-Shou Univ. (Taiwan)*	**15:25 H-4-1 (Invited)** **CMOS LSI for excitation and measurement of neural activity with microelectrode array** *A. Shimada[1], T. Iwata[2], N. Nakano[2] and K. Torimitsu[1], [1]NTT Basic Res. Labs. and [2]Keio Univ. (Japan)*	**15:25 I-4-1** **Silicon Mach-Zehnder optical switch with an electric double layer phase shifter** *M. Saito, T. Kita and H. Yamada, Tohoku Univ. (Japan)*	**15:25 J-4-1** **Multi Electron Wave Packet Dynamics in Applied Electric Fields** *Y. Takada[1], Y. T. Yoon[1], T. Shiokawa[1], S. Konabe[1,3], M. Arikawa[2], M. Muraguchi[2,3], T. Endoh[2,3], Y. Hatsugai[1,2,3] and K. Shiraishi[1,3], [1]Univ. of Tsukuba, [2]Tohoku Univ. and [3]CREST-JST (Japan)*				
15:55 G-4-2 **A Block-Parallel SAR ADC for CMOS Image Sensor with 3-D Stacked Structure** *K. Kiyoyama[1,2], K. W. Lee[2], T. Fukushima[2], H. Naganuma[2], H. Kobayashi[3], T. Tanaka[2] and M. Koyanagi[2], [1]Nagasaki Institute of Applied Science, [2]Tohoku Univ. and [3]Association of Super-Advanced Electronics Technologies (Japan)*	**15:55 H-4-2** **Development of Pillar-Shaped Stimulus Electrode Array for High Efficient Stimulation of Fully Implantable Retinal Prosthesis** *Y. Watanabe, C. Kigure, K. Lee, T. Fukushima, M. Koyanagi and T. Tanaka, Tohoku Univ. (Japan)*	**15:40 I-4-2** **Terahertz radiation from a (113)B GaAs/AlAs coupled multilayer cavity by ultrashort laser pulse excitation** *S. Katoh[1], T. Takimoto[1], Y. Nakagawa[1,2], K. Morita[1], T. Kitada[1] and T. Isu[1], [1]Univ. of Tokushima and [2]NICHIA Corp. (Japan)*					
16:15 G-4-3 **Adaptive Through-Silicon-Via Control with Clustering for 3D Solid-State-Drive Boost Converter System** *K. Johguchi, T. Hatanaka and K. Takeuchi, Univ. of Tokyo (Japan)*	**16:10 H-4-3** **CMOS image sensor for fluorescent beads counting** *K. Sasagawa[1,3], K. Ando[1], T. Kobayashi[1,3], T. Noda[1,3], T. Tokuda[1,3], R. Iino[2,3], H. Noji[2,3] and J. Ohta[1,3], [1]NAIST, [2]Univ. of Tokyo and [3]CREST-JST (Japan)*	**15:55 I-4-3 (Late News)** **A High-Sensitivity Gate/Body-Tied PMOSFET-Type Photodetector with an Overlapping Control Gate** *J. Jung[1], S. H. Seo[2], S. H. Jo[1], M. Bae[1] and J. K. Shin[1], [1]Kyungpook National Univ. and [2]Samsung Mobile Display (Korea)*	**15:55 J-4-3** **Impact of Quantum Confinement on Backgate-Bias Modulated Threshold-Voltage Characteristics for Ultra-Thin-Body Germanium-On-Insulator MOSFETs** *C. H. Yu, Y. S. Wu, V. P. H. Hu and P. Su, National Chiao Tung Univ. (Taiwan)*				
	16:25 H-4-4 **Brain interface device with permeable hydrogel membrane for *in vivo* analysis of neural cells** *H. Takehara, A. Nagaoka, J. Noguchi, T. Akagi, H. Kasai and T. Ichiki, Univ. of Tokyo (Japan)*		**16:10 J-4-4** **Fabrication of spin-MOSFETs using CoFe/Mg/AlO_x/Si Tunnel Junctions for the source and drain** *T. Okishio, Y. Takamura and S. Sugahara, Tokyo Tech (Japan)*				
			16:25 J-4-5 **Strain Effects on Avalanche Multiplication in a Silicon Nanodot Array** *N. Mori[1,2], H. Minari[1,2], S. Uno[2,3], H. Mizuta[4,5] and N. Koshida[6], [1]Osaka Univ., [2]CREST-JST, [3]Ritsumeikan Univ., [4]Univ. of Southampton, [5]JAIST and [6]Tokyo Univ. of Agri. and Tech. (Japan)*				

Coffee Break

Thursday, September 29

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
A-5: Oxide Devices (Area 6) (17:05-18:20) Chairs: S. Sasa (Osaka Inst. of Tech.) T. Suzuki (JAIST)	**KM-5: Nanowire and Quantum Structures (Area 8&13)** (17:05-18:20) Chairs: T. Suemasu (Univ. of Tsukuba) L. Lauhon (Northwestern University)	**B-5: Organic memory and photonic devices (2) (Area 10)** (17:05-18:20) Chairs: T. Someya (Univ. of Tokyo) H. Usui (Tokyo Univ. of Agri. & Tech.)	**C-5: 3D Interconnect (1) (Area 2)** (17:05-18:25) Chairs: T. Fukushima (Tohoku Univ.) N. Nakano (Keio Univ.)	**D-5: Noise and Fluctuation (Area 3)** (17:05-18:25) Chairs: F. L.Yang (National Nano Device Labs.) F. Boeuf (STMicroelectronics)	**E-5: Ge Metallization (Area 1)** (17:20-18:20) Chairs: B. H. Lee (GIST) S. Migita (AIST)	**F-5: CT-Flash (Area 4)** (17:05-18:05) Chairs: S. Shuto (Toshiba Corp.) Y. Sasago (Hitachi, Ltd.)
17:05 A-5-1 **Zinc Oxide Thin-Film Transistors on Flexible Plastic Substrates and Glass Substrates Fabricated at Room Temperature** *T. Higaki, Y. Kimura, T. Maemoto, S. Sasa and M. Inoue, Osaka Inst. of Tech. (Japan)*	**17:05 KM-5-1 (Invited)** **Epitaxial metal nanocrystal-semiconductor quantum dot plasmonic nanostructures** *A. Urbańczyk[1], F. W.M. van Otten[1] and R. Nötzel[2], [1]Eindhoven Univ. of Tech. and [2]Technical Univ. of Madorid (Netherlands)*	**17:05 B-5-1** **Evaluation of Polyvinylalcohol:Rhodamine Film Deposition Using Optical Waveguide and Surface Plasmon Resonance Spectroscopies** *S. Yokoyama, K. Shinbo, Y. Ohdaira, A. Baba, K. Kato and F. Kaneko, Niigata Univ. (Japan)*	**17:05 C-5-1** **Through Silicon Via (TSV) Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current** *L. Zhang[1, 2], H. Y. Li[1], S. Gao[1] and C. S. Tan[2], [1]A*STAR and [2]Nanyang Technological Univ. (Singapore)*	**17:05 D-5-1** **Impact of Random Telegraph Noise Reduction with Buried Channel MOSFET** *H. Suzuki, R. Kuroda, A. Teramoto, A. Yonezawa, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)*	**17:20 E-5-1** **Formation and Properties of Epitaxial NiGe/Ge(110) Contacts** *J. Yokoi, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)*	**17:05 F-5-1** **A Novel Operating Scheme for 2-bit/Cell Split Gate SONOS Flash Memory** *C. H. Chou[1], S. S. Chung[1], C. H. Lee[2], T. M. Hsieh[2], J. C. Liou[2], C. H. Chen[3], P. ZP. Chen[3] and H. H. Chen[3], [1]National Chiao Tung Univ., [2]Solid State System and [3]UMC (Taiwan)*
17:20 A-5-2 **Low Temperature Processed Zinc Oxide Thin Film Transistors by Plasma Assisted Atomic Layer Deposition** *Y. Kawamura[1], M. Tani[1], N. Hattori[2], N. Miyatake[2], M. Horita[1], Y. Ishikawa[1] and Y. Uraoka[1,3], [1]NAIST, [2]Mitsui Eng. and Shipbuilding Co., Ltd. and [3]CREST-JAST (Japan)*	**17:35 KM-5-2** **Growth and Characterization of MnAs Nanoclusters Embedded in GaAs Nanowires by Metal-Organic Vapor Phase Epitaxy** *M. Yatago[1], S. Sakita[1] and S. Hara[1,2], [1]Hokkaido Univ. and [2]PRESTO-JST (Japan)*	**17:20 B-5-2** **Two-stage polarization reversal process in a pentacene/poly(vinylidene fluoride - trifluoroethylene) double-layer capacitor** *J. Li, D. Taguchi, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)*	**17:25 C-5-2** **Impacts of Microbump-Induced Local Bending Stress in 3D-LSI** *H. Kino[1], M. Murugesan[1], K. W. Lee[1], J. C. Bea[1], C. Miyazaki[2], H. Kobayashi[2], H. Shimamoto[2], T. Fukushima[1], T. Tanaka[1] and M. Koyanagi[1], [1]Tohoku Univ. and [2]ASET (Japan)*	**17:25 D-5-2** **Random Trap Fluctuation (RTF) Induced Vth Variability and the Impact on the Reliability of Strained-Silicon CMOS Devices** *E. R. Hsieh[1], C. Y. Cheng[1], S. S. Chung[1], C. H. Tsai[2], R. M. Huang[2], C. T. Tsai[2] and C. W. Liang[2], [1]National Chiao Tung Univ. and [2]UMC (Taiwan)*	**17:40 E-5-2** **Improvement of Thermal stability of Ni-Germanide with Ni/Co/Ni/TiN Structure for High Performance Ge MOSFETs** *H. S. Shin[1], S. K. Oh[1], M. H. Kang[1,2], H. M. Kwon[1], J. W. Oh[3], P. Majhi[3], R. Jammy[3] G. W. Lee[1] and H. D. Lee[1], [1]Chungnam National Univ., [2]National NanoFab Center and [3]SEMATECH (Korea)*	**17:25 F-5-2** **Re-examination of Performance and Reliability Degradation in MONOS Memory with Ultra-thin (～ 2nm) SiN Charge Trap Layers** *H. Kusai, M. Morota, M. Oda, S. Fujii, K. Sakuma and M. Koyama, Toshiba Corp. (Japan)*
17:35 A-5-3 **Effects of Excimer Laser annealing of Oxide Semiconductor Films** *M. Fujii[1], R. Ishihara[2], T. Chen[2], J. der Cingel[2], M. R. T. Mofrad[2], M. Kasami[3], K. Yano[3], M. Horita[1,4], Y. Ishikawa[1,4] and Y. Uraoka[1,4], [1]NAIST, [2]Delft Univ. of Tech., [3]Idemitsu Kosan Co., Ltd. and [4]CREST-JST (Japan)*	**17:50 KM-5-3** **Study of the Indium Content Distribution of Core-shell InGaN/GaN Multi-Quantum Wells (MQWs) on GaN Nanorods** *Y. J. Li, S. P. Chang, J. R. Chang, Y. C. Chen, K. P. Sou, Y. C. Hsu, H. C. Kuo and C. Y. Chang, National Chiao Tung Univ. (Taiwan)*	**17:35 B-5-3** **In situ Electrochemical and Transmission Surface Plasmon Resonance for Studies of Electropolymerized Poly(3-Aminobenzoic acid) Thin Film** *S. Sriwichai[1], A. Baba[2], S. Phanichphant[1], K. Shinbo[2], K. Kato[2] and F. Kaneko[2], [1]Chiang Mai Univ. and [2]Niigata Univ. (Thailand)*	**17:45 C-5-3** **Room-Temperature Bonding of LSI Chips on PEN Film Using Mechanical Caulking of Au Cone Bump** *T. Shuto, N. Watanabe, A. Ikeda and T. Asano, Kyushu Univ. (Japan)*	**17:45 D-5-3** **Uniaxial Strain Effect on Flicker Noise and Random Telegraph Noise of SiC Strained nMOSFETs in 40nm Technology** *K. L Yeh, C. S. Chang and J. C. Guo, National Chiao Tung Univ. (Taiwan)*	**18:00 E-5-3** **Marked Suppression of the Fermi-level Pinning at Atomically Matched Fe_3Si/p-Ge(111) Contacts** *K. Kasahara[1], S. Yamada[1], M. Miyao[1] and K. Hamaya[1,2], [1]Kyushu Univ. and [2]PRESTO-JST (Japan)*	**17:45 F-5-3** **Robust Data Retention and Superior Endurance SONOS Nonvolatile Memory with NH_3 Plasma Treated and Pd NCs Embedded Charge Storage Layer** *S. H. Liu[1], W. L. Yang[1], S. T. Chen[1], M. R. Ye[1] and T. S. Chao[2], [1]Feng Chia Univ. and [2]National Chiao Tung Univ. (Taiwan)*
17:50 A-5-4 **High Mobility Amorphous Indium-Gallium-Zinc Oxide Thin-Film Transistor with a Strong Reduction Capping Layer** *H. W. Zan[1], C. C. Yeh[1], C. C. Tsai[1], H. F. Meng[1] and C. C. Yeh[2], [1]National Chiao Tung Univ. and [2]E Ink Holdings Inc. (Taiwan)*	**18:05 KM-5-4** **Study on the growth of In-rich InGaAs nanowires by selective-area metal-organic vapor phase epitaxy** *Y. Kohashi, S. Hara and J. Motohisa, Hokkaido Univ. (Japan)*	**17:50 B-5-4** **Transient Absorption Decay and Photoconductive Characteristics of NPh_3-Silole Doped Fluorene Blend Film** *T. Fukuda[1], S. Kimura[1], Z. Honda[1], N. Kamata[1], K. Mori[1], K. Hatano[1] and A. Furube[2], [1]Saitama Univ. and [2]AIST (Japan)*	**18:05 C-5-4** **3D Chip Stacking of RF Devices with Cu TSV, Cu/Sn Bumps and Sealing Ring** *W. Zhang[1], B. Majeed[1], X. Sun[1], G. Posada[1], C. Diekmann[2], C. Eggs[2], E. Schmidhammer[2] and W. De Raedt[1], [1]IMEC and [2]EPCOS AG (Belgium)*	**18:05 D-5-4** **Characteristics of hot hole injection, trapping, and detrapping in gate oxide of poly-Si TFTs** *Y. Kamakura[1,2], T. Himukashi[1], H. Tsuji[1] and K. Taniguchi[1], [1]Osaka Univ. and [2]CREST-JST (Japan)*		
18:05 A-5-5 **The Influence of a SnInGaZnO Electron Barrier Layer on the performance of Low-Driving Voltage InGaZnO Thin-Film Transistors** *H. Y. Huang[1], S. J. Wang[1], C. H. Wu[2], C. K. Chiang[1], Y. C. Huang[1] and J. Y. Su[1], [1]National Cheng Kung Univ. and [2]Chung Hua Univ. (Taiwan)*		**18:05 B-5-5 (Late News)** **Antireflective Protective Coating by Ion-Assisted Vapor Deposition Polymerization of Fluoropolymer Thin Films** *K. Senda[1,2], T. Matsuda[2], K. Tanaka[2] and H. Usui[2], [1]Sumitomo Precision Products Co., Ltd. and [2]Tokyo Univ. Agri. & Tech. (Japan)*				

Rump Sessions : 5F Hall 1 “Opportunities and Challenges of Heterogeneous Integration on CMOS” - Photonics, MEMS, Sensors, etc - , 5F Hall 2 “Future Roadmap for Graphene Science and Technology”

Thursday, September 29

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
G-5: RF Circuits (1) (Area 5) (17:05-18:20) Chairs: M. Horiguchi (Renesas Electronics. Corp.) H. Morimura (NTT Microsystem Integration Labs.)		**I-5: Er-Doped Devices (Area 7)** (17:05-18:05) Chairs: A. Wakahara (Toyohashi Univ. of Tech.) H. Isshiki (The Univ. of Electro-Communications)	**J-5: MEMS & Thin-Film Devices (Area 9)** (17:05-18:20) Chairs: Y. Uraoka (NAIST) H. Inokawa (Shizuoka Univ.)				
17:05 G-5-1 **An Injection-Locked LC Frequency Divider to Achieve Wide Locking Range and Low Power Consumption** *H. M. Hsu and G. L. Fu, National Chung Hsin Univ. (Taiwan)*		**17:05 I-5-1** **A GaAs/AlAs multilayer cavity with Er-doped InAs quantum dots embedded in strain-relaxed InGaAs barriers for ultrafast all-optical switches** *H. Ueyama[1], T. Takahashi[1], Y. Nakagawa[1,2], K. Morita[1], T. Kitada[1] and T. Isu[1], [1]Univ. of Tokushima and [2]NICHIA Corp. (Japan)*	**17:05 J-5-1** **Micromechanical Characterization of Optical Absorption in a GaAs/AlGaAs Heterostructure** *T. Watanabe[1,2], H. Okamoto[1], K. Onomitsu[1], H. Gotoh[1], T. Sogawa[1] and H. Yamaguchi[1,2], [1]NTT Basic Res. Labs. and [2]Tohoku Univ. (Japan)*				
17:25 G-5-2 **A 0.1-V 13-GHz Transformer-Based Quadrature VCO with a Capacitor Coupling Technique in 90nm CMOS** *T. Kamimura, S. Lee, S. Tanoi, H. Ito, N. Ishihara and K. Masu, Tokyo Tech (Japan)*		**17:20 I-5-2** **Strong suppression of scattering loss in $Er_{0.4}Y_{1.6}SiO_5$ crystalline waveguides** *T. Nakajima[1], T. Shinagawa[1], T. Sugawara[2], Y. Jiang[2], T. Kimura[1] and H. Isshiki[1], [1]Univ. of Electro-Communications and [2]Shincron Co., Ltd. (Japan)*	**17:20 J-5-2** **Mechanical idler generation** *I. Mahboob, Q. Wilmart, K. Nishiguchi, A. Fujiwara and H. Yamaguchi, NTT Basic Res. Labs. (Japan)*				
17:45 G-5-3 **1.2-17.6 GHz Ring-VCO-Based PLL with Injection Locking in 65 nm CMOS** *S. Lee, H. Ito, S. Amakawa, S. Tanoi, N. Ishihara and K. Masu, Tokyo Tech (Japan)*		**17:35 I-5-3** **$Er_xY_{2-x}SiO_5$ compact waveguide slotted into Si photonic crystal** *T. Sato, T. Nakajima, T. Kimura and H. Isshiki, Univ. of Electro-Communications (Japan)*	**17:35 J-5-3** **Theory of Resonant Tunneling through a Donor State** *N. Mori[1], A. Patanè[2] and L. Eaves[2], [1]Osaka Univ. and [2]Univ. of Nottingham (Japan)*				
18:05 G-5-4 (Late News) **A novel approach of Cap-sharing to reduce the big loop filter capacitance in semi-digital PLL** *P. Sareen, M. Dietl and K. Dewan, Texas Instruments (Germany)*		**17:50 I-5-4** **Energy levels and interaction between Er^{3+}-ions located at the two crystalographic sites of Er_2O_3 grown on Si(111)** *H. Omi and T. Tawara, NTT Basic Res. Labs. (Japan)*	**17:50 J-5-4** **Tri-Gate Poly-Si TFTs Fabricated by CW Laser Lateral Crystallization for Improvement of Electron Transport Properties** *S. Fujii, Y. Kawasaki, S. Kuroki and K. Kotani, Tohoku Univ. (Japan)*				
			18:05 J-5-5 **Bottom Electrode Modification of ZrO_2-Based RRAM Device with Au Nanodots** *D. Y. Lee, I. C. Yao and T. Y. Tseng, National Chiao Tung Univ. (Taiwan)*				

Rump Sessions : 5F Hall 1 “Opportunities and Challenges of Heterogeneous Integration on CMOS” - Photonics, MEMS, Sensors, etc - , 5F Hall 2 “Future Roadmap for Graphene Science and Technology”

Friday, September 30

5F Hall 1

AL-6: SiC&GaN Power Switching Devices (1) (Area 6&14)
(9:00-10:45)
Chairs: R. Hattori (Mitsubishi Electric Corp.)
M. Ishiko (Toyota Central R&D Labs., Inc)

9:00 AL-6-1 (Invited)
High-Voltage SiC Power Devices for Energy Electronics
T. Kimoto and J. Suda, Kyoto Univ. (Japan)

9:30 AL-6-2
Thermodynamic Control of Interface Layer Formation in High-k Gate Stacks on 4H-SiC
S. Nakatsubo, T. Nishimura, K. Kita, K. Nagashio and A. Toriumi, Univ. of Tokyo (Japan)

9:45 AL-6-3
Characteristics of 4H-SiC p-Channel MOSFETs with Ion-Implanted Buried Channel
M. Okamoto, M. Iijima, T. Nagano, K. Fukuda and H. Okumura, AIST (Japan)

10:00 AL-6-4
A Simple Thermal Impedance Measurement of SiC JFETs with Constant Current Operation
T. Kim and T. Funaki, Osaka Univ. (Japan)

10:15 AL-6-5
Effects of Substrate Defects on the Gate Leakage Current of AlGaN/GaN Heterojunction FETs Fabricated on Na Flux Bulk GaN
R. Hasegawa[1], N. Yafune[2], H. Tokuda[1], Y. Mori[3], H. Amano[4] and M. Kuzuhara[1], [1]Univ. of Fukui, [2]Sharp Corp., [3]Osaka Univ. and [4]Nagoya Univ. (Japan)

10:30 AL-6-6
Fabrication of GaN MOSFET using Selectively Re-grown n^+-GaN Layer on Etched Source and Drain Regions
D. S. Kim, H. S. Kang, C. H. Won, C. H. Bu, K. I. Jang, C. M. Yang, K. S. Im, K. W. Kim, S. D. Jung, R. H. Kim, M. K. Kwon and J. H. Lee, Kyungpook National Univ. (Korea)

5F Hall 2

KM-6: Graphene Synthesis (Area 8&13)
(9:00-10:45)
Chairs: H. Hibino (NTT Basic Res. Labs.)
S. Tanaka (Kyushu Univ.)

9:00 KM-6-1 (Invited)
Formation of graphene nanostructures on vicinal SiC surfaces
S. Tanaka, T. Kajiwara, Y. Kurisu and K. Morita, Kyushu Univ. (Japan)

9:30 KM-6-2
Tuning of Structural and Electronic properties of Epitaxial Graphene by Substrate Microfabrication
H. Fukidome[1], H. Handa[1], M. Kotsugi[2,3], Th. Seyller[4], Y. Kawai[1], T. Ohkouchi[2], K. Horn[5], R. Takahashi[1], K. Imaizumi[1], Y. Enta[6], M. Suemitsu[1] and T. Kinoshita[2,3], [1]Tohoku Univ., [2]JASRI/SPring-8, [3]CREST-JST, [4]Friedrich-Alexander-Universität Erlangen-Nürnberg, [5]Fritz-Harber-Institut and [6]Hirosaki Univ. (Japan)

9:45 KM-6-3
Theory on Initial Stage of Epitaxial Graphene Growth on SiC(0001)
H. Kageshima[1], H. Hibino[1], H. Yamaguchi[1] and M. Nagase[2], [1]NTT Baseic Res. Labs. and [2]Univ. of Tokushima (Japan)

10:00 KM-6-4
Formation of Graphene on Diamond C(111) Surfaces by Vacuum Annealing
S. Ogawa[1], T. Yamada[2], S. Ishidzuka[3], A. Yoshigoe[4], T. Kaga[1], H. Hozumi[1], M. Hasegawa[2], Y. Teraoka[4] and Y. Takakuwa[1], [1]Tohoku Univ., [2]AIST, [3]Akita Nat. Col. Tech. and [4]JAEA (Japan)

10:30 KM-6-6
Large Area CVD Graphene Film as Transparent Electrode for Organic Electronics
G. Kalita, K. Wakita and M. Umeno, Chubu Univ. (Japan)

10F 1002

B-6: Device physics and characterization of OTFT (1) (Area 10)
(9:00-10:45)
Chairs: M. Yoshida (AIST)
M. Sakai (Chiba Univ.)

9:00 B-6-1 (Invited)
Device Physics of Organic Transistors
T. Hasegawa, AIST (Japan)

9:30 B-6-2
Direct Observation of Charge Carrier Concentrations in Operating Field-Effect Transistors of Pentacene by Electron Spin Resonance
H. Tanaka[1], M. Hirate[1], S. Watanabe[1], H. Ito[1], K. Marumoto[2,3], T. Takenobu[3,4], Y. Iwasa[5] and S. Kuroda[1], [1]Nagoya Univ., [2]Univ. of Tsukuba, [3]PRESTO-JST, [4]Waseda Univ. and [5]Univ. of Tokyo (Japan)

9:45 B-6-3
Probing ambipolar carrier injection into pentacene field effect transistors using charge modulation spectroscopy and displacement current measurement
T. Manaka, S. Kawashima, Y. Tanaka and M. Iwamoto, Tokyo Tech (Japan)

10:00 B-6-4
Four-Probe Measurements on Field-Effect Transistors of High-Mobility Conjugated Polymers
H. Ito, T. Nozaki, H. Tanaka and S. Kuroda, Nagoya Univ. (Japan)

10:15 B-6-5
Analyzing diffusion-like interfacial carrier transport process in pentacene organic field-effect transistors by time-resolved second harmonic generation and impendence spectroscopy
L. Zhang, D. Taguchi, H. Msada, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)

10:30 B-6-6
Electric and structural characterizations on annealed dinaphthothienothiophene thin-film transistors.
K. Kuribara[1], H. Wang[2], N. Uchiyama[1], K. Fukuda[1], T. Yokota[1], T. Sekitani[1], U. Zschieschang[3], C. Jaye[4], D. Fischer[4], H. Klauk[3], T. Yamamoto[5], K. Takimiya[5], M. Ikeda[6], H. Kuwabara[6], Y. L. Loo[2] and T. Someya[1], [1]Univ. of Tokyo, [2]Princeton Univ., [3]Max Planck Inst. for Solid State Res., [4]National Inst. of Standards and Tech., [5]Hiroshima Univ. and [6]Nippon Kayaku Corp., Ltd. (Japan)

10F 1003

11F 1101

D-6: Advanced CMOS Devices (Area 3)
(9:00-10:30)
Chairs: T. Hiramoto (Univ. of Tokyo)
B. Doris (IBM)

9:00 D-6-1 (Invited)
Advanced Foundry CMOS: From Planar into the Multi-Gate Era
A. Wei, GLOBALFOUNDRIES (USA)

9:30 D-6-2
Observation of Hole Velocity Enhancement in Ge-rich Strained SiGe-on-insulator Tri-gate MOSFETs
K. Ikeda, M. Oda, T. Irisawa, Y. Kamimuta, Y. Moriyama and T. Tezuka, MIRAI-Toshiba (Japan)

9:50 D-6-3
Extremely Small Within-Device Variability in Intrinsic Channel Tri-Gate Silicon Nanowire MOSFETs
K. Mao, T. Mizutani, A. Kumar, T. Saraya and T. Hiramoto, Univ. of Tokyo (Japan)

10:10 D-6-4
Enhanced Performance of Tri-Gate Transistors with Gnox Using Optimized Novel SOI Realization Technology
S. H. Kim[1,2], H. J. Bae[1], C. W. Oh[1], D. W. Kim[1], S. Yamada[1], G. Y. Jin[1] and Y. H. Roh[2], [1]Samsung Electronics Co. and [2]Sungkyunkwan Univ. (Korea)

11F 1102

E-6: Ge Process Technology (1) (Area 1)
(9:00-10:20)
Chairs: K. Kita (Univ. of Tokyo)
J. Yugami (Renesas Electronics Corp.)

9:00 E-6-1
Hybrid-Formation of (100), (110), and (111) Ge-on-Insulator Structures on (100) Si Platform
M. Kurosawa[1,2], T. Sadoh[1] and M. Miyao[1], [1]Kyushu Univ. and [2]JSPS (Japan)

9:20 E-6-2
Dual Gated Germanium Junctionless p-MOSFETs
D. D. Zhao[1,2,3], C. H. Lee[1,2], T. Nishimura[1,2], K. Nagashio[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo, [2]CREST-JST and [3]Beijing Normal Univ. (Japan)

9:40 E-6-3
Control of Surface Roughness on Ge by Wet Chemical Treatments and Its Effects on Electron Mobility in n-FETs
C. H. Lee[1,2], T. Nishimura[1,2], T. Tabata[1,2], M. Yoshida[1], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]CREST-JST (Japan)

10:00 E-6-4
Strain and Dislocation Structures of $Ge_{1-x}Sn_x$ Heteroepitaxial Layers Grown on Ge(110) Substrates
T. Asano[1], Y. Shimura[1,2], O. Nakatsuka[1] and S. Zaima[1], [1]Nagoya Univ. and [2]JSPS (Japan)

11F 1103

F-6: PRAM/ReRAM (1) (Area 4)
(9:00-10:50)
Chairs: Y. Sasago (Hitachi, Ltd.)
Y. C. Chen (Macronix International Co., Ltd.)

9:00 F-6-1 (Invited)
Entropy-controlled Phase-change Memory
J. Tominaga, P. Fons, A. Kolobov, R. Simpson and X. Wang, AIST (Japan)

9:30 F-6-2
Effect of Resistance Drift on the Activation Energy for Crystallization in Phase Change Memory
C. Ahn[1], B. Lee[1], R. G. D. Jeyasingh[1], M. Asheghi[1], G. Hurkx[2], K.E. Goodson[1] and H. S. P. Wong[1], [1]Stanford Univ. and [2]NXP-TSMC Research Center (USA)

9:50 F-6-3
Effect of Interfacial oxide layer on Switching Uniformity of $Ge_2Sb_2Te_5$ Based Resistive Switching Memory Device
J. Y. Woo, S. J. Jung, S. M. Sadaf, E. J. Cha and H. S. Hwang, Gwangju Inst. of Sci. and Tech. (Korea)

10:10 F-6-4
Improvement in resistive switching parameters by selecting the SET polarity in $IrO_x/TaO_x/WO_x$/W structure
A. Prakash[1], S. Maikap[1], C. S. Lai[1], H. Y. Lee[2], W. S. Chen[2], F. T. Chen[2], M. J. Kao[2] and M. J. Tsai[2], [1]Chang Gung Univ. and [2]ITRI (Taiwan)

10:30 F-6-5
Reset Current Reduction with Excellent Filament Controllability by using Area Minimized and Field Enhanced Unipolar RRAM structure
K. C. Ryoo[1,2], S. H. Park[1], J. H. Oh[1,2], S. H. Jung[1], H. S. Jeong[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)

Coffee Break

Friday, September 30

11F 1104

G-6: Analog and Digital Circuits (Area 5)
(9:00-10:50)
Chairs: M. Ikebe (Hokkaido Univ.)
T. Hirose (Kobe Univ.)

9:00 G-6-1
A 220nA 32-kHz Crystal Oscillator with wide Voltage Range (1.0 - 5.5 V) for Battery-Operated MCUs
O. Ozawa, M. Horiguchi, Y. Okuda, A. Anzai, T. Ito, H. Shibata and M. Hiraki, Renesas Electronics Corp. (Japan)

9:20 G-6-2
A 12b Low Power Multi-Slope ADC with Time to Digital Converter
K. Kim, M. Ikebe, A. Kondou, J. Motohisa, Y. Amemiya and E. Sano, Hokkaido Univ. (Japan)

9:40 G-6-3
Compact Multi-Bit Encoder for High Speed Frequency-Mapping Associative Memory
S. Sasaki, M. Yasuda, A. Kawabata, T. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)

10:00 G-6-4
An Efficient Image-Vector-Generation Processor for Edge-Based Complementary Feature Representations
N. Yamashita and T. Shibata, Univ. of Tokyo (Japan)

10:20 G-6-5 (Late News)
Asynchronous Pulse Transmitter for Power Reduction in ThruChip Interface
M. Saito, N. Miura and T. Kuroda, Keio Univ. (Japan)

10:35 G-6-6 (Late News)
Post-Fabrication Independent L and Q Adjustment of On-Chip Inductors by Above-CMOS Processing for Rapid Prototyping of RF SoCs
Y. Sasaki and K. Kotani, Tohoku Univ. (Japan)

11F 1107

H-6: Micro Fabrication and Micro fluidic Devices (Area 11)
(9:00-10:45)
Chairs: M. Sasaki (Toyota Technological Inst.)
T. Sakata (Univ. of Tokyo)

9:00 H-6-1 (Invited)
Wet Process Innovation based on Micro/Nano Science: Controllable Anisotropy in Silicon Etching for MEMS 3D Structuring
K. Sato, Nagoya Univ. (Japan)

9:30 H-6-2
Oxygen sensor microarray sheet for *in situ* sensing of oxygen consumption of cultivated cell
M. Kojima[1], H. Takehara[1], T. Akagi[1], H. Shiono[2] and T. Ichiki[1], [1]Univ. of Tokyo and [2]Nikon Instruments Inc. (Japan)

9:45 H-6-3
Silicon based Lab-On-a-Chip system for Single-Nucleotide-Polymorphism:Fabrication and characterization
B. Majeed[1], B. Jones[1], D. S. Tezcan[1], N. Tutun[1], L. Haspeslagh[1], S. Peeters[1], P. Fiorini[1], M. O. de Beeck[1], C. van Hoof[1], M. Hiraoka[2], H. Tanaka[2] and I. Yamashita[2], [1]Imec and [2]Panasonic corp. (Belgium)

10:00 H-6-4
Sub-micro-liter Electrochemical Single-Nucleotide-Polymorphism Detector for Lab-On-Chip System
H. Tanaka[1], P. Fiorini[2], S. Peeters[2], B. Majeed[2], T. Sterken[2], M. O. de Beeck[2] and I. Yamashita[1], [1]Panasonic Corp. and [2]Imec (Japan)

10:15 H-6-5
Recovery based nanowire field-effect transistor detection of pathogenic avian influenza DNA
C. H. Lin[1], K. N. Teng[1], C. J. Chu[2,3], C. D. Chen[2], L. C. Tsai[3] and Y. S. Yang[1], [1]National Chiao Tung Univ., [2]Academia Sinica and [3]National Taipei Univ. of Tech. (Taiwan)

10:30 H-6-6
Ultralarge-scale DNA microreactor array enabling one-step synthesis of mutant protein library on chip
S. Sato[1,2], M. Biyani[1,3], T. Akagi[1,3] and T. Ichiki[1,3], [1]Univ. of Tokyo, [2]CMSI and [3]CREST-JST (Japan)

12F 1201

CI-6: Optical Interconnect (1) (Area 2&7)
(9:00-10:45)
Chairs: M. Tokushima (AIST)
Y. Ishikawa (Univ. of Tokyo)

9:00 CI-6-1 (Invited)
Silicon Photonics in Next Generation Computers
M. R. Watts, MIT (USA)

9:30 CI-6-2 (Invited)
High Speed Optoelectronic Devices in Silicon
L. Vivien[1], D. Marris-Morini[1], G. Rasigade[1], M. Ziebell[1], P. Chaysakul[1], X. Le Roux[1], E. Cassan[1] and J. M. Fédéli[2], [1]Univ. Paris Sud and [2]CEA-LETI/MINATEC (France)

10:00 CI-6-3
Si Waveguide-Integrated MSM Ge Photodiode
J. Fujikata[1,2], M. Noguchi[1,2], M. Miura[1,2], D. Okamoto[1,2], T. Horikawa[1,3] and Y. Arakawa[1,4], [1]PECST, [2]PETRA, [3]AIST and [4]Univ. of Tokyo (Japan)

10:15 CI-6-4
Adjacent Channel Crosstalk in 0.18-µm Si CMOS Photodiode Arrays with Body Contact
G. Y. Chen, F. P. Chou, C. W. Wang and Y. M. Hsin, National Central Univ. (Taiwan)

10:30 CI-6-5
Low-operation Voltage and High-speed Silicon Ring Optical Modulator with p/n Junctions along Waveguide
Y. Amemiya, R. Furutani, M. Fukuyama and S. Yokoyama, Hiroshima Univ. (Japan)

12F 1202

J-6: Photon & Spin in Nanostructures (Area 9)
(9:00-10:45)
Chairs: H. Gotoh (NTT Basic Res. Labs.)
K. Oto (Chiba Univ.)

9:00 J-6-1 (Invited)
Acoustic transport and manipulation of carriers and spins in GaAs
P. V. Santos, K. Biermann, A. Hernández-Mínguez, S. Lazič and R. Hey, Paul Drude Institute for Solid-State Electronics (Germany)

9:30 J-6-2 (Invited)
Imaging of Spin Polarized Quantum Hall Current in GaAs Quantum Well by Scanning Kerr Microscope
K. Oto[1], T. Matsuda[1], Y. Gunji[1], D. Fukuoka[1], K. Muro[1], N. Kumada[2] and Y. Hirayama[3,4], [1]Chiba Univ., [2]NTT Basic Res. Labs., [3]Tohoku Univ. and [4]ERATO (Japan)

10:00 J-6-3
Inherently fast spin relaxation of exciton in photo-excited self-assembled quantum dots
Y. H. Liao[1], J. I. Climente[2] and S. J. Cheng[1], [1]National Chiao-Tung Univ. and [2]Universitat Jaume I, Castello (Taiwan)

10:15 J-6-4
Wavelength tunable single-photon source with a side gate
T. Nakaoka[1,2,3], Y. Tamura[1], T. Miyazawa[1], K. Watanabe[1], Y. Ota[1], S. Iwamoto[1] and Y. Arakawa[1], [1]Univ. of Tokyo, [2]PRESTO-JST and [3]Sophia Univ. (Japan)

10:30 J-6-5
Donor-location-dependent RTS Observed by Trapping and Detrapping of a Photoexcited Electron by a Single Donor
A. Udhiarto, D. Moraru, T. Mizuno and M. Tabe, Shizuoka Univ. (Japan)

12F 1203

12F 1204

12F 1207

12F 1208

N-6: Spintronics materials and devices (Area 12)
(9:00-10:45)
Chairs: S. Kuroda (Univ. of Tsukuba)
H. Saito (AIST)

9:00 N-6-1 (Invited)
Spin-torque induced magnetization switching and oscillation in half-metallic Co_2MnSi-based CPP-GMR devices
Y. Sakuraba, R. Okura, K. Izumi, T. Seki, S. Bosu, M. Mizuguchi, K. Saito and K. Takanashi, Tohoku Univ. (Japan)

9:30 N-6-2
Magnetoresistance Effect in Current-Perpendicular-to-Plane Magnetoresistive Devices using $Co_2Fe_xMn_{1-x}Si$ Heusler Alloy
M. Oogane, J. Sato, H. Naganuma and Y. Ando, Tohoku Univ. (Japan)

9:45 N-6-3
Fabrication of Fully Epitaxial Magnetic Tunnel Junctions with CoFe Electrodes and a MgO Barrier on Ge(001) Substrates via a MgO Interlayer
G. F. Li, T. Taira, H. X. Liu, K. Matsuda, T. Uemura and M. Yamamoto, Hokkaido Univ. (Japan)

10:00 N-6-4
Quasiparticle Tunneling Spectroscopy in Fe_4N/MgO/NbN Junctions
K. Sakuma[1], T. Hohjo[1], T. Miyawaki[1], K. Ueda[1], H. Asano[1], Y. Komasaki[2] and M. Tsunoda[2], [1]Nagoya Univ. and [2]Tohoku Univ. (Japan)

10:15 N-6-5 (Invited)
Ultrafast Magneto-Optics Study on Magnetic Semiconductor (Ga,Mn)As
X. H. Zhang, Y. G. Zhu, L. F. Han, H. Yue, L. Chen and J. H. Zhao, Chinese Academy of Sci. (China)

Coffee Break

Friday, September 30

5F Hall 1

AL-7: SiC&GaN Power Switching Devices (2) (Area 6&14)
(11:15-12:30)
Chairs: N. Ikeda (Advanced Power Device Res. Assoc.)
M. Kuzuhara (Univ. of Fukui)

11:15 AL-7-1
InAlN/AlN/GaN Schottky Source/Drain MIS-HEMT with High Breakdown Voltage
Q. Zhou[1], H. Chen[2], C. Zhou[2], Z. H. Feng[1], S. J. Cai[2] and K. J. Chen[1], [1]Hong Kong Univ. of Sci. and Tech. and [2]Hebei Semiconductor Res. Inst. (China)

11:30 AL-7-2
Selective Electrochemical Formation of Recessed-Oxide-Gate Structures for AlGaN/GaN HEMTs
N. Azumaishi[1], N. Harada[1] and T. Hashizume[1,2], [1]Hokkaido Univ. and [2]CREST-JST (Japan)

11:45 AL-7-3
AlGaN/GaN HFET grown on 6-inch diameter Si(111) substrates by MOCVD
S. M. Cho, E. J. Hwang, J. Park, K. C. Kim and T. Jang, LG Electronics Inst. of Tech. (Korea)

12:00 AL-7-4
AlGaN/GaN HEMTs on Silicon with Hybrid Schottky-Ohmic Drain for Improved DC Characteristics
Y. S. Lin, Y. W. Lian, H. C. Lu, Y. C. Huang and S. S. H. Hsu, National Tsing Hua Univ. (Taiwan)

5F Hall 2

KM-7: Graphene Application (Area 8&13)
(11:15-12:30)
Chairs: K. Maehashi (Osaka Univ.)
H. Kageshima (NTT Basic Res. Labs.)

11:15 KM-7-1 (Invited)
Epitaxial CVD Growth of Graphene and Influence of Domain Structure on Transport Property
H. Ago[1], C. M. Orofeo[1], Y. Ogawa[1], B. Hu[1], Y. Ito[1], K. Kawahara[1], M. Tsuji[1], K. Ikeda[1], S. Mizuno[1] and H. Hibino[2], [1]Kyushu Univ. and [2]NTT Basic Res. Labs. (Japan)

11:45 KM-7-2
Touch Pressure Sensor using Metal/PVDF-TrFE/Graphene Device
E. J. Paek, H. J. Hwang, S. K. Lee, C. G. Kang, C. H. Cho, Y. G. Lee, S. K. Lim and B. H. Lee, GIST (Korea)

12:00 KM-7-3
Valinomycin-Modified Graphene Field-Effect Transistors for Potassium Ion Sensors
Y. Sofue, Y. Ohno, K. Maehashi, K. Inoue and K. Matsumoto, Osaka Univ. (Japan)

12:15 KM-7-4
Effect of ionic liquid on transfer characteristic of graphene channel on PZT
J. Suzuki[1], S. Kataoka[1], T. Arie[1,2] and S. Akita[1,2], [1]Osaka prefecture Univ. and [2]CREST-JST (Japan)

10F 1002

B-7: Device physics and characterization of OTFT (2) (Area 10)
(11:15-12:30)
Chairs: E. Itoh (Shinshu Univ.)
T. Manaka (Tokyo Tech)

11:15 B-7-1
Upward and Downward Orientation of an Interface Dipole Monolayer on Pentacene Organic Field-Effect Transistors: A Comparison Study
O. Y. Wei[1], M. Weis[2], T. Manaka[1] and M. Iwamoto[1], [1]Tokyo Tech and [2]Slovak Academy of Sci (Japan)

11:30 B-7-2
Mobility Improvement in Top-Gate Benzothienobenzothiophene Organic Transistors Processed by Spin Coating
F. Mochizuki[1], T. Endo[1], T. Nagase[1], T. Kobayashi[1], K. Takimiya[2], M. Ikeda[3,4] and H. Naito[1], [1]Osaka Prefecture Univ., [2]Hiroshima Univ., [3]Nippon Kayaku Corp., Ltd. and [4]Kyushu Univ. (Japan)

11:45 B-7-3
TIPS-Pentacene Organic Field-Effect Transistors Utilizing Poly(*p*-silsesquioxane) Insulating Layers With Different Phenol Groups
Y. Nakanishi[1], H. Kajii[1], K. Tamura[2] and Y. Ohmori[1], [1]Osaka Univ. and [2]Tokyo Ohka Kogyo Corp. Ltd. (Japan)

12:00 B-7-4
Effects of Film Morphology on Ambipolar Transport of Solution-Processed Top-gate-Type Organic Field-Effect Transistors Utilizing Blended Fluorene Derivatives
H. Kajii, K. Koiwai and Y. Ohmori, Osaka Univ. (Japan)

10F 1003

11F 1101

D-7: ET-SOI and Nanowire Devices (Area 3)
(11:15-12:25)
Chairs: M. Hane (Renesas Electronics Corp.)
O.Weber (CEA-LETI/MINATEC)

11:15 D-7-1 (Invited)
Extremely Thin SOI (ETSOI) - a Planar CMOS Technology for System-on-chip Applications
K. Cheng[1], A. Khakifirooz[1], P. Kulkarni[1], S. Ponoth[1], B. Haran[1], A. Kumar[1], T. Adam[1], A. Reznicek[1], N. Loubet[2], H. He[1], J. Kuss[1], M. Wang[1], T. M. Levin[1], F. Monsieur[2], Q. Liu[2], R. Sreenivasan[1], J. Cai[1], A. Kimball[1], S. Mehta[1], S. Luning[3], Y. Zhu[1], Z. Zhu[1], T. Yamamoto[4], A. Bryant[1], C. H. Lin[1], S. Naczas[1], H. Jagannathan[1], L. F. Edge[1], S. Allegret-Maret[2], A. Dube[1], S. Kanakasabapathy[1], S. Schmitz[1], A. Inada[4], S. Seo[1], M. Raymond[3], Z. Zhang[1], A. Yagishita[5], J. Demarest[1], J. Li[1], M. Hopstaken[1], N. Berliner[1], A. Upham[1], R. Johnson[1], S. Holmes[1], T. Standaert[1], M. Smalley[1], N. Zamdmer[1], Z. Ren[1], T. Nagumo[4], T. Wu[1], H. Bu[1], V. Paruchuri[1], D. Sadana[1], V. Narayanan[1], W. Haensch[1], J. O'Neill[1], T. Hook[1], M. Khare[1], G. Shahidi[1] and B. Doris[1], [1]IBM, [2]STMicroelectronic, [3]GLOBALFOUNDRIES, [4]Renesas and [5]Toshiba (USA)

11:45 D-7-2
Carrier Transport Mechanisms in Schottky Barrier Source/Drain Nanowire FETs with Lateral Silicidation Process
T. Ishikawa, M. Saitoh, K. Ota, C. Tanaka and T. Numata, Toshiba Corp. (Japan)

12:05 D-7-3
Advantages of Silicon Nanowire MOSFETs over Planar Ones Investigated from the Viewpoints of Static and Noise Properties
W. Feng[1,2], R. Hettiarachchi[1,2], S. Sato[3], K. Kakushima[3], M. Niwa[1,2], H. Iwai[3], K. Yamada[1,2] and K. Ohmori[1,2], [1]Univ. of Tsukuba, [2]CREST-JST and [3]Tokyo Tech (Japan)

11F 1102

E-7: Ge Process Technology (2) (Area 1)
(10:45-12:05)
Chairs: T. Aoyama (Toshiba Corp.)
T. Nabatame (NIMS)

10:45 E-7-1
Strained Ge Layers on SiGe(Sn) Buffer Layers Formed by Solid-phase Mixing Method
T. Yamaha[1], K. Mochizuki[1], Y. Shimura[1,2], O. Nakatsuka[1] and S. Zaima[1], [1]Nagoya Univ. and [2]JSPS (Japan)

11:05 E-7-2
Evaluation of Anisotropic Strain Relaxation in SSOI Nanostructure by Oil-Immersion Raman Spectroscopy
D. Kosemura[1], M. Tomita[1], K. Usuda[2] and A. Ogura[1], [1]Meiji Univ. and [2]AIST (Japan)

11:25 E-7-3
Channel strain measurements in 32nm-node CMOSFETs
M. Takei[1], H. Hashiguchi[1], T. Yamaguchi[1], D. Kosemura[1], K. Nagata[1,2] and A. Ogura[1], [1]Meiji Univ. and [2]JSPS (Japan)

11:45 E-7-4
Characterization of strain and crystallinity in patterned embedded Silicon Germanium structures
S. Mochizuki[1], A. Madan[2], A. Pofelski[3], A. G. Domenicucci[2], P. L. Flaitz[2], J. Li[2], Y. Y. Wang[2], T. Pinto[2], C. W. Lai[4], J. R. Holt[2], E. C. T. Harley[2], M. W. Stoker[2], A. Reznicek[2], D. Schepis[2] and V. Paruchuri[2], [1]Renesas Electronics, [2]IBM, [3]STMicroelectronics and [4]GLOBALFOUNDRIES Singapore (USA)

11F 1103

F-7: ReRAM (2) (Area 4)
(11:15-12:40)
Chairs: M. J. Tsai (ITRI)
K. Ishihara (Sharp Corp.)

11:15 F-7-1 (Invited)
Current Status and Future Challenges of Resistive Switching Memories
W. C. Chien, F. M. Lee, Y. Y. Lin, Y. C. Chen, M. H. Lee, H. L. Lung, K. Y. Hsieh and C. Y. Lu, Macronix International Co., Ltd. (Taiwan)

11:45 F-7-2
Investigation of Forming and Its Controllability in Novel HfO_2-Based 1T1R 40nm-Crossbar RRAM Cells
B. Govoreanu[1], S. Kubicek[1], G. Kar[1], Y. Y. Chen[1,2], V. Paraschiv[1], M. Rakowski[1,2], R. Degraeve[1], L. Goux[1], S. Clima[1], N. Jossart[1], C. Adelmann[1], O. Richard[1], T. Raes[1], D. Vangoidsenhoven[1], T. Vandeweyer[1], H. Tielens[1], K. Kellens[1], K. Devriendt[1], N. Heylen[1], S. Brus[1], B. Verbrugge[1], L. Pantisano[1], H. Bender[1], G. Pourtois[1], J.A. Kittl[1], D.J. Wouters[1,2], L. Altimime[1] and M. Jurczak[1], [1]Imec and [2]Katholieke Univ. Leuven (Belgium)

12:05 F-7-3
CMOS Compatible Hf-based RRAM with Ultra-low Switching Currents/Power
*F. Zhang[1], X. Li[2], B. Gao[1], B. Chen[1], P. Huang[1], Y. Fu[1], Y. Chen[1], L. Liu[1], J. Kang[1], N. Singh[2], G. Q. Lo[2] and D. L. Kwong[2], [1]Peking Univ. and [2]A*STAR (China)*

12:25 F-7-4 (Late News)
Alloy and Strain Induced Multivalency in Magneli Phase Ti_nO_{2n-3} and TiO_2-HfO_2 Alloys: Singlet Negative Ion States and Non-Linear Metallic Conduction
G. Lucovsky and J. W. Kim, NC State Univ. (USA)

Friday, September 30

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
G-7: RF Circuits (2) (Area 5) (11:15-12:35) Chairs: J. C. Guo (National Chiao Tung Univ.) M. Ikebe (Hokkaido Univ.)	**H-7: Nano fabrication and Application (Area 11)** (11:15-12:15) Chairs: K. Ajito (NTT Corp.) H. Nishio (OMRON Corp.)	**CI-7: Optical Interconnect (2) (Area 2&7)** (11:15-12:25) Chairs: S. Ogawa (AIST) H. Ishii (Toyohashi Univ. of Tech.)	**J-7: Quantum Transport in Nanostructures (Area 9)** (11:15-12:30) Chairs: T. Machida (Univ. of Tokyo) T. Nakaoka (Sophia Univ.)				**N-7: Spin transport in semiconductors (Area 12)** (11:15-12:30) Chairs: M. Yamamoto (Hokkaido Univ.) Y. Ohno (Tohoku Univ.)
11:15 G-7-1 **A 60-GHz Band Low Power Differential CMOS LNA with Current-Reuse Topology** *Y. Tsubouchi, S. Kawai, T. Mitomo, S. Saigusa and O. Watanabe, Toshiba Corp. (Japan)*	**11:15 H-7-1** **Electrostatic Control Mechanism of Lipid Bilayer Self-Spreading Using Nanogap as Molecule Gate** *Y. Kashimura, K. Furukawa and K. Torimitsu, NTT Basic Res. Labs. (Japan)*	**11:15 CI-7-1 (Invited)** **Optical Interconnection based on Silicon photonics** *S. Itabashi, K. Yamada, R. Kou, T. Watanabe, H. Shinojima, H. Nishi and T. Tsuchizawa, NTT Microsystem Integration Labs. (Japan)*					**11:15 N-7-1 (Invited)** **Spin Injection and Transport in a Si Channel at Room Temperature** *T. Suzuki[1], T. Sasaki[2], T. Oikawa[2], M. Shiraishi[3], Y. Suzuki[3] and K. Noguchi[2], [1]AIT, [2]TDK Corp. and [3]Osaka Univ. (Japan)*
11:35 G-7-2 **Low Voltage and Low power UWB CMOS LNA using Forward Body Biasing Technique** *J. R Huang and J. C. Guo, National Chiao Tung Univ. (Taiwan)*	**11:30 H-7-2** **Fabrication of a micro-lens array for Reflective Electron Beam Lithography** *B. Vereecke[1], L. Haspeslagh[1], F. Lazzarino[1], R. A. Miller[1], K. Kellens[1], H. Dekkers[1], R. Freed[2] and L. Grella[2], [1]Imec and [2]KLA-Tencor Corp. (Belgium)*	**11:45 CI-7-2** **High Efficient Unidirectional Optical Coupler for Through Silicon Photonic Via in Optoelectronic 3D-LSI** *A. Noriki, K. W. Lee, J. Bea, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)*	**11:30 J-7-2** **Coulomb diamonds and Two-electron Spin Blockade in Cotunneling Regime of Serial Vertical Triple Quantum Dot Device** *S. Amaha[1,2], W. Izumida[3], T. Hatano[2, 4], S. Teraoka[2, 5], K. Ono[1, 2], K. Kono[1], S. Taucha[2, 5], J. Gupta[6] and D. G. Austing[6], [1]RIKEN, [2]ICORP-JST, [3]Tohoku Univ., [4]ERATO-JST, [5]Univ. of Tokyo and [6]NRC-Canada (Japan)*				**11:45 N-7-2** **Electrical Creation of Spin Accumulation in *p*-type Ge** *H. Saito[1], S. Watanabe[1,2], Y. Mineno[1,3], S. Sharma[1], R. Jansen[1], S. Yuasa[1] and K. Ando[1], [1]AIST and [2]Univ. of Tsukuba (Japan)*
11:55 G-7-3 **An Inverter-based Wideband Low Noise Amplifier in 40nm CMOS Process** *D. N. Saimi Dharmiza, M. Oturu, S. Tanoi, H. Ito, N. Ishihara and K. Masu, Tokyo Tech (Japan)*	**11:45 H-7-3** **Fabricating a 2D Array of Φ6-nm, High Density (1.2×10^{12} cm^{-2}), and Periodic Silicon-Nanodisk Structures and Its Optical Characteristics for Solar Cells** *M. F. Budiman[1,4], M. Igarashi[1,4], K. M. Itoh[2,4], I. Yamashita[3,4], W. Hu[1,4] and S. Samukawa[1,4], [1]Tohoku Univ., [2]Keio Univ., [3]NAIST and [4]CREST-JST (Japan)*	**12:05 CI-7-3** **Investigation of grating coupler type optical I/O interface at the 1.55 μm wavelength range** *T. Osaka, T. Kita and H. Yamada, Tohoku Univ. (Japan)*	**11:45 J-7-3** **Electrostatic tuning of plasmonic cavities for edge magnetoplasmons** *M. Hashisaka[1], N. Kumada[2], H. Kamata[1,2], K. Washio[1], K. Muraki[2] and T. Fujisawa[1], [1]Tokyo Tech and [2]NTT Basic Res. Labs. (Japan)*				**12:00 N-7-3** **Radius dependence of Aharonov-Casher spin interference in InGaAs ring arrays** *F. Nagasawa[1], J. Takagi[1], Y. Kunihashi[1], M. Kohda[1,2] and J. Nitta[1], [1]Tohoku Univ. and [2]PRESTO-JST (Japan)*
12:15 G-7-4 **A High Efficiency Linear CMOS Power Amplifier for 5.8 GHz Dedicated Short Range Wireless Communication Systems** *Y. Suh[1], S. He[1], Q. Liu[1], K. Horie[2] and T. Yoshimasu[1], [1]Waseda Univ. and [2]Toshiba Corp. (Japan)*			**12:00 J-7-4** **Effect of Free Carriers on Dopant-induced Surface Potential in SOI-FETs** *M. Anwar[1], R. Nowak[1,2], D. Moraru[1], R. Jablonski[2], T. Mizuno[1] and M. Tabe[1], [1]Shizuoka Univ. and [2]Warsaw Univ. of Tech. (Japan)*				**12:15 N-7-4** **Effect of MgO Barrier Insertion on Spin-dependent Transport Properties of CoFe/n-GaAs** *T. Akiho, T. Uemura, M. Harada, K. Matsuda and M. Yamamoto, Hokkaido Univ. (Japan)*

Friday, September 30

5F Hall 1

AL-7: SiC&GaN Power Switching Devices (2) (Area 6&14)

12:15 AL-7-5
Step-stress Reliability Studies on AlGaN/GaN HEMTs on Silicon with Buffer Thickness Dependence
A. F. Wilson, A. Wakejima, S. L. Selvaraj and T. Egawa, Nagoya Inst. of Tech. (Japan)

A-8: Processing and Characterization Technologies (Area 6)
(14:00-15:30)
Chairs: Y. Miyamoto (Tokyo Tech)
Y. Ohno (Univ. of Tokushima)

14:00 A-8-1
High Integrity SiO_2 Gate Insulator Formed by Microwave-Excited PECVD for AlGaN/GaN Hybrid MOS-HFET on Si Substrate
H. Kamnbayashi[1,3], T. Nomura[1], S. Kato[1], H. Ueda[2], A. Teramoto[3], S. Sugawa[3] and T. Ohmi[3], [1]Advanced Power Device Res. Association, [2]Tokyo Electron Tech. Development Inst. Inc. and [3]Tohoku Univ. (Japan)

14:15 A-8-2
Low-Leakage Current n-GaN/AlGaN/GaN HEMT with TaO_xN_y Gate Dielectric
T. Sato, J. Okayasu, T. Yamanouchi, T. Yashiro, J. Suzuki and M. Takikawa, Advantest Labs. Ltd. (Japan)

14:30 A-8-3
Impacts of Dry Etching of GaN and AlGaN Surfaces on Interface Properties of GaN-based MOS Structures
S. Kim[1], Y. Hori[1], N. Azumaishi[1] and T. Hashizume[1, 2], [1]Hokkaido Univ. and [2]CREST-JST (Japan)

14:45 A-8-4
Damage-free GaN Etching by Chlorine Neutral Beam
Y. Tamura[1,3], X. Y. Wang[1,3], C. H. Huang[1,3], T. Kubota[1], J. Ohta[2], H. Fujioka[2,3] and S. Samukawa[1,3], [1]Tohoku Univ., [2]Univ. of Tokyo and [3]CREST-JST (Japan)

5F Hall 2

KM-7: Graphene Application (Area 8&13)

10F 1002

B-7: Device physics and characterization of OTFT (2) (Area 10)

12:15 B-7-5
Effects of Silver Nanoparticles Organic Envelope on Pentacene Organic Field-effect Transistors
K. Lee, M. Weis, X. Chen, D. Taguchi, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)

B-8: OTFT application (1) (Area 10)
(14:00-15:45)
Chairs: M. Sakai (Chiba Univ.)
M. Yoshida (AIST)

14:00 B-8-1 (Invited)
Organic Thin-Film Transistor-Based Non-Volatile Memory Devices
J. S. Lee, Kookmin Univ. (Korea)

14:45 B-8-3
High performance of pentacene field effect transistors using graphene electrodes and substrate treatments
S. Lee[1], G. Jo[1], S. J. Kang[1], G. Wang[1], M. Choi[1], W. Park[1], J. Yoon[1], T. Kwon[1], D. Y. Kim[1], Y. H. Kahng[1] and T. Lee[1,2], [1]Gwangju Inst. of Sci. and Tech. and [2]Seoul National Univ. (Korea)

15:00 B-8-4
Variation of Active Layer Thickness of Polymer Thin Film Transistors and its Effect on Digital Circuits Performance
L. Reséndiz[1], M. Estrada[2], A. Cerdeira[2] and V. Cabrera[1], [1]Inst. UPIITA - IPN and [2]Res. CINVESTAV (Mexico)

10F 1003

12:30-14:00 Lunch

C-8: 3D Interconnect (2) and Characterization (2) (Area 2)
(14:00-15:50)
Chairs: P. Leduc (CEA-LETI/MINATEC)
T. Hasegawa (Sony Corp.)

14:00 C-8-1 (Invited)
Low temperature curable nano-inks for printed wiring and transparent films
K. Suganuma, M. Nogi, T. Tokuno and J. Jiu, Osaka Univ. (Japan)

14:30 C-8-2
Stress from Tungsten-Filled TSVs Measured by Raman Spectroscopy on Cross-Sectional Samples
J. Gambino[1], D. Vanslette[1], B. Webb[1], C. Luce[1], G. Chrisman[1], T. Ueda[2], T. Ishigaki[2], K. Kang[2] and W.S. Yoo[2], [1]IBM and [2]WaferMasters, Inc. (USA)

14:50 C-8-3
Evaluation of Thermo-Mechanical Stress Induced by W-TSVs in 3D-LSI with W/Cu Hybrid TSVs
H. Hashiguchi[1], M.Murugesan[1], J. C. Bea[1], K. W. Lee[1], T. Fukushima[1], H. Kobayashi[2], T. Tanaka[1] and M. Koyanagi[1], [1]Tohoku Univ. and [2]Association of Super-Advanced Electronics Tech. (Japan)

15:10 C-8-4
Size and Deformation Mode Dependencies on the Strength of Dry-Etched Single Crystal Silicon Micro-Beams
T. Namazu[1,2], H. Yamagiwa[1], T. Fujii[1], M. Saito[3], K. Yamada[3] and T. Miyatake[3], [1]Univ. of Hyogo, [2]PRESTO-JST and [3]Panasonic Electric Works Co., Ltd. (Japan)

11F 1101

D-7: ET-SOI and Nanowire Devices (Area 3)

D-8: Device Reliability (Area 3)
(14:00-15:30)
Chairs: D. Hisamoto (Hitachi, Ltd.)
B. Doris (IBM)

14:00 D-8-1 (Invited)
A Consistent Modeling Framework to Explain Negative Bias Temperature Instability (NBTI) DC Stress, Recovery and AC Experiments
S. Mahapatra[1], A. E. Islam[2], S. Deora[1], V. D. Maheta[1] and M. A. Alam[2], [1]IIT Bombay and [2]Purdue Univ. (India)

14:30 D-8-2
HCI and NBTI Induced statistical Variability in CMOS Transistors
A. Cathignol[1], F. Cacho[2], X. Federspiel[2] and D. Roy[2], [1]IBM and [2]STMicroelectronics (France)

14:50 D-8-3
Compact Reaction-Diffusion Model for Accurate NBTI Prediction
C. Ma[1,3], M. Miyake[1], H. J. Mattausch[1], K. Matsuzawa[2], T. Iizuka[2], T. Hozhida[2], A. Kinoshita[2], T. Arakawa[2], J. He[3] and M. Miura-Mattausch[1], [1]Hiroshima Univ., [2]STARC and [3]Peking Univ. (Japan)

15:10 D-8-4
Enhanced Degradation by NBT stress in Si Nanowire Transistor
K. Ota[1], M. Saitoh[1], C. Tanaka[1], Y. Nakabayashi[1], K. Uchida[2] and T. Numata[1], [1]Toshiba Corp. and [2]Tokyo Tech (Japan)

11F 1102

E-7: Ge Process Technology (2) (Area 1)

E-8: III-V CMOS Technology (Area 1)
(13:35-15:55)
Chairs: E. Nishimura (Tokyo Electron Ltd.)
T. Nakayama (Chiba Univ.)

13:35 E-8-1 (Invited)
Challenges for High-k/III-V CMOS: Interfacial Chemistry, Defects, and Fermi Level Pinning
R. M. Wallace, Univ. of Texas (USA)

14:05 E-8-2
Guiding Principles for Bonding and Passivation at III-V － oxide Interfaces
J. Robertson and L. Lin, Cambridge Univ. (UK)

14:25 E-8-3
Effect of sulfur treatment on HfO_2/InGaAs MOS interfaces properties
R. Suzuki[1], S. Lee[1], S. H. Kim[1], T. Hoshii[1], M. Yokoyama[1], N. Taoka[1], T. Yasuda[2], W. Jevasuwan[2], T. Maeda[2], O. Ichikawa[3], N. Fukuhara[3], M. Hata[3], M. Takenaka[1] and S. Takagi[1], [1]Univ. of Tokyo, [2]AIST and [3]Sumitomo Chemical Co., Ltd. (Japan)

14:55 E-8-4
Effects of Nitrided-InGaAs Interfacial Layers formed by ECR nitrogen plasma on Al_2O_3/InGaAs MOS Properties
T. Hoshii[1], S. Lee[1], R. Suzuki[1], N. Taoka[1], M. Yokoyama[1], H. Yamada[2], W. Jevasuwan[3], M. Hata[2], T. Yasuda[3], M. Takenaka[1] and S. Takagi[1], [1]Univ. of Tokyo, [2]Sumitomo Chemical Co., Ltd. and [3]AIST (Japan)

11F 1103

F-7: ReRAM (2) (Area 4)

F-8: ReRAM (3) (Area 4)
(14:00-15:40)
Chairs: K. Ishihara (Sharp Corp.)
M. Moniwa (Renesas Electronics Corp.)

14:00 F-8-1
50nm HfO_2 ReRAM with 50-Times Endurance Enhancement by Set/Reset *Turnback* Pulse & Verify Scheme
K. Higuchi, K. Miyaji, K. Johguchi and K. Takeuchi, Univ. of Tokyo (Japan)

14:20 F-8-2
Hetero-device complementary resistive switches with high switch speed and reliability for cross point array applications
D. Lee, J. Park, S. Jung, G. Choi, J. M. Lee, M. Siddik, J. Shin, S. Kim, J. Woo and H. Hwang, Gwangju Inst. of Sci. and Tech. (Korea)

14:40 F-8-3
Flexible One Diode-One Resistor Cross-bar Resistive-Switching Memory
C. W. Hsu[1], J. J. Huang[1], Y. M. Tseng[1], T. H. Hou[1], W. H. Chang[2], W. Y. Jang[2] and C. H. Lin[2], [1]National Chiao Tung Univ. and [2]Winbond Electronics Corp. (Taiwan)

15:00 F-8-4
Formation free low power resistive switching memory using IrO_x/AlO_x/W cross-point with excellent uniformity and multi level operation
W. Banerjee, S. Z. Rahaman and S. Maikap, Chang Gung Univ. (Taiwan)

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11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
G-7: RF Circuits (2) (Area 5)	**H-7: Nano fabrication and Application (Area 11)**	**CI-7: Optical Interconnect (2) (Area 2&7)**	**J-7: Quantum Transport in Nanostructures (Area 9)**				**N-7: Spin transport in semiconductors (Area 12)**
			12:15 J-7-5 **Nanoparticle Single-Electron Transistor with Metal Bridged Top-Gate Electrodes** *Y. Azuma[1,2], S. Suzuki[1,2], K. Maeda[1,2], N. Okabayashi[1,2], D. Tanaka[2,3], T. Teranishi[2,3], M. R. Buitelaar[4], C. G. Smith[4] and Y. Majima[1,2,5], [1]Tokyo Tech, [2]CREST-JST, [3]Tsukuba Univ., [4]Univ. of Cambridge and [5]Sunchon National Univ. (Japan)*				

12:30-14:00 Lunch

		I-8: SiGe-Based Optical Devices (Area 7) (14:00-15:30) Chairs: S. Saito (Hitachi Ltd.) N. Iizuka (Toshiba Corp.)	**J-8: Qubit and Novel Functional Devices (Area 9)** (14:00-15:45) Chairs: K. Ono (RIKEN) T. Tanamoto (Toshiba Corp.)	**K-8: Graphene Property (Area 13)** (14:00-15:45) Chairs: J. H. Ahn (Sungkyunkwan Univ.) S. Sato (AIST)	**L-8: Power Devices & ICs (Area 14)** (14:00-15:45) Chairs: M. Ishiko (Toyota Central R&D Labs., Inc) N. Ikeda (Advanced Power Device Res. Assoc.)	**M-8: Growth techniques of Si and Ge (Area 8)** (14:00-15:45) Chairs: H. Hibino (NTT Basic Res. Labs.) K. Hara (Shizuoka Univ.)	**N-8: Circuit application of spintronics devices (Area 12)** (14:00-15:30) Chairs: K. Ito (Hitachi, Ltd.) M. Oogane (Tohoku Univ.)
		14:00 I-8-1 **Electroluminescence from One-dimensionally Self-Aligned Si-based Quantum Dots with High Areal Dot Density** *K. Makihara[1], H. Deki[2], M. Ikeda[3] and S. Miyazaki[1], [1]Nagoya Univ., [2]Hiroshima Kokusai Gakuin Univ. and [3]Hiroshima Univ. (Japan)*	**14:00 J-8-1 (Invited)** **Atomic physics and quantum optics using circuits behaving as tunable artificial atoms** *F. Nori[1,2], [1]RIKEN and [2]Univ. of Michigan (Japan)*	**14:00 K-8-1 (Invited)** **Trends and Future of Ultrafast Transistors and Terahertz Light Amplification by Stimulated Emission of Radiation Using Graphene** *T. Otsuji[1,2], [1]Tohoku Univ. and [2]CREST-JST (Japan)*	**14:00 L-8-1 (Invited)** **Key Power Device Technologies Catering to Sustainable Growth of Power Electronics** *G. Majumdar, Mitsubishi Electric Corp. (Japan)*	**14:00 M-8-1** **Impact on TFT Characteristics of Rapid Crystallization of Si using Nickel-Metal Induced Lateral Crystallization** *S. Nagata, G. Nakagawa and T. Asano, Kyushu Univ. (Japan)*	**14:00 N-8-1** **Anisotropic phase coherent length affected by coexistence of a spin orbit interaction and an in-plane magnetic field in InGaAs narrow wire structures** *S. Nonaka[1], Y. Kunihashi[1], M. Kohda[1,2] and J. Nitta[1], [1]Tohoku Univ. and [2]PRESTO-JST (Japan)*
		14:15 I-8-2 **Demonstration of Silicon Nanocavity LED with Enhanced Luminescence** *S. Nakayama, S. Iwamoto, S. Kako, S. Ishida and Y. Arakawa, Univ. of Tokyo (Japan)*	**14:30 J-8-2** **Steady-state solution for dark states using a three-level system in coupled quantum dots** *T. Tanamoto[1], K. Ono[2] and F. Nori[2,3], [1]Toshiba Corp., [2]RIKEN and [3]Univ. of Michigan (Japan)*	**14:30 K-8-2** **Effects of Randomly Distributed Local Dirac Points in Graphene Channel on Its FET Transfer Characteristics** *R. Ifuku, K. Nagashio, T. Nishimura and A. Toriumi, Univ. of Tokyo (Japan)*	**14:30 L-8-2** **Extraction enhanced lateral IGBT (E^2 LIGBT) : A super high speed LIGBT superior to LDMOS** *Y. Ashida[1], S. Takahashi[1], S. Shiraki[1], N. Tokura[1] and A. Nakagawa[2], [1]DENSO Corp. and [2]Nakagawa Consulting Office (Japan)*	**14:15 M-8-2** **High Speed Lateral Crystallization of Amorphous Silicon Films on Glass Substrates by Micro-Thermal-Plasma-Jet Irradiation and Its Application to Thin Film Transistor Fabrication** *Y. Fujita, S. Hayashi, H. Murakami and S. Higashi, Hiroshima Univ. (Japan)*	**14:15 N-8-2** **A Compact Nonvolatile Logic Element Using an MTJ/MOS-Hybrid Structure** *D. Suzuki, M. Natsui, T. Endoh, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)*
		14:30 I-8-3 **Si/SiO_2 Bilayer Beam Structure for Photoelastic Control of Si Photonic Devices** *M. Hirase, Y. Ishikawa and K. Wada, Univ. of Tokyo (Japan)*	**14:45 J-8-3** **Ultra-Low-Power Superconducting Logic Devices using Adiabatic Quantum Flux Parametron** *N. Yoshikawa, D. Ozawa and Y. Yamanashi, Yokohama National Univ. (Japan)*	**14:45 K-8-3** **Graphene Growth on Sidewall of Catalyst by CVD and Its Application to Graphene Transistors** *H. An[1], W. G. Lee[2] and J. W. Jung[1], [1]Sejong Univ. and [2]National Nano Fab Center (Korea)*	**14:45 L-8-3** **High Voltage and high reliability SOI power IC technologies and their application to 750V 4.5A micro-inverter IC** *S. Shiraki, S. Takahashi, A. Yamada, M. Yamamoto, K. Senda, Y. Ashida, A. Hiruma and N. Tokura, DENSO Corp. (Japan)*	**14:30 M-8-3** **Investigation of Ni Metal Induced Lateral Crystallization with a-Si Film Thickness at Very Thin Extent** *G. Nakagawa, T. Nakamae and T. Asano, Kyushu Univ. (Japan)*	**14:30 N-8-3** **Physics-based SPICE Model of Spin Torque Oscillators** *H. Lim, S. Ahn, S. Lee and H. Shin, Ewha Womans Univ. (Korea)*
		14:45 I-8-4 **Light Detection and Emission in Germanium-On-Insulator Diodes** *K. Tani[1,2,3], S. Saito[1,2,3], Y. Lee[3], K. Oda[1,2,3], T. Mine[3], T. Sugawara[1,2,3] and T. Ido[1,2,3], [1]PECST, [2]PETRA and [3]Hitachi, Ltd. (Japan)*	**15:00 J-8-4** **Atto-Joule Operation of High-Speed Shift Register Based on Ultra Low-Power Rapid Single Flux Quantum Circuit Technology** *A. Fujimaki[1], M. Tanaka[1,2], A. Kitayama[1], T. Kouketsu[1] and M. Ito[1], [1]Nagoya Univ. and [2]UC, Berkeley (Japan)*	**15:00 K-8-4** **Electrical Conductance in Graphene Contacting with Metal** *T. Moriyama, K. Nagashio, T. Nishimura and A. Toriumi, Univ. of Tokyo (Japan)*	**15:00 L-8-4** **A Novel FEM-LDMOS of Improved Off-state Breakdown Voltage Without Additional Mask** *H. B. Chen[1], C. J. Chang[2], J. J. Wu[1], W. C. Chen[3], C. C. Tsai[2] and C. Y. Chang[1], [1]National Chiao Tung Univ., [2]Himax Technologies and [3]Vanguard International Semiconductor Corp. (Taiwan)*	**14:45 M-8-4** **Orientation Control of Al-Induced Crystallized Silicon by Diffusion Barrier Layers** *A. Okada[1], K. Toko[1], K. Hara[2], N. Usami[2,3] and T. Suemasu[1,3], [1]Univ. of Tsukuba, [2]Tohoku Univ. and [3]CREST-JST (Japan)*	**14:45 N-8-4** **Time-Resolved Switching Characteristic in Magnetic Tunnel Junction with Spin Transfer Torque Write Scheme** *F. Iga, Y. Yoshida, S. Ikeda, T. Hanyu H. Ohno and T. Endoh, Tohoku Univ. (Japan)*

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5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
A-8: Processing and Characterization Technologies (Area 6)		**B-8: OTFT application (1) (Area 10)**	**C-8: 3D Interconnect (2) and Characterization (2) (Area 2)**	**D-8: Device Reliability (Area 3)**	**E-8: III-V CMOS Technology (Area 1)**	**F-8: ReRAM (3) (Area 4)**
15:00 A-8-5 **Germanium/Ni-InGaAs Solid-State Reaction for Contact Resistance Reduction on n^+ $In_{0.53}Ga_{0.47}As$** *H. X. Guo, E. Y. J. Kong, X. Zhang and Y. C. Yeo, National Univ. of Singapore (Singapore)*		**15:15 B-8-5** **Control of switching voltage of low voltage organic complementary inverter using floating gate structure** *T. Yokota[1], T. Sekitani[1], T. Nakagawa[1], Y. Noguchi[1], K. Takeuchi[1], U. Zschieschang[2], H. Klauk[2] and T. Someya[1], [1]Univ. of Tokyo, and [2]Max Planck Inst. for Solid State Res. (Japan)*	**15:30 C-8-5** **Local Interface Strength Evaluation for LSI Interconnect with Micron Resolution** *N. Shishido[1,5], C. Chen[1], H. Sato[1,5], S. Kamiya[1,5], M. Nishida[1,5], M. Omiya[2,5], T. Nokuo[3,5], T. Nagasawa[3,5], T. Suzuki[4] and T. Nakamura[4], [1]Nagoya Inst. of Tech., [2]Keio Univ., [3]JEOL Ltd., [4]Fujitsu Labs. Ltd. and [5]CREST-JST (Japan)*		**15:15 E-8-5** **Controlling anion composition at MIS interfaces on III-V Channels by Plasma Processing** *W. Jevasuwan[1], Y. Urabe[1], T. Maeda[1], N. Miyata[1], T. Yasuda[1], A. Ohtake[2], H. Yamada[3], M. Hata[3], S. Lee[4], T. Hoshii[4], M. Takenaka[4] and S. Takagi[4], [1]AIST, [2]NIMS, [3]Sumitomo Chemical. Co., Ltd. and [4]Univ. of Tokyo (Japan)*	**15:20 F-8-5** **Highly Uniform and Reliable Switching Properties in NbO_x Based RRAM Devices** *S. M. Sadaf, X. Liu, S. H. Choudhury, J. Shin, J. Woo, M. Siddik and H. Hwang, Gwangju Inst. of Sci. and Tech. (Korea)*
15:15 A-8-6 **Fabrication and analysis of AlN/GaAs(001) metal-insulator-semiconductor structure** *M. Kudo, H. A. Shih, M. Akabori and T. Suzuki, JAIST (Japan)*		**15:30 B-8-6** **3V-Operation Organic Transistors on Shape-Memory Film with Polyimide Planarization Layer** *Y. Kato[1], T. Sekitani[1], T. Yokota[1], K. Kuribara[1], U. Zschieschang[2], H. Klauk[2], T. Yamamoto[3], K. Takimiya[3], M. Ikeda[4], H. Kuwabara[4] and T. Someya[1], [1]Univ. of Tokyo, [2]Max Planck Inst. for Solid State Res., [3]Hiroshima Univ. and [4]Nippon Kayaku Corp. Ltd. (Japan)*			**15:35 E-8-6** **Formation of Ultra-thin and Uniform Ni-InGaAs Alloyed Contact for Scaled Metal S/D InGaAs MOSFETs** *T. Irisawa, M. Oda and T. Tezuka, AIST (Japan)*	

Coffee Break

		B-9: OTFT application (2) (Area 10) (16:10-17:25) Chairs: T. Manaka (Tokyo Tech) K. Kato (Niigata Univ.)	**C-9: Characterization (3) (Area 2)** (16:10-17:30) Chairs: J. Gambino (IBM Microelectronics) Y. Otsuka (Toray Research Center Inc.)		**E-9: Advanced Si Technology (Area 1)** (16:10-17:25) Chairs: J. Yugami (Renesas Electronics Corp.) T. Nakayama (Chiba Univ.)	**F-9: ReRAM (4) (Area 4)** (16:10-17:10) Chairs: Y. C. Chen (Macronix International Co., Ltd.) T. Endoh (Tohoku Univ.)
		16:10 B-9-1 **Bending test of organic TFTs with a soluble polycrystalline semiconductor** *T. Tokuhara, T. Sekitani, T. Yokota and T. Someya, Univ. of Tokyo (Japan)*	**16:10 C-9-1** **In Situ Analysis of Plasma-Induced Modification on Porous SiOCH Films** *H. Yamamoto, K. Asano, K. Ishikawa, K. Takeda, H. Kondo, M. Sekine and M. Hori, Nagoya Univ. (Japan)*		**16:10 E-9-1** **Silicon-On-Insulator Fabrication Using Si/HfO_2/Si Epitaxial Structure** *S. Migita and H. Ota, AIST (Japan)*	**16:10 F-9-1** **Record resistance ratio and bipolar/unipolar resistive switching scenario using novel Cu/GeO_x/W memory device** *S. Z. Rahaman[1], S. Maikap[1], S. K. Ray[1,2], H. Y. Lee[3], W. S. Chen[3], F. T. Chen[3], M. J. Kao[3] and M. J. Tsai[3], [1]Chang Gung Univ., [2]Indian Inst. of Tech. and [3]ITRI (Taiwan)*
		16:25 B-9-2 **Solution-processed C_{60} field-effect transistors with high mobility** *W. Kang[1], M. Kitamura[1,2], M. Kamura[1,3], S. Aomori[1,3] and Y. Arakawa[1], [1]Univ. of Tokyo, [2]Kobe Univ. and [3]Sharp Corp. (Japan)*	**16:30 C-9-2** **Potential Characterization of Interconnect Corrosion by Kelvin Probe Force Microscopy** *M. Kodera, Y. Yoshimizu and K. Uchida, Toshiba Corp. (Japan)*		**16:30 E-9-2** **Enabling epitaxy on ultrathin implanted SOI** *L. Grenouillet[1], N. Posseme[1], S. Ponoth[2], N. Loubet[3], V. Destefanis[1], Y. Le Tiec[1], S. Mehta[2], A. Kumar[2], Q. Liu[3], B. Haran[2], K. Cheng[2], N. Berliner[2], J. Fullam[2], J. Kuss[2], G. Shahidi[2], O. Faynot[1], B. Doris[2]and M. Vinet[1], [1]CEA-LETI, [2]IBM and [3]ST Microelectronics (USA)*	**16:30 F-9-2** **Effects of Ti interfacial layer on resistive switching memory performance using Cu filament in high-κ Ta_2O_5solid-electrolyte** *A. K. Sahoo[1], S. Z. Rahaman[1], S. Maikap[1], H. Y. Lee[2], W. S. Chen[2], F. T. Chen[2], M. J. Kao[2] and M. J. Tsai[2], [1]Chang Gung Univ. and [2]ITRI (Taiwan)*

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11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
		I-8: SiGe-Based Optical Devices (Area 7)	**J-8: Qubit and Novel Functional Devices (Area 9)**	**K-8: Graphene Property (Area 13)**	**L-8: Power Devices & ICs (Area 14)**	**M-8: Growth techniques of Si and Ge (Area 8)**	**N-8: Circuit application of spintronics devices (Area 12)**
		15:00 I-8-5 **Improving Optical Properties of Ge Layers Fabricated by Epitaxial Growth Combined with Ge Condensation** *K. Oda[1, 2, 3], K. Tani[1, 2, 3], S. Saito[1, 2, 3], T. Okumura[3] and T. Ido[1, 2, 3], [1]PETRA, [2]PECST and [3]Hitachi Ltd. (Japan)*	**15:15 J-8-5** **Induced Dielectric Polarization and Piezoelectric Effects on Valence Band alignment in Multi-Quantum Well Composed of Wurtzite Semiconductors** *S. Emura, M. Morifuji, M. Kondow and H. Asahi, Osaka Univ. (Japan)*	**15:15 K-8-5** **Electronic Structure Modulation of Graphene Adsorbed by Metal Pillars** *Y. Takagi[1,2] and S. Okada[1,2], [1]Univ. of Tsukuba and [2]CREST-JST (Japan)*	**15:15 L-8-5** **Reduction of Power Loss of Zero Current Switching Converter by Optimizing Power Devices** *S. Machida[1], N. Kikuchi[1], T. Segawa[2], Y. Shimo[2] and M. Kobayashi[2], [1]Toyota Central R&D Labs. Inc. and [2]Toyota Motor Corp. (Japan)*	**15:00 M-8-5** **Phosphorus Mediated Growth of Ge Layer on Si(001) Substrate** *H. Hanafusa[1], N. Hirose[2], A. Kasamatsu[2], T. Mimura[2], T. Matsui[2] and Y. Suda[1], [1]Tokyo Univ. of Agri. and Tech. and [2]NICT (Japan)*	**15:00 N-8-5** **Mixing Effect in Magnetic Tunnel Junctions** *G. Shiomi[1], Y. Masugata[1], S. Ishibashi[1], H. Tomita[1], D. Maehara[2], T. Nozaki[2], S. Miwa[1], H. Kubota[2], A. Fukushima[2], S. Yuasa[2] and Y. Suzuki[1], [1]Osaka Univ. and [2]AIST (Japan)*
		15:15 I-8-6 **Photoluminescence from n$^+$ -Ge microdisk on Si-on-Insulator Structure** *K. Takinai[1], A. Yoshida[1], Y. Ishikawa[1], K. Wada[1], T. Tsuchizawa[2], T. Watanabe[2], K. Yamada[2] and S. Itabashi[2], [1]Univ. of Tokyo and [2]NTT Microsystem Integration Labs. (Japan)*	**15:30 J-8-6 (Late News)** **Correlation measurement of 1/f noise in semiconductor point contacts with a common lead** *M. Yamagishi[1], M. Hashisaka[1], K. Muraki[2] and T. Fujisawa[1], [1]Tokyo Tech and [2]NTT Basic Res. Labs. (Japan)*	**15:30 K-8-6 (Late News)** **Field-Effect Transistor with Graphene by Direct Alcohol CVD** *M. Ishii, A. Nakamura, H. Inokawa and J. Temmyo, Shizuoka Univ. (Japan)*	**15:30 L-8-6** **Dynamic-Carrier-Distribution-Based Compact Modeling of P-i-N Diode Reverse Recovery Effect** *J. Nakashima, M. Miyake and M. Miura-Mattausch, Hiroshima Univ. (Japan)*	**15:15 M-8-6** **Precise thickness and strain control during epitaxial growth of strained Ge/SiGe multilayers by industrial class CVD** *M. Myronov, X. C. Liu, A. Dobbie and D. R. Leadley, Univ. of Warwick (UK)*	**15:15 N-8-6** **Role of Synthetic Ferrimagnets in MTJs from Wave Packet Dynamics** *M. Arikawa[1], M. Muraguchi[1,2], Y. Hatsugai[1,3], K. Shiraishi[3] and T. Endoh[1], [1]Tohoku Univ., [2]CREST-JST and [3]Univ. of Tsukuba (Japan)*
						15:30 M-8-7 **Boron and Carbon co-doping in high percentage Silicon-Germanium Alloys - Effects of Dopant Incorporation, Strain Compensation and Microstructure -** *A. Reznicek, T. N. Adam, Z. Zhu, J. Li, R. Murphy, S. W. Badell, V. Paruchuri and D.K. Sadana, IBM (USA)*	

Coffee Break

		I-9: Quantum-Dot Devices (Area 7) (16:10-17:25) Chairs: A. Wakahara (Toyohashi Univ. of Tech.) M. Tokushima (AIST)		**K-9: Graphene Device (Area 13)** (16:10-17:25) Chairs: T. Otsuji (Tohoku Univ.) H. Tsuchiya (Kobe Univ.)	**L-9: Novel Concepts (Area 14)** (16:10-17:25) Chairs: N. Usami (Tohoku Univ.) Y. Kurokawa (Tokyo Tech)	**M-9: Characterization of group IV related materials (Area 8)** (16:10-17:10) Chairs: K. Hara (Shizuoka Univ.) H. Hibino (NTT Basic Res. Labs.)	**N-9: Physics of spintronics devices (Area 12)** (16:10-17:25) Chairs: J. H. Zhao (Chinese Academy of Sciences) K. Ito (Hitachi, Ltd.)
		16:10 I-9-1 **Effect of Reduced Stacking Periods on Modulation Bandwidth of Self-Assembled Quantum-Dot Lasers: Theoretical Study** *M. Ishida[1], Y. Tanaka[2,3,4,5], T. Yamamoto[2,3,4,5], M. Sugawara[5] and Y. Arakawa[1], [1]Univ. of Tokyo, [2]Fujitsu Labs. Ltd., [3]Fujitsu Ltd., [4]PETRA and [5]QD Laser, Inc. (Japan)*		**16:10 K-9-1** **Electrical Characterization of Bilayer Graphene Formed by Hydrogen Intercalation of Monolayer Graphene on SiC(0001)** *S. Tanabe, Y. Sekine, H. Kageshima and H. Hibino, NTT Basic Res. Labs. (Japan)*	**16:10 L-9-1** **CO_2 conversion with light and water by GaN photo-electrode** *S. Yotsuhashi[1], M. Deguchi[1], Y. Zenitani[1], R. Hinogami[1], H. Hashiba[1], Y. Yamada[1] and K. Ohkawa[2], [1]Panasonic Corp. and [2]Tokyo Univ. of Sci. (Japan)*	**16:10 M-9-1** **Probing Transverse-Optical Phonons in Strained Si Nanowire: Strain Profiles and Nanomechanical properties** *A. Tarun[1], N. Hayazawa[1], O. Moutanabbir[2] and S. Kawata[1], [1]RIKEN and [2]Max Planck Inst. (MPI) (Japan)*	**16:10 N-9-1** **Giant Zeeman splitting in the magneto-reflectance spectra of a diluted magnetic semiconductor (Zn,Cr)Te** *N. Matsumoto, K. Kanazawa and S. Kuroda, Univ. of Tsukuba (Japan)*
		16:25 I-9-2 **Characterization of wavelength tunable quantum dot external cavity laser (QD-ECL) for 1.3-μm waveband narrow line-width coherent light source** *N. Yamamoto[1], K. Akahane[1], T. Kawanishi[1], Y. Yoshioka[2] and H. Takai[2], [1]NICT and [2]Tokyo Denki Univ. (Japan)*		**16:25 K-9-2** **Electric-field-induced band gap of bilayer graphene in ionic liquid** *Y. Yamashiro, Y. Ohno, K. Maehashi, K. Inoue and K. Matsumoto, Osaka Univ. (Japan)*	**16:25 L-9-2** **Local Characterization of Multicrystalline Silicon Solar Cells through Photothermal and Potential Measurements by Scanning Probe Microscopy** *K. Hara and T. Takahashi, Univ. of Tokyo (Japan)*	**16:25 M-9-2** **Leakage Current Control of Fluoride Ultra-thin Films Grown on Ge Substrates** *K. Takahashi, Y. Hayashi, R. Kayanuma and K. Tsutsui, Tokyo Tech (Japan)*	**16:25 N-9-2** **Observation of magnetic domain wall motion induced by adiabatic spin transfer torque in Co/Ni nanowires** *T. Koyama[1], K. Ueda[1], D. Chiba[1,2], S. Fukami[3], H. Tanigawa[3], T. Suzuki[3], N. Ohshima[3], N. Ishiwata[3], Y. Nakatani[4] and T. Ono[1], [1]Kyoto Univ., [2]PRESTO-JST, [3]NEC Corp. and [4]Univ. of Electro-communications (Japan)*

Friday, September 30

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
		B-9: OTFT application (2) (Area 10)	**C-9: Characterization (3) (Area 2)**		**E-9: Advanced Si Technology (Area 1)**	**F-9: ReRAM (4) (Area 4)**
		16:40 B-9-3 **Inkjet printing of small-molecule semiconductor thin films for high-performance organic transistors** *H. Minemawari[1], T. Yamada[1], M. Matsui[1], J. Tsutsumi[1], S. Haas[1], R. Kumai[1,2] and T. Hasegawa[1], [1]AIST and [2]KEK (Japan)*	**16:50 C-9-3** **Oxidation Resistance of Ti Oxide Self-Formed Barrier in Cu Interconnects** *K. Ito[1], K. Kohama[1], K. Hamasaka[1], Y. Shirai[1] and M. Murakami[2], [1]Kyoto Univ. and [2]The Ritsumeikan Trust (Japan)*		**16:50 E-9-3** **Performance and Variability Comparisons between ALD- and PVD-TiN Gate FinFET** *T. Hayashida[1,2], K. Endo[3], Y. X. Liu[3], S. O'uchi[3], T. Matsukawa[3], W. Mizubayashi[3], S. Migita[3], Y. Morita[3], H. Ota[3], H. Hashiguchi[1], D. Kosemura[1], T. Kamei[1], J. Tsukada[3], Y. Ishikawa[3], H. Yamauchi[3], A. Ogura[1] and M. Masahara[1,3], [1]Meiji Univ., [2]JSPS and [3]AIST (Japan)*	**16:50 F-9-3** **Improving switching characteristics of Cu/Si_xN_y/Pt device with low voltage stress to perform forming** *Q. Liu, H. B. Lv, S. B. Long, W. Wang, Y. T. Li, Y. Wang, M. Wang, K. W. Zhang, H. W. Xie and M. Liu, Chinese Academy of Sci. (China)*
		16:55 B-9-4 **High performance top-contact organic thin-film-transistors using screen printed source and drain electrodes** *Y. Zhao[1], M. Kaltenbrunner[2], T. Sekitani[1], S. Bauer[2] and T. Someya[1], [1]Univ. of Tokyo and [2]Johannes Kepler Univ. Linz (Japan)*	**17:10 C-9-4** **Effects of Cu Film Texture and Barrier Structure on Cu Grain Growth** *K. Kohama[1], T. Matsumoto[1], K. Ito[1], Y. Shirai[1] and M. Murakami[2], [1]Kyoto Univ. and [2]The Ritsumeikan Trust (Japan)*		**17:10 E-9-4 (Late News)** **Extremely scaled (~0.2 nm) equivalent oxide thickness of higher-k ALD-HfO_2 gate stacks** *Y. Morita, S. Migita, W. Mizubayashi and H. Ota, AIST (Japan)*	
		17:10 B-9-5 **Hotpress Method for Thin Crystalline Organic Field-Effect Transistors** *A. Inoue[1], T. Okamoto[1], Y. Joho[1], M. Sakai[1], H. Yamauchi[1], M. Nakamura[1,2] and K. Kudo[1], [1]Chiba Univ. and [2]NAIST (Japan)*				

Friday, September 30

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
		I-9: Quantum-Dot Devices (Area 7)		**K-9: Graphene Device (Area 13)**	**L-9: Novel Concepts (Area 14)**	**M-9: Characterization of group IV related materials (Area 8)**	**N-9: Physics of spintronics devices (Area 12)**
		16:40 I-9-3 **Integrated Amplifier for Gain Spectra Measurement of Bilayer Quantum Dot Laser Material** *H. Shahid[1], D. T. D. Childs[1], M. A. Majid[1], K. Kennedy[1], R. Airey[1], R. A. Hogg[1], E. Clarke[2], P. Spencer[2] and R. Murray[2], [1]Univ. of Sheffield and [2]Imperial College (UK)*		**16:40 K-9-3** **Electron tunneling in bilayer graphene *p-n* junction controlled by gate electric field** *H. Miyazaki[1,2], M. Lee[1], S. L. Li[1], A. Kanda[2,3] and K. Tsukagoshi[1,2], [1]MANA, NIMS, [2]CREST-JST and [3]Univ. of Tsukuba (Japan)*	**16:40 L-9-3** **Impact of light element impurities on crystalline defect generation in silicon substrate** *T. Tachibana[1], T. Sameshima[1], T. Kojima[2], K. Arafune[3], K. Kakimoto[4], Y. Miyamura[5], H. Harada[5], T. Sekiguchi[5], Y. Ohshita[2] and A. Ogura[1], [1]Meiji Univ., [2]Toyota Tech. Inst., [3]Univ. of Hyogo, [4]Kyusyu Univ. and [5]NIMS (Japan)*	**16:40 M-9-3** **Analysis of Atomic Arrangement at 3C-SiC/Si(001) Interface by Aberration-Corrected Transmission Electron Microscopy** *J. Yamasaki, S. Inamoto, H. Tamaki and N. Tanaka, Nagoya Univ. (Japan)*	**16:40 N-9-3** **Magnetic States and Minor loop analysis in Co/Cu/Co trilayer ring structures** *A.S. Demiray[1], T. Miyawaki[1], Y. Watanabe[1], M. Kohda[1,2] and J. Nitta[1], [1]Tohoku Univ. and [2]PRESTO-JST (Japan)*
		16:55 I-9-4 **Optimization of quantum dot molecular beam epitaxy diode for broadband applications** *M. A. Majid, M. Hugues, D. T. D. Childs and R. A. Hogg, Univ. of Sheffield (UK)*		**16:55 K-9-4** **Gating Operation of Transport Current in Graphene Nanoribbon Fabricated by Helium Ion Microscope** *S. Nakaharai[1], T. Iijima[2], S. Ogawa[2], H. Miyazaki[3], S. Li[3], K. Tsukagoshi[3], S. Sato[1] and N. Yokoyama[1], [1]AIST-GNC, [2]AIST-ICAN and [3]NIMS-MANA (Japan)*	**16:55 L-9-4** **Flash-Lamp-Induced Explosive Crystallization of Amorphous Films Leaving Behind Periodic Microstructures** *K. Ohdaira[1,2] and H. Matsumura[1], [1]JAIST and [2]PRESTO-JST (Japan)*	**16:55 M-9-4 (Late News)** **Germanium layer Transfer with Epitaxial Lift-off Technique** *T. Maeda[1], H. Ishii[1], T. Itatani[1], T. Takada[2], M. Hata[2] and T. Yasuda[1], [1]AIST and [2]Sumitomo Chemical Co., Ltd. (Japan)*	**16:55 N-9-4 (Invited)** **Spin Current Generation and Utilization in Metals and Insulators** *Eiji Saitoh, [1]Tohoku Univ. ,[2]CREST-JST and [3]ASRC-JAEA (Japan)*
		17:10 I-9-5 **Photoresponse improvement of InAs/GaAs quantum dot infrared photodetectors using $GaAs_{1-x}Sb_x$ overgrown layer** *C. T. Huang, Y. C. Chen and S. C. Lee, National Taiwan Univ. (Taiwan)*		**17:10 K-9-5** **RF Performance of Graphene Nano-Ribbon MOSFET vs. TFET** *V. P. Sreenivas, K.T. Lam and G. Liang, National Univ. of Singapore (Singapore)*	**17:10 L-9-5** **Preparation of a Diameter-controlled Silicon Nanowire Array by Metal Assisted Chemical Etching using Silica Nanoparticles (MACES)** *S. Kato[1], Y. Watanabe[1], Y. Kurokawa[1], A. Yamada[1], Y. Ohta[2], Y. Niwa[2] and M. Hirota[2], [1]Tokyo Tech and [2]Nissan Res. Center (Japan)*		

RUMP SESSIONS

–September 29 (Thursday) 19:00-21:00

Session A (5F Hall 1)

"Opportunities and Challenges of Heterogeneous Integration on CMOS" -Photonics, MEMS, Sensors, etc -

Si CMOS miniaturization has brought great impacts on information and communication technologies for a long time. Miniaturization, so called More Moore, is going to down to less than 10nm, although there may be various technological difficulties and economical obstacles. Heterogeneous integration and/or integration with diverse functionalities such as photonics, MEMS (Micro Electro Mechanical Systems), sensing, etc., so called More Than Moore, is expected to open the new paradigm. In this rump session, experts of photonics, MEMS, sensing, and CMOS will discuss what is expected to be brought by heterogeneous integration, and how we should collaborate for their convergence system.

Organizer: S. Miyazaki (Nagoya Univ.)

Moderators: K. Masu (Tokyo Tech)
J. Fujikata (NEC Corp.)

Panelists: Y. Arakawa (Univ. of Tokyo)
N. Nishiyama (Tokyo Tech)
T. Seki (Omron Corp.)
T. Ohguro (Toshiba Corp.)
K. Maenaka (Univ. of Hyogo)

Session B (5F Hall 2)

"Future Roadmap for Graphene Science and Technology"

Graphene is a new class of two-dimensional materials and has a wide range of potential applications. In this rump session, panelists will propose optimistic scenarios for future graphene science and technology in several categories; quantum electronics, nanostructure, production, process, transistors, photonics, transparent electrodes, and so on. Some of the most difficult hurdles for the future will be picked up for each category, and the current challenges will be explained. By predicting how and when the hurdles are overcome in an optimistic manner, the future roadmap for graphene science and technology will be built.

Organizer: H. Yamaguchi (NTT Corp.)

Moderators: T. Otsuji (Tohoku Univ.)
H. Hibino (NTT Corp.)

Panelists: T. Ihn (ETH Zurich)
K. Nagashio (Univ. of Tokyo)
S. Sato (AIST)
S. Tanaka (Kyushu Univ.)
K. Uchida (Tokyo Tech)

SHORT COURSES

September 27, 2011, Nagoya University

=Short Course (1)=

Materials and Processing for Advaced CMOS – From Fundamentals to State-of-the-Art –

Organizer : Seiichi Miyazaki (Nagoya University)

This short course is aimed at graduated students and young researchers from both industry and academia, and world's leading experts in the field of silicon technology will lecture on the fundamental aspect and knowledge about material processing and device technologies for Si CMOS devices including the overview of technological issues and challenges in the past, today and the future. All lectures will be done in English, and all participants at SSDM 2011 are welcome.

10:00 - 11:30 **Plenary Lecture**
"3D Integration Technology and New Application"
Mitsumasa Koyanagi, New Industry Creation Hatchery Center, Tohoku University

(11:30 - 12:30 Lunch)

12:30 - 13:15 "Review on Advanced Gate Stack Technology"
Byoung Hun Lee, Gwangju Institute of Science and Technology

13:15 - 14:00 "Channel Engineering for Advanced CMOS Devices"
Shinichi Takagi, The University of Tokyo

14:00 - 14:45 "Control of Plasma-Surface Reactions for Next Generation Semiconductor Devices"
Tetsuya Tatsumi, Sony Corporation, Keio University

(14:45 - 15:00 Break)

15:00 - 15:45 "Advanced Lithography"
Shinji Okazaki, EUVA/GIGAPHOTON INC.

15:45 - 16:30 "Random Variability in Scaled MOS Transistors"
Toshiro Hiramoto, The University of Tokyo

16:30 - 17:30 Lab Tours

=Short Course (2)=

Fundamentals and Applications of Carbon Nanotube and Graphene

Organizers : Yutaka Ohno (Nagoya University)
Shintaro Sato (AIST)

This short course is intended for students and young researchers who are interested in electronics applications of carbon nanotubes and graphene. The world's leading experts in this field will lecture on their fundamental electronic structure and transport phenomena, growth and characterization techniques, device and conductor applications, together with recent progresses and future aspects. All lectures will be done in English, and all SSDM participants from overseas as well as Japan are welcome.

10:00 - 11:30 **Plenary Lecture**
"3D Integration Technology and New Application"
Mitsumasa Koyanagi, New Industry Creation Hatchery Center, Tohoku University

(11:30 - 12:30 Lunch)

12:30 - 13:15 "Electron and Phonon of Graphene Related Materials"
Riichiro Saito, Tohoku University

13:15 - 14:00 "Graphene Transport Modulated by Gate Electric field"
Kazuhiko Tsukagoshi, Hisao Miyazaki, Song-Lin Li, NIMS-MANA, CREST-JST

14:00 - 14:45 "Recent Advances in Growth and Characterization of Graphene and Nanotubes"
Hiroki Ago, Kyushu University

(14:45 - 15:00 Break)

15:00 - 15:45 "Carbon Nanotubes for VLSI: Interconnect and Transistor Applications"
Yuji Awano, Keio University

15:45 - 16:30 "Graphene Films for Electronic Applications"
Jong-Hyun Ahn, Sungkyunkwan University

16:30 - 17:30 Lab Tours

WORKSHOPS

September 27, 2011, WINC AICHI

=Workshop (1)=

Current Status and Future Prospective of Wide Gap Semiconductor Power Devices

Organizers : Hideto Miyake (Mie University)
Tatsuo Oomori (Mitsubishi Electric Corporation)

The power devices with wide bandgap semiconductors such as SiC and GaN are essentially superior to the Si device in the high breakdown electric field and the high-temperature operation. This year will be the first year when the power devices and HEMTs using SiC and GaN would come into practical applications, and the future trends are focused on. This workshop covered a broad range of areas from the crystal growth of SiC and GaN to their device applications.

13:00 - 13:45 "Seeking New Application Fields Using Group III Nitrides"
Hiroshi Amano, Nagoya University

13:45 - 14:30 "Automotive Applications of GaN Power Devices"
Tetsu Kachi and Tsutomu Uesugi, Toyota Central R&D Labs., Inc.

14:30 - 15:15 "Recent Progress of GaN HEMT for High Frequency and High Power Applications"
Masahito Kanamura, Toshihide Kikkawa, Fujitsu Labs. Ltd.

(15:15 - 15:30 Break)

15:30 - 16:15 "Progress and Future Challenges of SiC Power Devices"
Tsunenobu Kimoto, Kyoto University

16:15 - 17:00 "Development of SiC Single Crystals Growth"
Jun Kojima, Kazukuni Hara, Shoichi Yamauchi, Shoichi Onda,
R&D Partnership for Future Power Electronics Technology Research Laboratories, DENSO CORPORATION

17:00 - 17:45 "Recent Progress of SiC Power Devices and Remaining Issues"
Tatsuo Oomori, Masayuki Imaizumi, Mitsubishi Electric Corporation

=Workshop (2)=

Recent Advancement in Printed Organic Electronics

Organizers : H. Usui (Tokyo University of Agriculture and Technology)
T. Someya (The University of Tokyo)

Rapid progress in organic electronics has been achieved in recent years, leading to promising results in the field of organic light emitting diodes (OLEDs) and organic field effect transistors (OFETs). Instead of replacing the conventional inorganic semiconductors, the final goal of organic electronics is considered to realize printed electronics, which can bring about innovative breakthrough in cost effectiveness, large scale, as well as flexibility. Although the roll-to-roll printed organic electronics have some ways to come into the market, there has been the steady progress in this area in recent years. This workshop reviews the current status and perspective of printed organic electronics especially in viewpoint of processing and application technologies.

13:00 - 13:45 "Introductory Talk and Overview of Printed Organic Electronics"
Takao Someya, The University of Tokyo

13:45 - 14:30 "Low-Temperature / High Resolution Printing Techniques for Flexible TFT Devices"
Toshihide Kamata,
National Institute of Advanced Industrial Science and Technology

14:30 - 15:15 "Flexible TFT Array by Printing Method"
Manabu Ito, Display Research Laboratory,
Technical Research Institute, Toppan Printing Co., Ltd.

(15:15 - 15:30 Break)

15:30 - 16:15 "A Rollable OLED Display Driven by OTFT"
Mao Katsuhara, Makoto Noda, Norihito Kobayashi, Akira Yumoto,
Ryouichi Yasuda, Shinichi Ushikura, Gen Yukawa, Nobukazu Hirai,
Iwao Yagi, and Kazumasa Nomoto,
Display Device Development Division, Sony Corporation

16:15 - 17:00 "Printed Electronics for Large Area Flexible Device"
Hiroki Maeda, Research & Development Center, Dai Nippon Printing Co., Ltd.

17:00 - 17:45 "Roll-to-Roll Gravure Printing Process for Penny RFID Tags"
Minhun Jung[1,2], Jinsoo Noh[1,2], Joonseok Kim[1,2], Kyunghwan Jung[1,2],
Hwiwon Kang[1,2], ChaeminLim[1,2], Soyeon Kim[2], Kwangyong Lee[1],
Daae Kim[2], Dongsun Yeom[2], Yongsu Park[1], Minjin Lee[1],
Donghwan Kim[1,2], Yong-Gil Lee[2], Kwangyong Park[2] and Gyoujin Cho[1],
[1]Sunchon National University, [2]Printed Electronics Research Institute, Paru Co., Ltd.

INSTRUCTION FOR SPEAKERS

Oral Presentation:

Time Schedule

	Total session time	Presentation time	Discussion time
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	10 min.	5 min.

BELL: First: Warning, Second: End of speech, Third: End of discussion.

Audio-Visual Equipment

The following equipments are ready at each conference meeting room during SSDM 2011:

* LCD projector
* PC (laptop computer), Windows XP, PowerPoint 2003-2010 and PDF
  The use of personal PCs for presentations is prohibited.
* Microphone
* Projection laser pointer

Uploading Your Presentation

The single most important action of authors is to upload your presentation file to the PC in each session room using your own USB thumb drive. It is the presenter's responsibility to **upload the slide file as soon as possible in each session room at any break** well in advance to the session of presentation. At a short break, the PC may be too crowded to upload the file. If the chairman cannot find your presentation file at the beginning of the session, your presentation will be withdrawn.

In the presentation PC, each presenter's file should be positioned in the folder that corresponds to the session of presentation. The file must be compatible with Microsoft PowerPoint 2010 or Adobe Acrobat 9 on Microsoft Windows. Compatibility can be checked at the Speakers Room, Conference Room 1106 on 11th floor where the same PCs as in each session room are installed. Details will be informed on SSDM website at http://www.ssdm.jp.

Poster Presentation:

Presenting Poster

Poster sessions are scheduled for Thursday, September 29 from 13:30 to 15:00 at Exhibition Hall on 6th floor. Poster boards will be available with identifying labels. Authors are requested to prepare their posters between 10:00 and 15:00 on September 29 and remove them by 15:30 on September 29. Please note that after 16:00 all the remaining poster will be destroyed. Usable space on each poster board will be approximately 900 mm wide and 2,100 mm high. Pushpins will be available.

Each presentation will be assigned a board, labeled with the abstract number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near by their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are required to make 2 minutes short oral presentation on September 29. The presentation time should be kept strictly to 2 minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations should be held in a quick, successive sequence. While one speaker is giving his/her presentation, next speakers should wait nearby in line for their turn in order to move on to the next presentation.

Please note that any absent speakers will be skipped and each presentation will be automatically stopped after 2 minutes have elapsed. Only a PC projector will be made available.

Short oral presentations will be held as follows:

Area 1	11F 1102
Area 2	10F 1003
Area 3	11F 1101
Area 4	11F 1103
Area 5	11F 1104
Area 6	5F Hall 1
Area 7	12F 1201
Area 8	12F 1207
Area 9	12F 1202
Area 10	10F 1002
Area 11	11F 1107
Area 12	12F 1208
Area 13	12F 1203
Area 14	12F 1204

Confidentiality:

We will delete all electronic files from the SSDM computers after presentations are completed. SSDM will not publish or distribute the presentation material.

Agreement not to pre-publication abstracts:

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to the presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

EXHIBITION

On the days of the conference SSDM 2011 Exhibition will be held at Conference Room 1001, 10F of WINC AICHI. The show will feature the displays of the latest products of the following exhibitors. Complementary coffee service will be available at the Room 1001 during the intermissions of the technical sessions.

Exhibitors:

ELIONIX INC
HiSOL,Inc.
JEOL Ltd**.**
NTT Microsystem Integration Laboratories
R-DEC Co., Ltd.
SILVACO, Inc.
TNS Systems LLC
Tokai Region Nanotechnology Manufacturing Cluster

Show dates and hours:

September 28 : 8:30 - 18:00
September 29 : 8:30 - 19:00
September 30 : 8:30 - 14:00

AUTHOR INDEX

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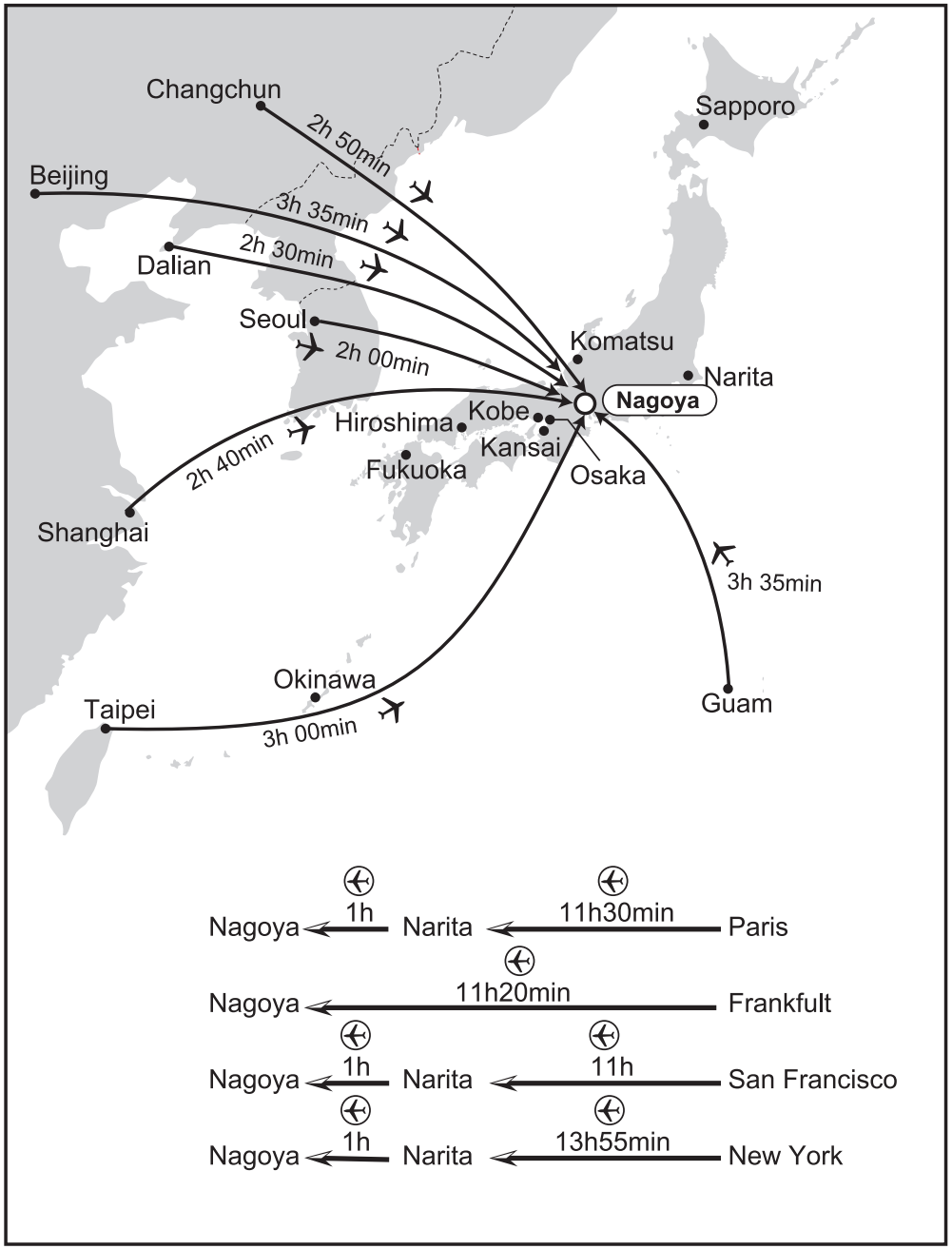
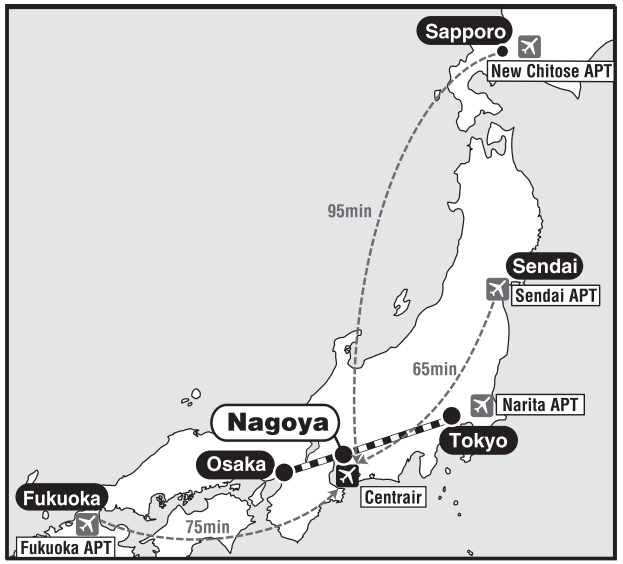
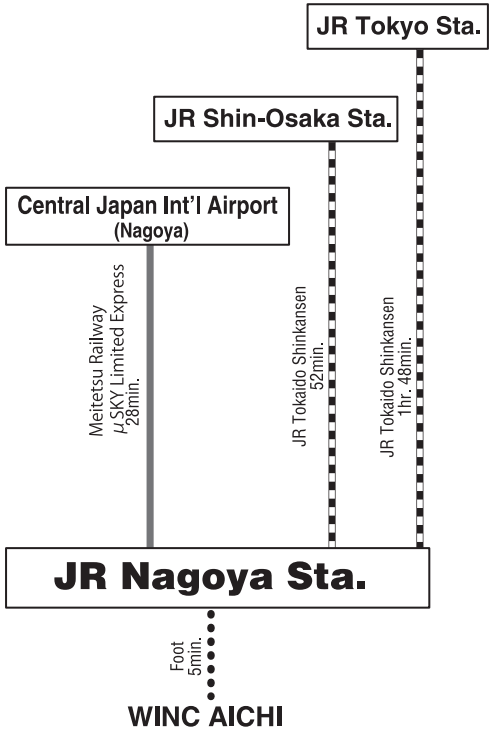


ACCESS TO WINC AICHI





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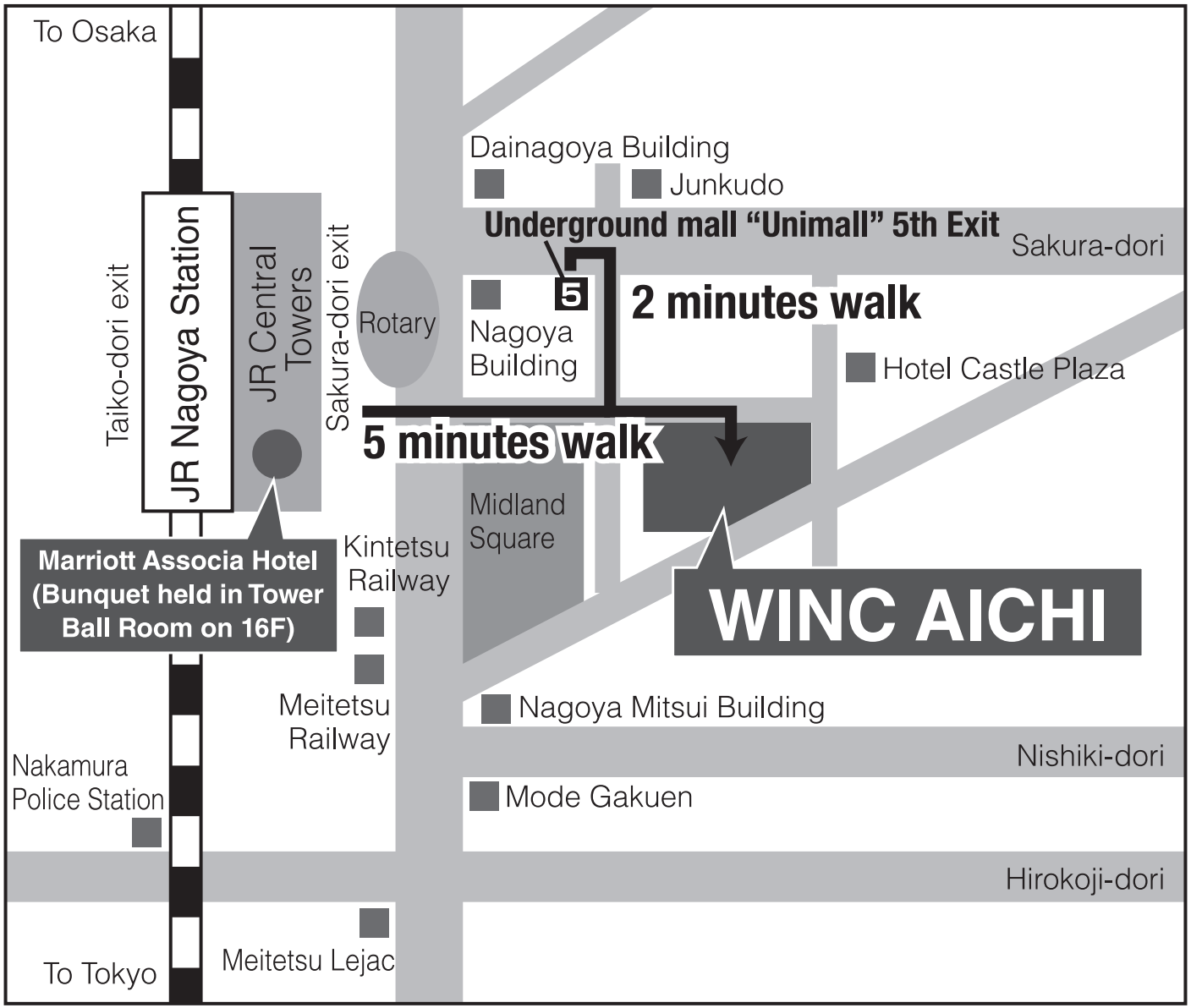
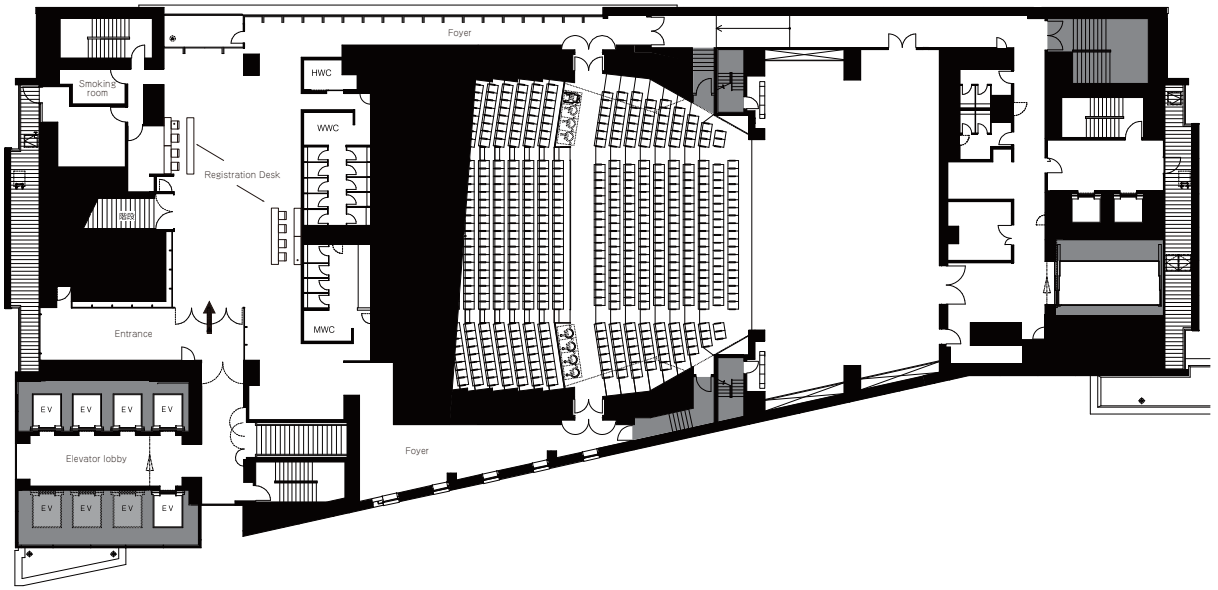
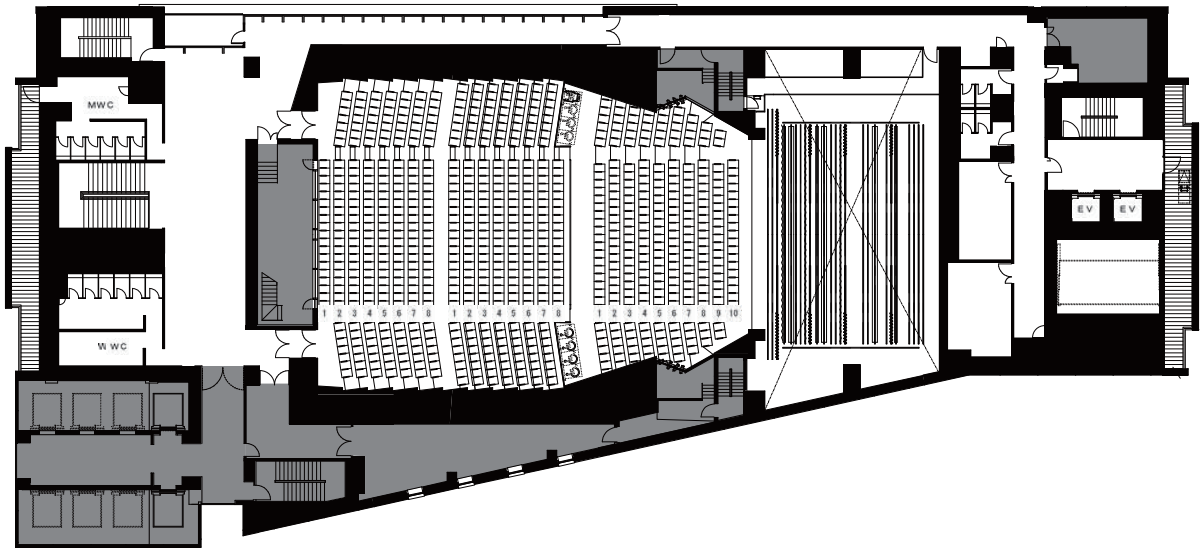


FLOOR GUIDE

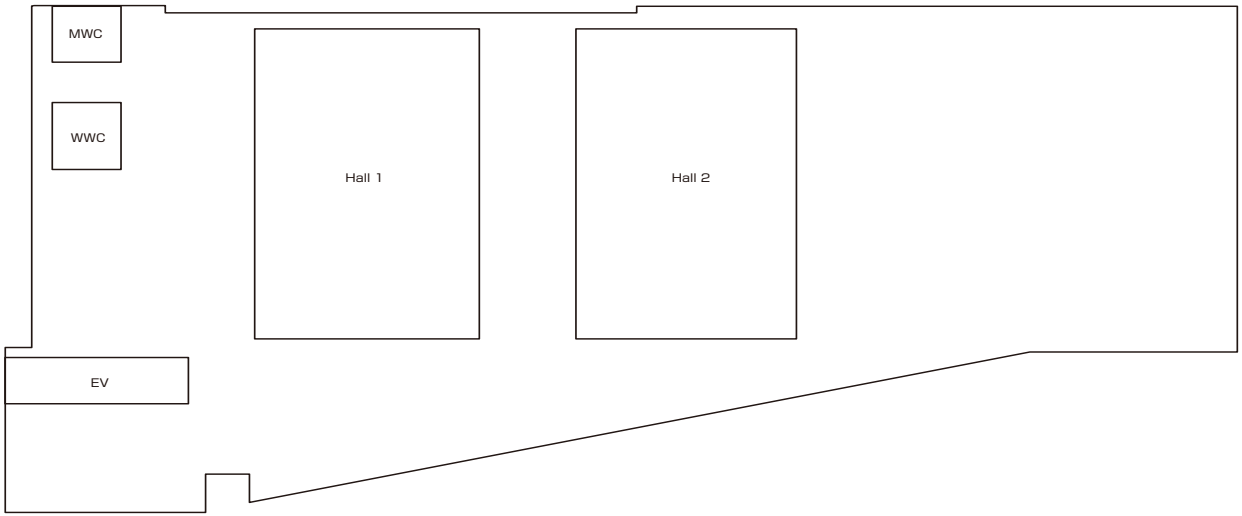
2F WINC HALL



3F WINC HALL



5F HALL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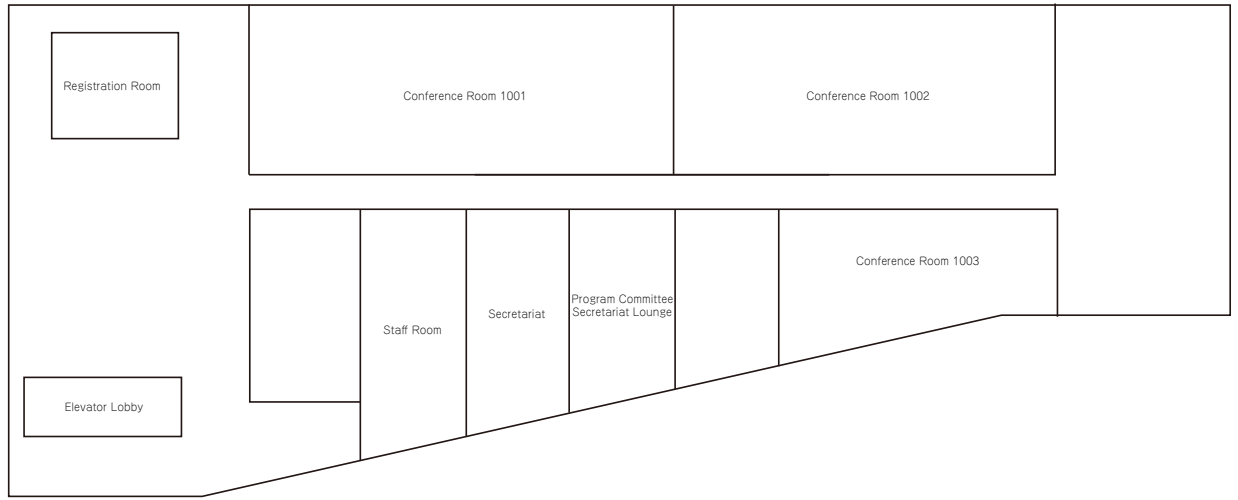
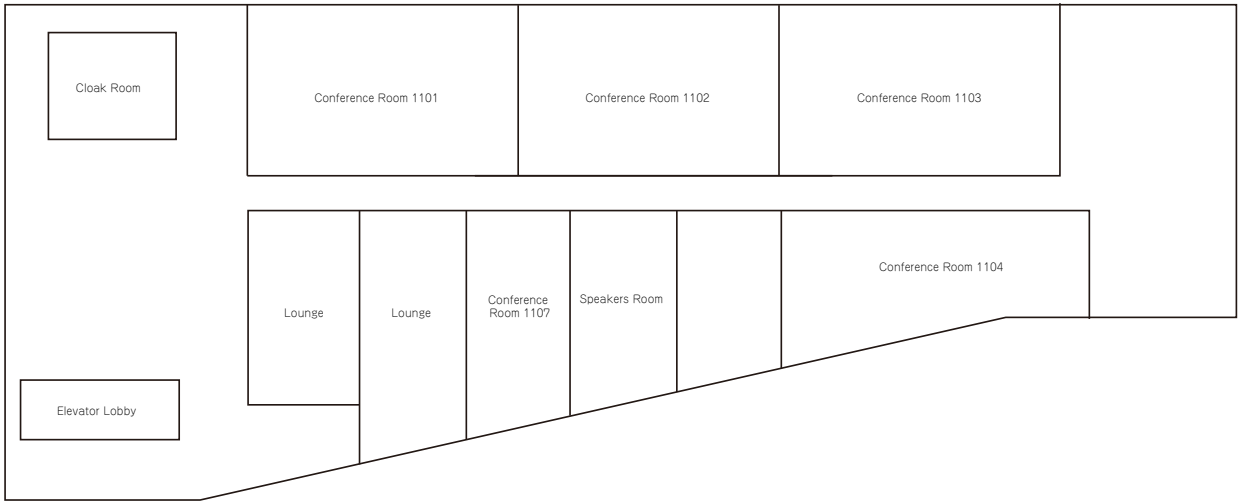
EV

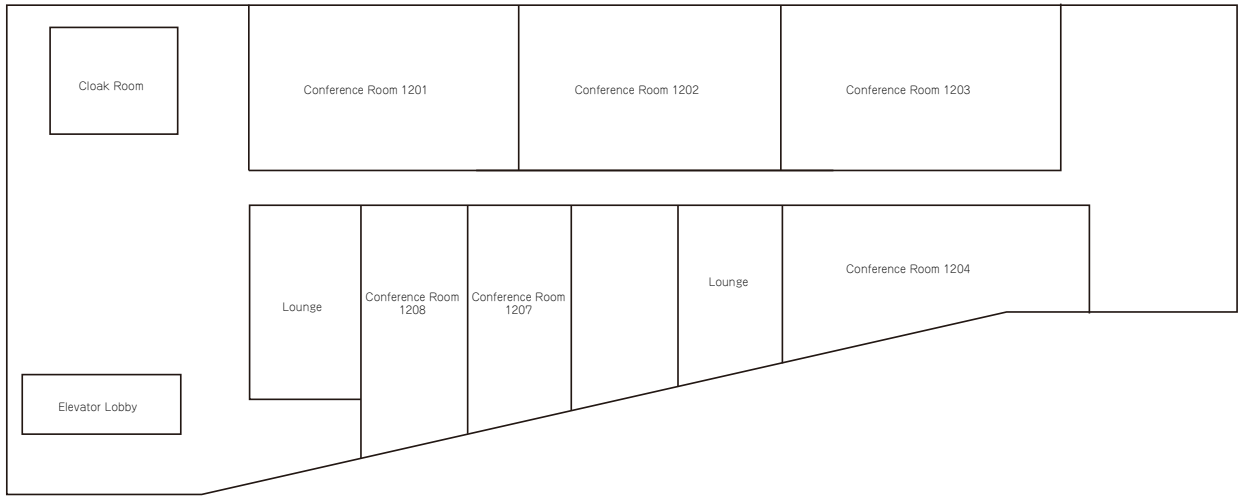
10F


Registration Room
Conference Room 1001
Conference Room 1002
Conference Room 1003
Staff Room
Secretariat
Program Committee
Secretariat Lounge
Elevator Lobby

11F


Cloak Room
Conference Room 1101
Conference Room 1102
Conference Room 1103
Lounge
Lounge
Conference Room 1107
Speakers Room
Conference Room 1104
Elevator Lobby

12F


Cloak Room
Conference Room 1201
Conference Room 1202
Conference Room 1203
Lounge
Conference Room 1208
Conference Room 1207
Lounge
Conference Room 1204
Elevator Lobby

MEMO

PROGRAM TIME TABLE

Wednesday, September 28

9:30-12:15 Opening & Plenary Sessions (2F WINC HALL)

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
13:30-15:15 Area 6: A-1: GaN FET Technologies	**13:30-15:15 Area 10&14:** BL-1: Organic Photovoltaics (1)	**13:30-15:15 Area 10:** B-1: OLEDs	**13:30-15:15 Area 2:** C-1: Future Interconnect	**13:30-15:10 Area 3:** D-1: Modeling and Circuits	**13:30-15:20 Area 1:** E-1: Ge-MOS	**13:30-15:00 Area 4:** F-1: STT-RAM
15:40-16:55 Area 6: A-2: III-V HBTs and FETs	**15:40-17:25 Area 10&14:** BL-2: Organic Photovoltaics (2)	**15:40-17:25 Area 10:** B-2: Organic device fabrication process and interface control		**15:40-17:00 Area 3:** D-2: Device & Characteristics	**15:45-17:15 Area 1:** E-2: Characterization in Gate Stacks	**15:40-17:30 Area 4:** F-2: FeRAM/DRAM/SRAM

19:00-21:00《Banquet/Young Researcher Award (16F, Tower Ball Room, Marriott Associa Hotel)》

Thursday, September 29

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
		9:00-10:15 Area 10: B-3: Novel structure and fabrication process for OTFT	**9:00-10:00 Area 2:** C-3: Memory Application		**9:00-10:20 Area 1:** E-3: Process Technology and Analysis	**9:00-10:00 Area 4:** F-3: NAND
10:45-12:00 Short Presentation Area 6		**10:45-12:00 Short Presentation** Area 10	**10:45-12:00 Short Presentation** Area 2	**10:45-12:00 Short Presentation** Area 3	**10:45-12:00 Short Presentation** Area 1	**10:45-12:00 Short Presentation** Area 4

13:30-15:00《Poster Session》6F Exhibition Hall

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
15:25-16:25 Area 6: A-4: Novel III-V Devices and Applications	**15:25-16:40 Area 8&13:** KM-4: Nanowire Growth and Characterization	**15:25-16:40 Area 10:** B-4: Organic memory and photonic devices (1)	**15:25-16:35 Area 2:** C-4: Characterization (1)	**15:25-16:45 Area 3:** D-4: Tunnel-FET	**15:25-16:55 Area 1:** E-4: Junction Technology and Physics	**15:25-16:25 Area 4:** F-4: e-Flash
17:05-18:20 Area 6: A-5: Oxide Devices	**17:05-18:20 Area 8&13:** KM-5: Nanowire and Quantum Structures	**17:05-18:20 Area 10:** B-5: Organic memory and photonic devices (2)	**17:05-18:25 Area 2:** C-5: 3D Interconnect (1)	**17:05-18:25 Area 3:** D-5: Noise and Fluctuation	**17:20-18:20 Area 1:** E-5: Ge Metallization	**17:05-18:05 Area 4:** F-5: CT-Flash

19:00-21:00《Rump Sessions》5F Hall 1 "Opportunities and Challenges of Heterogeneous Integration on CMOS" - Photonics, MEMS, Sensors, etc - , 5F Hall 2 "Future Roadmap for Graphene Science and Technology"

Friday, September 30

5F Hall 1	5F Hall 2	10F 1002	10F 1003	11F 1101	11F 1102	11F 1103
9:00-10:45 Area 6&14: AL-6: SiC&GaN Power Switching Devices (1)	**9:00-10:45 Area 8&13:** KM-6: Graphene Synthesis	**9:00-10:45 Area 10:** B-6: Device physics and characterization of OTFT (1)		**9:00-10:30 Area 3:** D-6: Advanced CMOS Devices	**9:00-10:20 Area 1:** E-6: Ge Process Technology (1)	**9:00-10:50 Area 4:** F-6: PRAM/ReRAM (1)
11:15-12:30 Area 6&14: AL-7: SiC&GaN Power Switching Devices (2)	**11:15-12:30 Area 8&13:** KM-7: Graphene Application	**11:15-12:30 Area 10:** B-7: Device physics and characterization of OTFT (2)		**11:15-12:25 Area 3:** D-7: ET-SOI and Nanowire Devices	**10:45-12:05 Area 1:** E-7: Ge Process Technology (2)	**11:15-12:40 Area 4:** F-7: ReRAM (2)
14:00-15:30 Area 6: A-8: Processing and Characterization Technologies		**14:00-15:45 Area 10:** B-8: OTFT application (1)	**14:00-15:50 Area 2:** C-8: 3D Interconnect (2) and Characterization (2)	**14:00-15:30 Area 3:** D-8: Device Reliability	**13:35-15:55 Area 1:** E-8: III-V CMOS Technology	**14:00-15:40 Area 4:** F-8: ReRAM (3)
		16:10-17:25 Area 10: B-9: OTFT application (2)	**16:10-17:30 Area 2:** C-9: Characterization (3)		**16:10-17:25 Area 1:** E-9: Advanced Si Technology	**16:10-17:10 Area 4:** F-9: ReRAM (4)

Area Scope

Area 1: Advanced LSI Processing & Materials Science
Area 2: Advanced Interconnect / Materials Technology and Characterization
Area 3: CMOS Devices / Device Physics
Area 4: Advanced Memory Technology
Area 5: Advanced Circuits and Systems
Area 6: Compound Semiconductor Electron Devices and Related Technologies
Area 7: Photonic Devices and Optoelectronic Integration
Area 8: Advanced Material Synthesis and Crystal Growth Technology
Area 9: Physics and Application of Novel Functional Devices and Materials
Area 10: Organic Materials Science, Device Physics, and Applications

PROGRAM TIME TABLE

Wednesday, September 28

9:30-12:15 Opening & Plenary Sessions (2F WINC HALL)

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
13:30-15:10 Area 5&11: GH-1: Image Sensor and MEMS Technology (1)		**13:30-15:15 Area 7:** I-1: Optical Link and Related Devices		**13:30-15:15 Area 13:** K-1: CNT Property	**13:30-15:15 Area 14:** L-1: Quantum Well& III-V Solar Cell	**13:30-15:15 Area 8:** M-1: Nitrides	
15:40-17:20 Area 5&11: GH-2: Image Sensor and MEMS Technology (2)		**15:40-17:10 Area 7:** I-2: Photonic Crystals		**15:40-17:10 Area 13:** K-2: CNT Device	**15:40-17:25 Area 14:** L-2: Thin-Film Silicon Solar Cells	**15:40-17:25 Area 8:** M-2: Oxides	

19:00-21:00《Banquet/Young Researcher Award (16F, Tower Ball Room, Marriott Associa Hotel)》

Thursday, September 29

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
9:00-10:15 Area 5: G-3: Variation and Reliability	**9:00-10:15 Area 11:** H-3: Electric, Magnetic and Optical Biosensing	**9:00-10:15 Area 7:** I-3: Plasmonics and Nonlinear Devices	**9:00-10:15 Area 9:** J-3: Graphene Quantum Transport	**9:00-10:00 Area 13:** K-3: Nanowire/Nanotube FET	**9:00-10:15 Area 14:** L-3: Compound Thin Film Solar Cells	**9:00-10:15 Area 8:** M-3: III-V Compounds	
10:45-12:00 Short Presentation Area 5	**10:45-12:00 Short Presentation** Area 11	**10:45-12:00 Short Presentation** Area 7	**10:45-12:00 Short Presentation** Area 9	**10:45-12:00 Short Presentation** Area 13	**10:45-12:00 Short Presentation** Area 14	**10:45-12:00 Short Presentation** Area 8	**10:45-12:00 Short Presentation** Area 12

13:30-15:00《Poster Session》6F Exhibition Hall

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
15:25-16:35 Area 5: G-4: Circuits for 3D Structure	**15:25-16:40 Area 11:** H-4: Neural Interface Technology	**15:25-16:25 Area 7:** I-4: Novel Optical Devices	**15:25-16:40 Area 9:** J-4: Advanced MOSFETs and Transport				
17:05-18:20 Area 5: G-5: RF Circuits (1)		**17:05-18:05 Area 7:** I-5: Er-Doped Devices	**17:05-18:20 Area 9:** J-5: MEMS & Thin-Film Devices				

19:00-21:00《Rump Sessions》5F Hall 1 "Opportunities and Challenges of Heterogeneous Integration on CMOS" - Photonics, MEMS, Sensors, etc - , 5F Hall 2 "Future Roadmap for Graphene Science and Technology"

Friday, September 30

11F 1104	11F 1107	12F 1201	12F 1202	12F 1203	12F 1204	12F 1207	12F 1208
9:00-10:50 Area 5: G-6: Analog and Digital Circuits	**9:00-10:45 Area 11:** H-6: Micro Fabrication and Micro fluidic Devices	**9:00-10:45 Area 2&7:** CI-6: Optical Interconnect (1)	**9:00-10:45 Area 9:** J-6: Photon & Spin in Nanostructures				**9:00-10:45 Area 12:** N-6: Spintronics materials and devices
11:15-12:35 Area 5: G-7: RF Circuits (2)	**11:15-12:15 Area 11:** H-7: Nano fabrication and Application	**11:15-12:25 Area 2&7:** CI-7: Optical Interconnect (2)	**11:15-12:30 Area 9:** J-7: Quantum Transport in Nanostructures				**11:15-12:30 Area 12:** N-7: Spin transport in semiconductors
		14:00-15:30 Area 7: I-8: SiGe-Based Optical Devices	**14:00-15:45 Area 9:** J-8: Qubit and Novel Functional Devices	**14:00-15:45 Area 13:** K-8: Graphene Property	**14:00-15:45 Area 14:** L-8: Power Devices & ICs	**14:00-15:45 Area 8:** M-8: Growth techniques of Si and Ge	**14:00-15:30 Area 12:** N-8: Circuit application of spintronics devices
		16:10-17:25 Area 7: I-9: Quantum-Dot Devices		**16:10-17:25 Area 13:** K-9: Graphene Device	**16:10-17:25 Area 14:** L-9: Novel Concepts	**16:10-17:10 Area 8:** M-9: Characterization of group IV related materials	**16:10-17:25 Area 12:** N-9: Physics of spintronics devices

Area 11: Micro/Nano Electromechanical Systems and Bio/Medical Analyses
Area 12: Spintronics Materials and Devices
Area 13: Application of Nanotubes, Nanowires, and Graphene
Area 14: Photovoltaics & Power Semiconductor Devices

2011 International Conference on Solid State Devices and Materials (SSDM 2011)

SECRETARIAT

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