ADVANCE PROGRAM

2010 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference September 22-24, 2010
Short Course September 21, 2010
Place The University of Tokyo
(Hongo Campus)
Tokyo Dome Hotel

Sponsored by
The Japan Society of Applied Physics
Technical-Cosponsored by
IEEE Electron Devices Society
in cooperation with
The Electrochemical Society of Japan
IEEE EDS Japan Chapter
The Institute of Electrical Engineers of Japan
The Institute of Electronics, Information and Communication Engineers
The Institute of Image Information and Television Engineers
Japan Institute of Electronics Packaging

ssdm 2010

Web Site : http://www.ssdm.jp

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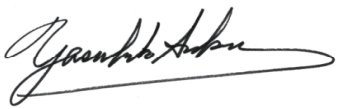
PREFACE

On behalf of the organizing committee, it is my great pleasure and honor to welcome you to the 42nd International Conference on Solid State Devices and Materials (SSDM 2010), held on September 22-24, 2010 in Tokyo, Japan. SSDM 2010 is sponsored by the Japan Society of Applied Physics and technically co-sponsored by the IEEE Electron Devices Society.
SSDM is one of the most important and large-scale conferences in the field of solid state device technologies and materials, presenting the latest scientific achievements and exchanging technical information. SSDM has been continuously growing and increasing its significance as a unique conference covering a broad spectrum of the area; SSDM covers a very wide scope and includes the physics and processing technology of electron devices, photonic devices and organic devices as well as their materials and integration into circuits and systems.

This year, the venue of the SSDM 2010 is the Hongo Campus, the main campus of the University of Tokyo. Usually, SSDM is held at a conference center or related facility. As academia takes an ever increasing and important role in the SSDM and as university campuses are open to public, SSDM 2010 is of great significance. The opening and plenary sessions will be held at Yasuda Auditorium standing at the heart of the campus as a symbol of the university as a whole. In the plenary session, we are pleased to invite two distinguished speakers, Dr. Michiharu Nakamura and Dr. Simon Deleonibus who will speak on the future prospects of nanoelectronics and 3D LSI technology, respectively. In addition, SSDM 2010 features a special plenary session entitled “A half century of Esaki diode and lasers” which will be held at the Tokyo Dome Hotel just before the conference reception in the evening on the same day. We are honored to have an opportunity to listen to commemorative lectures by two great scholars of erudition, Professor Koichi Shimoda and Professor Leo Esaki. We hope all participants, especially young researchers and students, will be stimulated and encouraged by these lectures.
Reflecting the international nature of SSDM, 889 high quality abstracts were submitted to SSDM 2010 from 23 countries. A great effort by the technical program committee for the selection of the abstracts results in an excellent technical program consisting of 66 invited papers, including the four plenary talks, 335 contributed oral papers, 214 poster papers and 40 late news papers. The papers have been categorized into 14 sub-areas, covering advanced and important topics. We hope all the papers presented at SSDM 2010 address in depth nearly all the key issues of the field and provide stimulation and new perspectives to all participants.

We wish to express our sincere appreciation to all the committee members for their tremendously significant contribution to the SSDM 2010. We also express our hearty gratitude to the financial support provided by the supporting corporations and foundations including MEXT-JSPS. Finally, we sincerely hope SSDM2010 enhances your research for upcoming years and provides you with an invaluable experience.

September 2010



Yasuhiko ARAKAWA
General Chair, SSDM 2010
Professor, The University of Tokyo

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as of August 31, 2010

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as of August 31, 2010

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Y. Taguchi (Keio Univ.)
Y. S. Yang (National Chiao Tung Univ.)

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Y. Ohno (Tohoku Univ.)
M. Oogane (Tohoku Univ.)
H. Saito (AIST)
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S. Sato (AIST)
K. Tateno (NTT Corp.)
S. Uno (Nagoya Univ.)
S. J. Wind (Columbia Univ.)

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T. Minemoto (Ritsumeikan Univ.)
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K. Nishioka (Univ. of Miyazaki)
K. Ohdaira (JAIST)
I. Omura (Kyushu Inst. of Tech.)
G. Stokkan (Norwegian Univ.)

GENERAL INFORMATION

DATE

Conference: September 22-24, 2010 (Official language is English)
Short Course: September 21, 2010 (in English)

CONFERENCE VENUE

The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-0033, Japan
Phone +81-3-5841-6564 (from Sept. 21 to September 24)
http://www.u-tokyo.ac.jp/index_e.html
SSDM 2010 will be held at Hongo campus, the main campus of the University of Tokyo. The conference rooms are distributed over the campus. For details, see the campus map on the conference website and in Page 66 of this booklet.

Tokyo Dome Hotel
1-3-61 Koraku, Bunkyo-ku, Tokyo, 112-8562, Japan
Phone: +81-3-5805-2111 Fax: +81-3-5805-2200
http://www.tokyodome-hotels.co.jp/e/index.html
Special Plenary Session and Conference Reception will be held at Tokyo Dome Hotel. The hotel is located close to Korakuen station on Namboku line. This is the next station of Todaimae station. The access map from the University to the hotel is available on the conference web site and in Page 67.

TECHNICAL SESSIONS AND EVENTS

Oral and Poster Presentations:
The rooms for the technical sessions will be located in Faculty of Engineering Bldg. 2. The poster presentation will be held at Takeda Bldg., which is located in approximately 5 minutes walk from Faculty of Engineering Bldg. 2. See the campus map in Page 66.

Plenary Sessions:
Plenary Session and Special Plenary Session are scheduled on September 22. Plenary Session will be held at Yasuda Auditorium in The University of Tokyo after the opening session. Special Plenary Session "A Half Century of Esaki Diode and Lasers" will be held at Tenku in Tokyo Dome Hotel from 17:00 on the same day. Short abstracts for Plenary and Special Plenary Talks are shown in Page 11.

Conference Reception:
The conference reception will be held at Tokyo Dome Hotel on September 22, 18:30-20:00. The reception will start just after the Special Plenary Session in the next room. The reception is completely free of charge. Participants who register the conference are welcome to the reception. Drinks and appetizers will be served. During the reception, SSDM Young Researcher Award ceremony will be held.

Rump Sessions:
SSDM 2010 is organizing two Rump Sessions, which will be held on September 23, 18:30-20:00 at Sanjo Conference Hall, The University of Tokyo. Details can be found on Page 12.

Short Course:
On September 21, Short course lectures on “Si technology challenges in More Moore and More than Moore era” are arranged. When you are going to attend the course, you are requested to make a registration for short course, not for the conference itself. The scope and contents of the course are shown in Page 13.

Award Ceremony:
Award Ceremony for SSDM Award and SSDM Paper Award will be held in the opening session, which will start at 10:00AM on September 22 in Yasuda Auditorium.

Exhibition:
Exhibition will be held at the exhibition space on Forum, the 2nd floor of Faculty of Engineering Bldg. 2. For details, see Page 55.

REGISTRATION

All participants, who have registered through the conference website, are requested to stop by the registration desk to pick up your name card and congress kit. Please present your confirmation slip which will be e-mailed to you after your payment is confirmed. On-site registration is also available on the desk. The desk will be located on Forum, the 2nd floor of Faculty of Engineering Bldg. 2.
Open hours are as follows:

September 22	8:30-16:00
	16:00-18:10 in front of Room Tenku in Tokyo Dome Hotel (B1F)
September 23	8:30-17:00
September 24	8:30-15:30

SPECIAL ISSUE of JJAP

Authors of SSDM2010 papers are encouraged to submit their original papers to the Special Issue of Japanese Journal of Applied Physics which will be published in April 2011.

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate’s stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Tokyo is warm and sometimes humid in September. The temperature range is 18-30°C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo (conference site) and 60 Hz in western Japan including Kyoto and Osaka.

INTERNET ACCESS

Wireless internet access is available on the 1st and 2nd floor of the conference main site, Faculty of Engineering Bldg. 2. The following commercial connection services are available: BB mobile point (Softbank Telecom) http://tm.softbank.jp/wlan/index.html, Livedoor Wireless (Livedoor) http://wireless.livedoor.com/ In addition, complementary internet connection will be provided. Detailed information will be included in the congress kit.

PLENARY SESSION

September 22 (Wednesday) 10:30-12:00
Yasuda Auditorium, The University of Tokyo

10:30-11:15
"Nanotechnology for Sustainable Society"

Michiharu Nakamura
Director, Hitachi Ltd., Japan

The primary role of nanotechnology is to provide disruptive technologies for social sustainability and industrial revitalization. The theme of this presentation is to discuss the future direction of nanotechnology R&D in a global society. The rapid technological progress seen in the 20th century focused on higher performance and better functionality. This technology-push approach, however, is being re-examined since the critical state of global sustainability, resulting from modern industrialization and its accompanying lifestyles which are heavily dependent on massive consumption of natural resources, has been recognized. Society requires that these problems be solved through technology-based innovations such as "green" and "life" innovations; and it is exciting to imagine how we can resolve such social problems and reinforce industrial competitiveness with advanced nanotechnology R&D. We show that nanotechnology is playing key roles in the spiral cycles of green innovation and life innovation, and that comprehensive approaches including technology development, device feasibility study, system prototyping, and human resource development are crucial in terms of achieving nanotechnology–based innovations. Collaborative R&D centers represented by TIA-nano in Tsukuba will accelerate such activities in Japan. Collaborative efforts between academia, independent R&D institutes, and industry *under one roof* will overcome organizational constraints and work better for technology development, education, and achieving social goals.

11:15-12:00
"More Moore and More Than Moore meeting for 3D in the 21th century"

Simon Deleonibus
Research Director, CEA-LETI, France

Co-integrating More than Moore devices with CMOS to interface the outside Multiphysics world brings Functional Diversification. 3D integration will address at wafer level device to packaging technologies capable to reduce cost and improve system performance.
Nanoelectronics linear scaling appeals new 3D integration schemes in order to continue Moore's law. Unique opportunities exist to increase the devices performances, system complexity and reduce power consumption of mobile, handheld objects. Also new design and functional architectures will be possible by mixing logic and memory devices to save power consumption and introduce new applications by using neuromorphic or bio inspired approaches. Devices other than CMOS can be co-integrated with CMOS to interface the outside Multiphysics world (MEMS, sensors and actuators, RF devices, power devices,…) allowing new functionalities. 3D Wafer Level Packaging and System on a Wafer allow these new routes.
Functional diversification added to Nanoelectronics will make possible new future systems to address increasing societal needs. 3D integration will address, at the wafer level, device to packaging technologies capable of reducing cost and improving system performance.

SPECIAL PLENARY SESSION
"A Half Century of Esaki Diode and Lasers"

September 22 (Wednesday) 17:00-18:30
Tenku, Tokyo Dome Hotel

17:00-17:45
"50 Years of the Lasers"

Koichi Shimoda
Professor Emeritus, The University of Tokyo, Japan

Invention of the maser by C. H. Townes in 1954 opened the door for generation of coherent electromagnetic wave at higher frequencies than that could be obtained with electronic devices. Competitive research for infrared and optical masers resulted in the achievement of the laser in 1960.
Pulsed laser action in ruby was first observed by T. H. Maiman on May 16, 1960. Then the cw operation of He-Ne laser was achieved by A. Javan and his collaborators on December 12, 1960. They were followed by evolution of a variety of solid-state lasers, gas lasers, semiconductor lasers, liquid lasers, short pulse lasers, as well as laser theories and laser applications. A high-power laser system may now deliver a peak power of multi-peta watts, while nano-laser may generate single photons.
Recent development of new lasers is not restricted by the resonance of atoms and molecules, but by artificial structures. Thus tunable lasers operating in a wide spectral range are being developed. Quantum-dot lasers on the one hand and X-ray free electron lasers on the other hand are now under active investigation.

17:45-18:30
"In Half a Century of Research Career, What Did I Explore?"

Leo Esaki
President, Yokohama College of Pharmacy Chairman, The Science and Technology Promotion Foundation of Ibaraki, Japan

In 1945-46, we physics students were really fascinated by the introduction of the revolutionary knowledge of "Quantum Mechanics" which had not yet been widely disseminated. I was interested in putting the new knowledge of quantum mechanics to practical use.
In 1956, I initiated the investigation of the quantum mechanical tunneling in narrow Ge p-n junctions at SONY, Tokyo. We first obtained a backward diode. When the junction width narrowed down to about 10 nanometers, the current-flow mechanism was convincingly tunneling not only in the reverse direction but also in the low-voltage range of the forward direction, giving rise to a prominent current-peak. Since the current-peak associated with a negative resistance had never been predicted, the Esaki Tunnel diode - the very first quantum electron device - came as a total surprise in 1957.
In 1969, Esaki and Tsu at IBM T.J. Watson Research Center, New York, proposed a semiconductor superlattice, a "man-made periodic quantum structure" which is engineered by applying the advanced growth technique of MBE, after designing the periodic structure in accordance with the principles of quantum theory in such a way as to exhibit unprecedented electronic properties.
Esaki and his coworkers' pioneering research on superlattices and quantum wells in the 1970s and 1980s triggered a wide spectrum of experimental and theoretical investigations resulting in not only the observation of a number of intriguing phenomena, but also the emergence of a new class of transport and optoelectronic devices.

RUMP SESSIONS

September 23 (Thursday) 18:30-20:00
Sanjo Conference Hall, The University of Tokyo

Session A (1st Floor)

"Will Carbon Create A New ICT Paradigm Beyond The Silicon Establishments?"

CNT and recently graphene have been attracting a considerable research interest even in Si community, though only high mobility or migration robustness will not reroute the way to step aside from the red brick wall. So, questions are, whether or not, (i) we will be able to muddle through the present Si research blockade by welcoming a new friend, Mr. Carbon (a tough negotiator), (ii) carbon will really challenge to silicon giant by him/herself (Don Quixote), or (iii) carbon will create application frontiers Si tech has not been so far interested in (a western cowboy). This rump session will discuss challenges (optimistically) and opportunities (positively) of "carbon" for something new from above standpoint. Join our rump session just for a fun as well as for catching some for further Si tech advancement.

Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of. Tokyo)
M. Nihei (AIST)

Panelists: A. A. Balandin (UC Riverside)
B. H. Hong (Sungkyunkwan Univ.)
T. Otsuji (Tohoku Univ.)
K. Wakabayashi (NIMS)
J. C. S. Woo (UCLA)

Session B (Basement Floor)

"Silicon Solar Cells - Their key technologies and future prospects - "

The era of solar energy is coming. Solar cells show a bright future as a clean and inexhaustible electric power source. Their production level has expanded more than 10 GW, and approximately 85% shipped solar cells were crystal and poly-crystal silicon solar cells in 2009. In this rump session, we will discuss the key technologies of silicon solar cells and foresee their future.

Organizer: T. Fukui (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech)
A. Masuda (AIST)

Panelists: M. Konagai (Tokyo Tech)
T. Sameshima (Tokyo Univ. of Agri. & Tech.)
N. Usami (Tohoku Univ.)
I. Sakata (AIST)

SHORT COURSE

September 21 (Tuesday) 11:00-17:30
Room 241, Faculty of Engineering Bldg.2, 4F, Hongo Campus, The University of Tokyo

“Si technology challenges in More Moore and More than Moore era”

Organizers: D. Hisamoto (Hitachi, Ltd.) / K. Ohashi (NEC)
*All lectures are given in English.

ULSI technology has been flourished for over 40 years in line with Moore’s Law, today, however, advanced technologies which can take us beyond the Law (more Moore) or superior technologies (more than Moore) are urgently being pursued. In this short course, the outlook for Si technology challenges today and in the future with regard to the above situation will be presented by spirited tutors from academia and industry. To raise interest and inspire students and young researchers, the issues will be explained from basic theoretical and practical points of view.

11:00-12:00 Overview of Si challenges
A Toriumi, Univ. of Tokyo

(12:00-13:00 Lunch)

13:00-13:50 Advanced CMOS Technology － Continuing challenges to keep Moore's Law －
K. Ishimaru, Toshiba America Electronic Components Inc.

13:50-14:40 Carrier Transport in Advanced CMOS Transistors
N. Mori, Osaka University

14:40-15:30 Electric property fluctuation in deca- nanometer scale MOSFET caused by single electron capture and emission
R. Yamada, Hitachi, Ltd.

(15:30-15:50 Break)

15:50-16:40 Si Photonics
K. Wada, Univ. of Tokyo

16:40-17:30 Surface MEMS
H. Toshiyoshi, Univ. of Tokyo

TECHNICAL PROGRAM

Wednesday, September 22

Opening & Plenary Sessions (Yasuda Auditorium)

Opening Session (10:00-10:30)
Chair: S. Takagi, Univ. of Tokyo

10:00
Welcome Address
Y. Arakawa, Univ. of Tokyo

Award Ceremony

Plenary Sessions (10:30-12:00)
Chair: K. Masu, Tokyo Tech

10:30 PL-1-1
Nanotechnology for Sustainable Society
M. Nakamura, Hitachi Ltd., Japan

The primary role of nanotechnology is to provide disruptive technologies for social sustainability and industrial revitalization. The theme of this presentation is to discuss the future direction of nanotechnology R&D in a global society.

11:15 PL-1-2
More Moore and More Than Moore meeting for 3D in the 21st century
S. Deleonibus, CEA-LETI, France

Co-integrating More than Moore devices with CMOS to interface the outside Multiphysics world brings Functional Diversification. 3D integration will address at wafer level device to packaging technologies capable to reduce cost and improve system performance.

12:00-13:00 Lunch

1F 211

A-1: Organic Device Physics (Area 10)
(13:00-14:15)
Chairs: T. Shimada (Hokkaido Univ.)
M. Nakamura (Chiba Univ.)

13:00 A-1-1 (Invited)
Electronic Structures and Electric Properties of Rubrene Single Crystal Studied By Photoemission, Time-of-Flight, and Displacement Current Measurements
H. Ishii, Chiba Univ. (Japan)
Rubrene single crystal has attracted much attention because it has the highest hole mobility of organic semiconductors so far reported. By overcoming charging problem by laser irradiation, we have succeeded to directly observe the band-dispersion relation. On the basis of the photoemission results as well as time-of-flight mobility measurement, the carrier transport mechanism will be discussed.

13:30 A-1-2
Carrier Propagation Dependence on Applied Potentials in Pentacene OFET Investigated by Impedance Spectroscopy and Electrical Time-of-Flight Techniques
J. Lin[1], M. Weis[2], D. Taguchi[1], T. Manaka[1] and M. Iwamoto[1], [1]Tokyo Tech and [2]Slovak Aca. Sci (Japan)
Impedance spectroscopy and electrical time-of-flight techniques were used for the evaluation of carrier propagation dependence on various applied potentials in a pentacene OFET. These techniques are based on carrier propagation, thus isolates the effect of charge density. The results agree well with our developed model.

1F 212

B-1: Ge MOS Technology 1 (Area 1)
(13:00-14:10)
Chairs: J. Yugami (Renesas Electronics Corp.)
O. Nakatsuka (Nagoya Univ.)

13:00 B-1-1 (Invited)
Defect-Free GOI (Ge on Insulator) by SiGe Mixing-Triggered Liquid-Phase Epitaxy
M. Miyao[1], K. Toko[1,2], M. Kurosawa[1,2] and T. Sadoh[1,2], [1]Kyushu Univ. and [2]JSPS (Japan)
The present paper reviews our recent progress in the novel GOI growth technique. Following subjects will be discussed: (1) Basic idea for SiGe mixing-triggered rapid melting growth, (2) Defect-free giant GOI (~1 cm length) with high carrier mobility (~ 1200 cm2/Vs), (3) Possible application to 3D-LSI, thin film transistors, and spin-transistors.

13:30 B-1-2
Advantage of High-pressure Oxidation for Ge/GeO_2 Stack Formation
C. H. Lee[1], T. Nishimura[1,2], T. Tabata[1], S. Wang[1], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
The PDA for Ge/GeO2 stack has been systematically investigated, and it has been revealed that LOA is quite important for passivating Ge/GeO2 interface. However, GeO2 bulk properties are different between APO- and HPO-grown GeO2 films.

1F 213

C-1: Low Frequency Noise (Area 3)
(13:00-14:20)
Chairs: T. Hiramoto (Univ. of Tokyo)
T. Tanaka (Fujitsu Semiconductor Ltd.)

13:00 C-1-1
Contributions of Interface-Trap and Minority-Carrier Responses to C-V characteristics of Al_2O_3/InGaAs Capacitors
Y. Urabe[1], N. Miyata[1], T. Yasuda[1], H. Yamada[2], M. Hata[2], N. Taoka[3], T. Hoshii[3], M. Takenaka[3] and S. Takagi[3], [1]AIST, [2]Sumitomo Chemical Co., Ltd. and [3]Univ. of Tokyo (Japan)
We clarified the contribution of minority-carrier response to the C-V and conductance characteristics of ALD-Al_2O_3/InGaAs MIS capacitor using the temperature-dependent measurement. As a result, we found that the *Gp/ω* ridge structure measured at -50°C is mainly composed of the interface-trap responses.

13:20 C-1-2
New Insights into Flicker Noise Improvement Mechanism Using Random Telegraph Signal Technique
T. L. Li, S. Y. Huang, B. Hung, C. Y. Tzeng and S. Chou, United Microelectronics Corp. (Taiwan)
This work demonstrated that the improvement of low-frequency noise using F-incorporation and H2-sintering can be attributed to the relaxed trap-to-carrier influence and reduced trap density, respectively.

2F 221

D-1: Nonlinear Optics (Area 7)
(13:00-14:15)
Chairs: K. Akiyama (Mitsubishi Electric Corp.)
H. Yamada (Tohoku Univ.)

13:00 D-1-1 (Invited)
Roadmap of ultrafast energy-saving optical semiconductor devices to Year 2025
Y. Ueno, Univ. of Electro-Communications (Japan)
Evolution in energy efficiency of many-core parallel processors through year 2025 looks unclear, because the serial speed of new electronic cores has stopped to evolve. With reviewing application-research activities in opto-electronics, instead, the author estimates what possibilities the still-crude 100-times-faster serial processors (e.g. 200-Gb/s) will contribute through year 2025.

13:30 D-1-2
Quasi-Phase-Matched Difference Frequency Generation at 3.4 μm in High-Quality GaAs/AlGaAs Waveguides
K. Hanashima, I. Ohta, J. Ota, T. Matsushita and T. Kondo, Univ. of Tokyo (Japan)
We have succeeded in fabricating high-quality periodically-inverted GaAs/AlGaAs waveguides, and achieved the lowest propagation loss ever reported and reasonable high efficiency in quasi-phase matched difference frequency generation at 3.4 μm.

4F 241

E-1: DRAM (Area 4)
(13:00-14:20)
Chairs: K. Hamada (Elpida Memory, Inc.)
S. Miura (NEC Corp.)

13:00 E-1-1
Performance Improvement of a Novel Capacitor-less 1T-DRAM Based on a Lateral p Type Doped Region
G. Guegan[1], G. Molas[1], S. Puget[2] and C. Raynaud[1], [1]CEA-LETI/MINATEC and [2]STMicroelectronics (France)
A novel architecture is proposed on a standard PD-SOI in order to facilitate the formation of a deep body potential. This new device with significant memory performance improvement, is a promising candidate for future embedded 1T-DRAM.

13:20 E-1-2
Characterization of junctionless Z-RAM cell
C. W. Lee[1], S. Okhonin[2], M. Nagoya[2], A. Kranti[1], I. Ferain[1], N. Dehdashti Akhavan[1], P. Razavi[1], R. Yu[1], R. Yan[1] and J. P. Colinge[1], [1]Tyndall National Inst. and [2]Innovative Silicon (Ireland)
We fabricated the silicon nanowire JunctionLess(JL) proposed for capacitorless 1T DRAM. The JL-MuGFET has more advantage such as a very low leakage current, a low turn-on voltage, extremely easy processing. We believe that this JL based Z-RAM memory will use in sub-nano scale regime.

4F 242

F-1: Graphene Structures and Transport (Area 9)
(13:00-14:15)
Chairs: T. Machida (Univ. of Tokyo)
Y. Kawano (RIKEN)

13:00 F-1-1 (Invited)
STS Observations of Topological Dirac Fermion on Graphite Surafaces
T. Matsui, K. Tagami, M. Tsukada and H. Fukuyama, [1]Univ. of Tokyo and [2]Advanced Coropration (Japan)
Surface states of graphite in magnetic field were studied both theoretically and experimentally with scanning tunneling spectroscopy to show that the property of massless Dirac fermion in Graphene is appeared on graphite surfaces.

13:30 F-1-2 (Invited)
Electronic Transport Properties in Graphene Nanoribbons and Junctions
K. Wakabayashi[1,2], [1]NIMS and [2]PRESTO, JST (Japan)
We focus theoretically on the electronic transport properties of graphene nanoribbons and nanojunctions. The presence of a perfectly conducting channel in disordered graphene nanoribbons is pointed out. Nanojunctions are shown to have the zero-conductance anti-resoances associated with the edge states. The condition of the resonances is discussed.

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12:00-13:00 Lunch

4F 243

G-1: RF Circuits and Systems (1) (Area 5)
(13:00-14:10)
Chairs: M. Ikebe (Hokkaido Univ.)
H. Takao (Kagawa Univ.)

13:00 G-1-1 (Invited)
Evolution of Transceiver Architectures toward Software-Defined and Cognitive Radios
T. Tsukahara, T. Tsushima and H. Ito, Univ. of Aizu (Japan)
The evolution of CMOS transceiver architectures is described, especially focusing on SDR and CR applications. After explaining some examples of transceiver designs, we propose a high-precision complex quadrature modulator suitable for SDR and CR transmitters. It features an inherent correction mechanism of phase and amplitude errors.

13:30 G-1-2
A 6-10 GHz CMOS Tunable Power Amplifier for Reconfigurable RF Transceivers
J. Y. Hong, D. Imanishi, K. Okada and A. Matsuzawa, Tokyo Tech (Japan)
A CMOS power amplifier with a tunable output impedance matching is proposed for a multi-standard transceiver that operates at frequency band from 6 to 10GHz. The output 1-dB compression point, saturated output power and maximum PAE are larger than 15.5.dBm, 19.8dBm and 7.1%, respectively.

4F 244

H-1: New Functional Materials (Area 8)
(13:00-14:15)
Chairs: H. Hibino (NTT Basic Res. Labs.)
B. H. Hong (Korea Univ.)

13:00 H-1-1 (Invited)
Let us update the present status of research on magnetic semiconductors
H. Munekata, Tokyo Tech (Japan)
Present status at to research on III-V-based, oxide-based, and group-IV based magnetic semiconductors will be discussed, together with potential, future applications which may not be restricted within the limit of devices for electrical computers.

13:30 H-1-2
In situ Observation of Fe growth on GaAs(001) and InAs(001) by X-ray diffraction
S. Fujikawa and M. Takahasi, JAEA (Japan)
We evaluated Fe films on GaAs(001) and InAs(001) by in-situ X-ray diffraction measurements with increasing Fe thickness. While the Fe/InAs was strained even at 30 ML, Fe/GaAs was already relaxed at 4 ML.

4F 245

I-1: III-V High-Speed and High-FrequencyTransistors (Area 6)
(13:00-14:15)
Chairs: S. Tanaka (Shibaura Inst. of Tech.)
S. Yamahata (NTT Corp.)

13:00 I-1-1 (Invited)
Adding Value to CMOS through Heterogeneous Integration
Y. Royter, P. R.. Patterson, J. C. Li, K. R. Elliot, T. Hussain, M. F. Boag-O'Brien, J. R. Duvall, M. C. Montes, D. A. Hitko, M. Sokolich, D. H. Chow and P. D. Brewer, HRL Laboratories, LLC (USA)
Technology capable of wafer-scale device-level integration of InP HBTs and CMOS has been developed, making full simultaneous utilization of III-V device speed and CMOS circuit complexity possible. Resulting circuits maintain maximum CMOS integration density and HBT performance without significant CMOS or HBT degradation, and produce high yield heterogeneous interconnects with < 5um length.

13:30 I-1-2
InP/InGaAs MOSFET with Back-Electrode Structure Bonded on Si Substrate Using a BCB Adhesive Layer
T. Kanazawa, R. Terao, Y. Yamaguchi, S. Ikeda, Y. Yanai and Y. Miyamoto, Tokyo Tech (Japan)
We demonstrated InP/InGaAs/InP channel MOSFET with a back-metal gate on Si using the BCB bonding. In the I-V measurement with dual-gate operation, the drain current of 880 mA/mm and transconductance of 450 mS/mm were achieved.

4F 246

J-1: Carbon Nanotube Devices (Area 13)
(13:00-14:15)
Chairs: Y. Ohno (Nagoya Univ.)
S. Suzuki (NTT Corp.)

13:00 J-1-1 (Invited)
Synthesis and dry depositon of SWCNT networks for flexible, transparent conductors and field effect transistors
A. Kaskela[1], A. G. Nashibulin[1], M. Y, Zavodchikova[1], B. Aitchison[2], Y. Tian[1], Z. Zhu[1], H. Jiang[1], D. P. Brown[2] and E. I. Kauppinen[1], [1]Aalto University and [2]Canatu Oy (FINLAND)
We present the floating Fe catalyst synthesis of high quality SWCNTs from CO. Methods for SWCNT dry deposition onto polymeric substrates at ambient temperature to manufacture transparent thin film FETs and conducting films are discussed.

13:30 J-1-2
Characterization of Carbon Nanotube Thin Film Transistors by Scanning Probe Microscopy
Y. Okigawa, Y. Ohno, S. Kishimoto and T. Mizutani, Nagoya Univ. (Japan)
We measured carbon nanotube (CNT) - thin-film transistors in detail by Kelvin probe force microscopy, point-contact current-imaging AFM, and scanning gate microscopy. Non uniform images which correlated each other ware obtained even in the randomly- oriented 2D networks of CNTs.

2F 222

K-1: Modeling of Power LDMOSFET (Area 14)
(13:30-14:00)
Chairs: T. S. Chow
(Rensselaer Polytechnic Institute)
M. Ishiko (Toyota Central R&D Labs., Inc.)

13:45 K-1-2
Modeling of RESURF LDMOS for Accurate Prediction of Junction Condition on Device Characteristics
T. Saito[1,2], T. Tanaka[1], T. Hayashi, K. Kikuchihara, T. Kanamoto, [2]H. Masuda, M. Miyake, [1]S. Amakawa, H. J. Mattausch and M. Miura-Mattausch, [1]Renesas Electronics Corp. and [2]Hiroshima Univ. (Japan)
The compact model for high-voltage MOSFETs HiSIM_HV was extended to RESURF structure. The model considers the influence of the dynamically varying depletion width at the drain/substrate junction, causing the resistance modification and the expansion effect of impact ionization.

2F 223

L-1: Biosensors (Area 11)
(13:00-14:15)
Chairs: K. Ajito (NTT Corp.)
S. Contera (Univ. of Oxford)

13:00 L-1-1 (Invited)
Detection of biomolecular recognition using Bio-transistors
Y. Miyahara, C. Hamai-Kataoka, A. Matsumoto T. Goda and Y. Maeda, NIMS (Japan)
We have been investigating direct interaction between biomolecular charges and charged carriers in semiconductor materials. Field effect transistors have been used to detect biomolecular recognition based on electrostatic interaction. The platform based on the bio-transistors is suitable for a simple and inexpensive system for clinical research and diagnostics.

13:30 L-1-2
Sensitivity Improvement of Biosensors Using Si Ring Optical Resonators
M. Fukuyama, Y. Amemiya, Y. Abe, Y. Onishi, A. Hirowatari, K. Terao, T. Ikeda, A. Kuroda and S. Yokoyama, Hiroshima Univ. (Japan)
The sensitivity of antigen detection using Si ring optical resonators is found to be in the order of 10-6 g/ml. Using the variety of approach it was suggested that the sensitivity of the biosensor will be improved by factor of 100. Then the practical Si ring biosensor will be realized.

Wednesday, September 22

1F 211

A-1: Organic Device Physics (Area 10)

13:45 A-1-3
Transient Absorption Decay Characteristics at Visible Wavelength Region for NMe_2-Silole:Fluorene Blend Film
T. Fukuda[1], A. Furube[2], R. Kobayashi[1], N. Kamata[1] and K. Hatano[1], [1]Saitama Univ. and [2]AIST (Japan)
We investigated charge carrier dynamics in a silole doped F8BT blend film by measuring transient absorption decay at a visible wavelength region. The transient absorption characteristics are useful to understand carrier dynamics in organic material, and they were measured by femtosecond pump-probe technique.

14:00 A-1-4
Computational Analysis of Electron Injection on Light-Emitting Polymer/Cathode Interface
I. Yamashita, H. Onuma, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
We simulated the electron injection on the light-emitting polymer/cathode interface by using a quantum chemistry calculation and Monte Carlo method. We investigated the relationship between structure of the interface and electron injection properties.

1F 212

B-1: Ge MOS Technolosy 1 (Area 1)

13:50 B-1-3
Nature of Interface Traps in Ge MIS Structures with GeO_2 Interfacial Layers
N. Taoka[1], W. Mizubayashi[1], Y. Morita[1], S. Migita[1], H. Ota[1] and S. Takagi[1,2], [1]MIRAI-NIRC and [2]Univ. of Tokyo (Japan)
Ge MIS interface properties with GeO2 interfacial layers have been systematically investigated. It is found that the natures of the interface traps depend on oxidation temperatures, and that acceptor-like traps are widely distributed in bandgap.

1F 213

C-1: Low Frequency Noise (Area 3)

13:40 C-1-3
Drastic reduction of the low frequency noise in Si(100) p-MOSFETs
P. Gaubert, A. Teramoto, R. Kuroda, Y. Nakao, H. Tanaka and T. Ohmi, Tohoku Univ. (Japan)
On the account of new fabrication processes, we demonstrate in this paper that very efficient ways for reducing the 1/f noise in MOSFETs have been achieved. Moreover, a drop down to almost 4 decades can be expected regarding the Si(100) p-MOSFETs.

14:00 C-1-4
Layout Dependent STI Stress Effect on High Frequency Performance and Flicker Noise in Nanoscale CMOS Devices
K. L. Yeh, C. Y. Ku and J. C. Guo, National Chiao Tung Univ. (Taiwan)
The impact of MOSFET layout dependent stress on high frequency performance and flicker noise is investigated. Donut MOSFETs, attributed to the suppression of STI transverse stress and excess traps can realize the lowest flicker noise and improved f_1.

2F 221

D-1: Nonlinear Optics (Area 7)

13:45 D-1-3
Experimental Observation of Self-Phase Modulation in ZnO Channel Waveguides
E. Y. Morales Teraoka[1], D. H. Broaddus[2], T. Kita[1], A. Tsukazaki[1,3], M. Kawasaki[1,3,4], A. L. Gaeta[2] and H. Yamada[1], [1]Tohoku Univ., [2]Cornell Univ., [3]PRESTO, Japan Science and Technology Agency, [4]WPI Advanced Institute for Materials Research and [5]CRESTO, Japan Science and Technology Agency (Japan)
We demonstrate spectral broadening of femtosecond pulses due to SPM in the fabricated ZnO waveguides. Using the obtained measurements, we estimate the nonlinear strength parameter and the nonlinear refractive index.

14:00 D-1-4
Remarkable Enhancement of Optical Kerr Signal by increasing Quality Factor in a GaAs/AlAs Multilayer Cavity
K. Morita, T. Takahashi, T. Kitada and T. Isu, Univ. of Tokushima (Japan)
The spectral widths of the laser pulses were tuned to the cavity modes and the Q dependent optical Kerr signal was investigated using GaAs/AlAs multilayer cavity structure. We have revealed that the optical Kerr signal was remarkably enhanced by Q (proportional to Q4) in our cavity.

4F 241

E-1: DRAM (Area 4)
(13:00-14:20)

13:40 E-1-3
A Study of a Data Retention Characteristic for Various Schemes of Gate Oxide Formation in Sub-50-nm Saddle-Fin Transistor DRAM Technology
S. W. Ryu, S. K. Chun, T. Jang, B. Lee, D. Lee, M. Yoo, S. Cha, J. G. Jeong and S. J. Hong, Hynix Semiconductor Inc. (Korea)
A data retention characteristic has been investigated for different gate oxide formation schemes with saddle-Fin transistor DRAM. It was confirmed that the Interface traps by charge pumping method strongly affected the data retention time.

14:00 E-1-4
An analysis of Conduction Mechanism and Reliability Characteristics of MIM Capacitor with Single ZrO_2 Layer
H. M. Kwon[1], I. S. Han[1], S. U. Park[1], J. D. Bok[1], Y. J. Jung[1], H. S. Shin[1], C. Y. Kang[2], B. H. Lee[3], R. Jammy[2] and H. D. Lee[1], [1]Chungnam National Univ., [2]SEMATECH and [3]GIST (Korea)
In this paper, current transport mechanism and reliability of MIM capacitor with single zirconium oxide layer are characterized in depth.

4F 242

F-1: Graphene Structures and Transport (Area 9)

14:00 F-1-3
Field-Effect in Multiple Graphene Layer Structures
M. Ryzhii[1,3], T. Otsuji[2,3], V. Mitin[4], M. S. Shur[5] and V. Ryzhii[1,3], [1]Univ. of Aizu, [2]Tohoku Univ., [3]J. Sci. Technol. Agency, [4]Univ. at Buffalo and [5]Rensselaer Polytech. Inst. (Japan)
The field effect in gated multiple-graphene layer structures is studied. The distributions of the potential, Fermi energy, and electron density over the graphene layers are calculated.

Coffee Break (2F Forum)

1F 211

A-2: Electric Characterization of Organic Semiconductors (Area 10)
(14:45-15:45)
Chairs: M. Yoshida (AIST)
E. Itoh (Shinshu Univ.)

14:45 A-2-1 (Invited)
Non-Contact Measurement of Charge Carrier Mobility in Inorganic and Organic Semiconductor Materials
S. Seki[1,2], A. Asano, Y. Honsho[1] and A. Saeki[1,2], [1]Osaka Univ. and [2]PRESTO, JST (Japan)
Intrinsic charge carrier mobility in inorganic and organic semiconductor materials is determined by non-contact microwave measurement technique as the short-range transport properties of charge carriers, and discussed in relation to the values by several conventional techniques.

15:15 A-2-2
Probing of Transient Electric Field Distribution in ITO/PI/P3HT/Au Using Time-Resolved Second Harmonic Generation Measurement
R. Miyazawa, D. Taguchi, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
The discovery of highly conducting organic materials, e.g., pentacene, polythiophene, etc. has resulted in studies of their possible application to organic electronics devices, such as organic electroluminescent devices (OLEDs), organic solar cells and organic field-effect transistors (OFETs).

1F 212

B-2: Ge MOS Technology 2 (Area 1)
(14:45-16:05)
Chairs: S. Miyazaki (Nagoya Univ.)
T. Nabatame (NIMS)

14:45 B-2-1
Effects of GeO_2-Metal Interaction on V_{FB} of GeO^2 MIS Gate Stacks
F. I. Alzakia[1], K. Kita[1,2], T. Nishimura[1,2], k. Nagashio[1,2] and A. ToriumiToriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
The flatband voltages (VFB) of GeO2 gate stacks with various metals have been investigated. The metal-GeO2 interaction, which is pronounced for high work function metals, significantly affects the VFB of GeO2 MIS stacks.

15:05 B-2-2
Single-Crystalline (100) Ge Stripes with High Mobilities Formed on Insulating Substrates by Rapid-Melting-Growth with Artificial Single-Crystal Si Seeds
K. Toko, T. Sakane, H. Yokoyama, M. Kurosawa, T. Sadoh and M. Miyao, Kyushu Univ. (Japan)
Orientations of single-crystal Ge stripes are controlled to (100) planes on insulating substrates by SiGe-mixing triggered melting-growth combined with the Si (100) micro-seed technique. In addition, defect-free Ge with the high hole mobility is demonstrated.

1F 213

C-2: Transport Physics (Area 3)
(14:45-16:05)
Chairs: Y. Nishida (Renesas Electronics Corp.)
N. Mori (Osaka Univ.)

14:45 C-2-1
Abrupt Source Heterostructures with Lateral-Relaxed/Strained Layers for Quasi-Ballistic CMOS Transistors using Lateral Strain Control Technique of Strained Substrates
T. Mizuno[1,2], M. Hasegawa[1], K. Ikeda[3], M. Nojiri[4] and T. Horikawa[2], [1]Kanagawa Univ., [2]MIRAI-NIRC, [3]MIRAI-Toshiba and [4]AIST (Japan)
We have experimentally studied abrupt source relaxed-/strained-layers heterojunction structures for quasi-ballistic CMOS, by a local O+ ion implantation induced relaxation technique of strained substrates with SiO2 mask patterns.

15:05 C-2-2
Impact of Transistor Layout Configuration on Current Drive Performance in (100)/<110> and (100)/<100> SiGe channel pMOSFETs: Comparative Study to Si channel
K. Nakatsuka, H. Okamoto, H. Itokawa, K. Okano, T. Izumida, M. Kondo, T. Morooka, I. Mizushima, A. Azuma, N. Aoki, S. Inaba and Y. Toyoshima, Toshiba Corp. (Japan)
We systematically studied the mobility modulation by transistor layout configuration in Si and SiGe channel pMOSFETs, and found that hole mobility in <100>/(100) channel SiGe is the highest in short and narrow channel pMOSFETs.

2F 221

D-2: Advanced Design and Measurement (Area 7)
(14:45-15:45)
Chairs: H. Yamada (Tohoku Univ.)
K. Akiyama (Mitsubishi Electric Corp.)

14:45 D-2-1
Time-Resolved Measurements on Sum Frequency Generation Strongly Enhanced in (113)B GaAs/AlAs Coupled Multilayer Cavity
F. Tanaka, T. Takimoto, K. Morita, T. Kitada and T. Isu, Univ. of Tokushima (Japan)
In this study, strong SFG from the (113)B coupled multilayer cavity was confirmed to originate from the interference between the enhanced internal light electric fields of the cavity modes by time-resolved measurements.

15:00 D-2-2
Development of half-cladding semiconductor photonic device structure for surface transmission of light waves
N. Yamamoto[1], D. Murakami[2], H. Fujioka[2], K. Akahane[1], T. Kawanishi, H. Sotobayashi[3] and H. Takai[2], [1]NICT, [2]Tokyo Denki Univ. and [3]Aoyama Gakuin Univ. (Japan)
We propose a half-cladding semiconductor laser (HaCL) structure to achieve a surface transmission of light-waves in the novel photonic device. A light emission from the fabricated HaCL structure is successfully demonstrated under the current injection.

4F 241

E-2: Flash Memory Ⅰ (Area 4)
(14:45-16:05)
Chairs: T. Endoh (Tohoku University)
E. Yang (eMemory Technology Inc.)

14:45 E-2-1
Improvement of Data Retention in NAND Flash Memory for beyond 3x nm using HTO Liner and IPD Thickness Optimization
J. S. Leem, J. Seo, B. K. Kim, K. S. Kim, H. H. Chang, K. O. Ahn, S. K. Lee and S. J. Hong, Hynix Semiconductor Inc. (Korea)
In this paper, we present our results on how to improve reliability with optimizing mechanical stress in active and interpoly dielectrics thickness, and confirmed the results through various simulations and test methods on 41nm NAND technology.

4F 242

F-2: Novel Structures (Area 9)
(14:45-16:00)
Chairs: T. Matsui (Univ. of Tokyo)
K. Wakabayashi (NIMS)

14:45 F-2-1
Piezoelectric control of coupled vibration in elastically coupled nanomechanical oscillators
H. Okamoto[1], C. Y. Chang[1,2], K. Onomitsu[1], E. Y. Chang[2] and H. Yamaguchi[1], [1]NTT Basic Res. Labs. and [2]National Chiao Tung Univ. (Japan)
We have demonstrated all-piezoelectric operation of coupled nanomechanical oscillators at room temperature. We will be able to use the piezoelectric control of coupled vibration for applications of coupled nanomechanical oscillators, such as highly sensitive sensors.

15:00 F-2-2
Ge nanowires for nanoscale nonvolatile memory applications
S. Maikap[1], S. Majumdar[1,2], W. Banerjee[1], S. Mondal[1], S. Manna[2] and S. K. Ray[2], [1]Chang Gung Univ. and [2]Indian Institute of Technology, Kharagpur (Taiwan)
The Ge nanowires are prepared by VLS method. A broad peak in photoluminescence spectrum is due to germanium-oxygen vacancies. Good flash and resistive memory devices are obtained using Ge nanowire MOS structure for the first time.

Wednesday, September 22

4F 243

G-1: RF Circuits and systems (1) (Area 5)

13:50 G-1-3
RF Signal Generator Based on Time-to-Analog Converter Using Multi-Ring Oscillators in 90nm CMOS
K. Nakano, S. Amakawa, N. Ishihara and K. Masu, Tokyo Tech (Japan)
In this paper, a scalable wideband RF signal generator that uses a time-to-analog conversion technique using multi-ring oscillators is proposed and confirmed by fabricating a chip using 90nm CMOS.

4F 244

H-1: New Functional Materials (Area 8)

13:45 H-1-3
Luminescence Characteristics and Annealing Effect of Tb-doped AlBNO Films for Inorganic Electroluminescence Devices
K. Masumoto[1], A. Semba[1], C. Kimura[1], T. Taniguchi[2], K. Watanabe[2] and H. Aoki[1], [1]Osaka Univ. and [2]National Inst. for Materials Sci. (Japan)
Inorganic electroluminescence devices have attracted attention owing to their application in low-power-consumption displays. However, the operating voltage is very high. To lower the operating voltage, we have investigated Tb-doped AlBNO films as the luminescence layer.

14:00 H-1-4
Influence of Nitrogen Doping on the LaAlO Film Properties
M. Honjo, N. Komatsu, C. Kimura and H. Aoki, Osaka Univ. (Japan)
We have investigated the influence on the electrical and optical properties of the LaAlON (N: 0-4%) films of nitrogen doping as a way of improving the water resistance.

4F 245

I-1: III-V High-Speed and High-Frequency Transistors (Area 6)

13:45 I-1-3
Source/Drain Engineering for $In_{0.7}Ga_{0.3}As$ N-MOSFETs: Raised Source/Drain with *In Situ* Doping for Series Resistance Reduction
X. Gong[1], H.C. Chin[1], S.M. Koh[1], L. Wang[1], Ivana[1], Z. Zhu[1], B. Wang[2], C.K. Chia[2] and Y.C. Yeo[1], [1]National Univ. of Singapore and [2]Inst. of Materials Res. and Engineering, Agency for Sci. Tech. and Res. (Singapore)
We report the first demonstration of $In_{0.7}Ga_{0.3}As$ N-MOSFETs with in situ doped raised source/drain (S/D) regions. By using the new S/D architecture, a ~30% reduction in series resistance Rs can be obtained, leading to enhancement in I_{Dsat} of the $In_{0.7}Ga_{0.3}As$ N-MOSFETs.

14:00 I-1-4
A sub 350°C GaSb pMOSFET with ALD high-k dielectric
A. Nainani, T. Irisawa, Y. Sun, F. Crnogorac and K. Saraswat, Stanford Univ. (USA)
Bandgap & offsets for ALD Al_2O_3 on GaSb are calculated using SRPES. Interface characteristics are investigated using C/G-V. p+/n diode with ION/IOFF > 5E4 is developed. Finally, output characteristics on self-aligned GaSb-pMOSFET are presented.

4F 246

J-1: Carbon Nanotube Devices (Area 13)

13:45 J-1-3
Study on Device Parameters of Carbon Nanotube FETs to Realize Steep Subthreshold Slope of less than 60 mV/decade
B. P. Algul[1], T. Kodera[2], S. Oda[2] and K. Uchida[1], [1]Tokyo Tech and [2]QNERC (Japan)
In carbon nanotube FETs (CNFETs) device parameters to observe subthreshold slope (SS) of less than 60 mV/dec have been studied. It is demonstrated, for the first time, that band-to-band tunneling (BTBT) current can be greatly enhanced by reducing the thickness of inter-layer oxide (t_{int}) between substrate and CNT.

14:00 J-1-4
Metal-Catalyst-Free Growth of Carbon Nanotubes for CMOS Integration
T. Uchino[1], G. N. Ayre[1], D. C. Smith[1], J. L. Hutchison[2], C. H. de Groot[1] and P. Ashburn[1], [1]Univ. of Southampton and [2]Univ.of Oxford (UK)
Metal-catalyst-free growth of carbon nanotube (CNT) on SiO_2 using a thin Ge film is reported for the first time. This growth process is used to produce back gate CNTFETs with Pd source/drain contacts.

2F 222

K-1: Modeling of Power LDMOSFET (Area 14)

2F 223

L-1: Biosensors (Area 11)

13:45 L-1-3
Fast DNA sequencing with nanopore-embedded graphene electrodes
Y. He[1], R. H. Scheicher[2], A. Grigoriev[2], R. Ahuja[2,3], S. Long[1], Z. Ji[1], Z. Yu[1] and M. Liu[1], [1]Laboratory of nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, [2]Condensed Matter Theory Group, Department of Physics and Astronomy, Uppsala University and [3]Applied Materials Physics, Department of Materials and Engineering, Royal Institute of Technology (China)
We set up model and perform simulation of DNA sequencing with nanopore-embedded graphene nanoelectrodes. Simulation results show that compared to sequencing with gold nanoelectrodes, much improved discrimination of different nucleotides and single-base resolution are achieved. The achieved results can provide a design guide for future realization of nanopore-based electrical DNA sequencing.

14:00 L-1-4
Poly Crystalline Silicon Nanowire Field-Effect Transistor for Real-Time Detection of Influenza Virus DNA
C. Y. Hsiao[1], W. T. Lai[1], M. P. Lu[2] and Y. S. Yang[1,2], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)
Real-time detection of avian influenza H5 virus DNA using complementary captured DNA probe modified poly crystalline nanowire field-effect transistor was demonstrated. The result indicated that a simple, quick, and high sensitive biosensor can be developed.

Coffee Break (2F Forum)

4F 243

G-2: RF Circuits and Systems (2) (Area 5)

(14:45-16:05)
Chairs: H. Takao (Kagawa Univ.)
M. Ikebe (Hokkaido Univ.)

14:45 G-2-1
A 5.4-9.2 GHz 19.5 dB CMOS UWB Receiver Frontend Low Noise Amplifier for Confocal Imaging System
A. Azhari, S. Kubota, A. Toya, N. Sasaki and T. Kikkawa, Hiroshima Univ. (Japan)
A 5.4-9.2 GHz CMOS LNA for UWB wireless communication with 19.5 dB power gain and 3.5 dB noise figure is presented. Wireless communication of Gaussian monocycle pulse by horn antennas and LNA is also investigated.

15:05 G-2-2
Confocal Imaging System Using 28.2 Gsample/s UWB Sampling Circuit
A. Toya, N. Sasaki, S. Kubota and T. Kikkawa, Hiroshima Univ. (Japan)
A confocal imaging technique was presented for detecting a target. To realize the technique in CMOS, a high-sampling rate sampling circuit is required. Here, we adopted the 28.2 GSample/s sampling circuit with an improved multiplexer.

4F 244

H-2: Growth of Grapheme for Electronics Applications (Area 8)

(14:45-16:00)
Chairs: H. Hibino (NTT Basic Res. Labs.)
H. Munekata (Tokyo Tech)

14:45 H-2-1 (Invited)
Towards Industrial Applications of Graphene Electrodes
B. H. Hong, Sungkyunkwan Univ. (Korea)
We introduce ultra-large scale (~30 inch) synthesis, roll-to-roll transfer, and chemical doping of graphene films showing excellent electrical and physical properties suitable for practical applications.

15:15 H-2-2
Uniformity of Graphene CVD Growth Depending on the Thickness and Domain Structure of Epitaxial Metal Films
S. Yoshii, K. Nozawa, K. Toyoda and N. Matsukawa, Panasonic Corp. (Japan)
We investigated the graphene growth on epitaxial Ni, Ru and Co films. Locally enhanced segregation at grain boundary was found to be one of the major sources of non-uniformity. Uniform graphene growth was achieved with a single domain thin Ru film, in which grain boundaries were eliminated and segregation was suppressed.

4F 245

I-2: GaN HEMTs (Area 8)

(14:45-16:00)
Chairs: Y. Ohno (Univ. of Tokushima)
S. Kuroda (Sumitomo Electric Device Innovations, Inc.)

14:45 I-2-1 (Invited)
Integration Technologies for GaN Power Transistors
T. Ueda, T. Tanaka and D. Ueda, Panasonic Corp. (Japan)
Newly developed technologies for mono-lithic integration of GaN power switching transistors are reviewed. The topics include the world first GaN-based inverter IC, a novel chip layout eliminating undesired surface flashover to achieve high breakdown voltages with low on-state resistances.

15:15 I-2-2
High-Gain and High-Bandwidth AlGaN/GaN HEMT Comparator
A. M. H. Kwan, K. Y. Wong, X. Liu and K. J. Chen, Hong Kong Univ. of Sci. and Tech. (Hong Kong)
The dynamic response of AlGaN/GaN HEMT voltage comparator was characterized. This comparator with active load demonstrates superior performance of high gain (>31dB) and wide bandwidth (>4MHz), and small propagation delay time (<20ns) over a wide range of temperatures up to 250 deg C.

4F 246

J-2: Carbon Nanotube Properties and Transport (Area 13)

(14:45-16:00)
Chairs: S. Sato (AIST)
S. Akita (Osaka Prefecture Univ.)

14:45 J-2-1
Single Wall Carbon Nanotube Growth from Boron- and Nitrogen-Containing Feedstocks
S. Suzuki and H. Hibino, NTT Corp. (Japan)
BN-doped SWCNTs were successfully grown by thermal CVD method. Blueshifts of Raman spectra were clearly observed, which is an indication of considerable carrier doping. Our results indicate the possibility of both bandgap tuning and carrier doping of SWNTs.

15:00 J-2-2
Transient thermal response of an individual carbon nanotube
Y. Ohshima, T. Arie and S. Akita, Osaka Prefecture Univ. (Japan)
We have investigated the transient thermal response of an individual MWNT under the Joule heating. The suspended MWNT showed the response time within 100 ns corresponding to the transient properties of the electrical input power.

2F 222

K-2: Power Module Technology (Area 14)

(14:45-15:45)
Chairs: T. Shinohe (Toshiba Corp.)
S. Matsumoto (Kyushu Inst. of Tech.)

14:45 K-2-1 (Invited)
High Performance Silicon Carbide Power Modules for Extreme Environment Applications
A. B. Lostetter, J. Hornberger, B. McPherson, R. Shaw, B. Reese and M. Schupbach, Arkansas Power Electronics International, Inc. (USA)
In this presentation, APEI, Inc. will discuss the status of development of our high performance SiC power modules for extreme environment applications.

15:15 K-2-2 (Invited)
Review of Power Converter Temperature and Loss Simulation using Compact Device Models
P. A. Mawby and A. T. Bryant, Univ. of Warwick (UK)
This paper describes the simulation technique developed for the determining the losses in high power converters. |The state of the art models are based on fundamental understanding of the power semiconductor devices that underpin this rapidly evolving technology.

2F 223

L-2: Silicon Based Biomedical Devices (Area 11)

(14:45-16:00)
Chairs: Y. S. Yang (National Chiao Tung Univ.)
J. Ohta (NAIST)

14:45 L-2-1 (Invited)
Advanced Silicon Integration Technologies for Lab-on-Chip and Implantable Device Applications
C. V. Hoof[1,2] and M. O. D. Beeck[1], [1]IMEC and [2]Katholieke Univ. Leuven (Belgium)
This paper will present silicon-based enablers of eHealth. Ultra-low-power circuits will enable wearable wireless health assistants, advanced silicon integration and packaging will enable miniaturized implantable systems, and silicon-based sensors and microsystems will enable Lab-on-Chip (LoC) solutions for personal diagnostics.

15:15 L-2-2
Electronic immunochromatography embedding RFID sensor
Y. Yazawa, C. Gouda, A. Shiratori, T. Oonishi, K. Watanabe and K. Uchida, Hitachi, Ltd. (Japan)
A novel sensitive and quantitative POCT device—incorporating a chemiluminescent reaction and RFID sensor chips into an immunochromatographical test strip—with easy operability was developed and demonstrated.

Wednesday, September 22

1F 211

A-2: Electric Characterization of Organic Semiconductors (Area 10)

15:30 A-2-3
Grain boundary effect on charge transport in pentacene thin films
M. Weis[1], K. Gmucova[1], V. Nadazdy[1], D. Hasko[2], D. Taguchi[3], T. Manaka[3] and M. Iwamoto[3], [1]Slovak Academy of Sciences, [2]International Laser Centre and [3]Tokyo Tech. (Slovakia)
We illustrates with the organic field-effect transistors decrease of the effective mobility and presence of traps with decrease of the grain size. Accumulation of the defects on the grain boundary is also discussed.

1F 212

B-2: Ge MOS Technology 2 (Area 1)

15:25 B-2-3
Suppression of ALD-Induced Degradation of Ge MOS Interface Properties by Low Power Plasma Nitridation of GeO_2
R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka and S. Takagi, Univ. of Tokyo (Japan)
A low power plasma nitridation process to an ultra thin GeO2 IL was proposed to eliminate the degradation induced by ALD Al2O3 deposition, without losing the superior MOS interface properties of GeO2/Ge.

15:45 B-2-4
GeO Desorption Mechanism from GeO_2/Ge Stack Determined by ^{73}Ge Labeling Technique in Thermal Desorption Spectroscopy (TDS) Analysis
S. K. Wang[1], K. Kita[1,2], T. Nishimura[1,2], K. Nagashio[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
Desorption mechanism of GeO from GeO_2/Ge has been studied. We conclude that the GeO desorption initiates from the GeO_2 surface by using ^{73}Ge labeling technique. Two kinds of GeO desorption (uniform and non-uniform) has been demonstrated.

1F 213

C-2: Transport Physics (Area 3)

15:25 C-2-3
Experimental Investigation and Modeling for Surface Roughness Limited Mobility in Strained pMOSFETs
W. P. N. Chen, J. J. Y. Kuo, B. K. Y. Lu and P. Su, National Chiao Tung Univ. (Taiwan)
This work provides an experimental assessment of surface roughness scattering limited mobility under process-induced uniaxial strain. By accurate split C-V mobility extraction method, the surface roughness scattering limited mobility of advanced strained short channel devices has been extracted at cryogenic temperature to suppress phonon scattering mechanism.

15:45 C-2-4
Impact of the Channel Direction Dependent Low Field Hole Mobility on Si(100)
R. Kuroda, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)
The channel direction dependency of low field hole mobility characteristics due to the direction dependency of heavy hole effective mass is experimentally observed for pMOS fabricated on the atomically flat silicon (100) orientation surface.

2F 221

D-2: Advanced Design and Measurement (Area 7)

15:15 D-2-3
Design Rules and Characterisation of Electrically Pumped VECSELS
D. T. D. childs, J. Orchard, L. C. Lin, B. J. Stevens, D. Williams and R. A. Hogg, Univ. of Sheffield (UK)
We present details of the design rules and trade offs in the realisation of CW room temperature operating VECSELs. We focus on measurements of thermal effects specific to electrically pumped devices.

15:30 D-2-4
Programmable optically reconfigurable gate array using a silver-halide holographic memory including six configuration contexts
S. Kubota and M. Watanabe, Shizuoka Univ. (Japan)
This paper presents a practical demonstration of a programmable optically reconfigurable gate array (PORGA) using a silver-halide holographic memory including six configuration contexts. Aspects of the PORGA architecture performance were analyzed experimentally.

4F 241

E-2: Flash Memory Ⅰ (Area 4)

15:25 E-2-3
The Evaluation Method and Characteristics of IPD layer in TLC (Triple Level Cell) NAND Flash
B. D. Jo, Y. Jeong, J. Y. Park, P. H. Kim, S. J. Park, M. K. Cho, K. O. Ahn and Y. Koh, Hynix Semiconductor Inc. (Korea)
As NAND flash market demand for larger capacity at low cost increases, the feature-size scaling and multi-level per bit have been developed. Hence, Triple Level Cell (3 bits per cell) is being intensively developed now. In this paper, we present newly adopted evaluation method of IPD layer and its characteristics in terms of charge trap, program saturation Vth and charge loss according to PV levels in TLC NAND flash.

15:45 E-2-4
A Low Power and Improving Read Disturb Characteristics by Using Multi-CSL Architecture in MLC NAND Flash Memory
M. Kang[1,2], K. T. Park[2], Y. Song[2], S. Lee[2], Y. Lim[2], K. D. Suh[3] and H. Shin[1], [1]Seoul National Univ., [2]Samsung Electronics Co., Ltd. and [3]Sungkyunkwan Univ. (Korea)
In this paper, a new NAND string and its read operation scheme using multi-common source line (CSL) architecture to suppress power consumption and improve the read disturb characteristics were proposed in 40 nm NAND technology.

4F 242

F-2: Novel Structures (Area 9)

15:15 F-2-3
Observation of Resistive Switching in ZnO Single Crystal Whiskers
R. Mohan and S.J. Kim[1], Jeju Nat. Univ. (Korea)
The resistive memory switching in ZnO single crystal whiskers has been investigated. Anomalous resistance fluctuations between intermediate resistance states and RON state have been observed by using the current bias method.

15:30 F-2-4
Formation of thin-film-like Ge quantum dots array in thermally oxidizing SiGe pillar technique for energy harvest/conversion applications
C. C. Wang, K. H. Chen, C. Y. Chien and P. W. Li, National Central Univ. (Taiwan)
We propose a simple method, thermally oxidizing vertical SiGe pillar matrix, for generating dense and size-tunable Ge QD array in a self-organized manner. The knowledge gained from this 3D QD array system is readily transferable for fabricating QD photovoltaic and TE devices.

15:45 F-2-5
KFM Observation of Single-Electron Filling in Isolated and Clustered Dopants
M. Anwar[1], D. Moraru[1], M. Ligowski[1,2], T. Mizuno[1], R. Jablonski[2], Y. Ono[3] and M. Tabe[1], [1]Shizuoka Univ., [2]Warsaw Univ. of Tech. and [3]NTT Basic Res. Labs. (Japan)
We utilized LT-KFM to characterize charging effects in thin P-doped SOI-FETs. We observe single-electron filling, with changing VBG, in isolated and in clusters of dopants. This observation will provide support for design of electronic devices based on single-electron charging of individual dopants.

Special Plenary Session: A Half Century of Esaki Diode and Lasers (Tokyo Dome Hotel)

Special Plenary Session (17:00-18:30)
Chair: Y. Arakawa, Univ. of Tokyo, Japan

17:00 PL-2-1
50 Years of the Laser
K. Shimoda, Univ. of Tokyo, Japan

17:45 PL-2-2
In Half a Century of Research Career, What did I Explore?
L. Esaki, Yokohama College of Pharmacy / The Science and Technology Promotion Foundation of Ibaraki, Japan

18:30-20:00 Reception (Tokyo Dome Hotel)

Wednesday, September 22

4F 243

G-2: RF Circuits and Systems (2) (Area 5)

15:25 G-2-3
Wide-Frequency-Range Low-Noise Injection-locked Ring VCO for UWB Applications in 90 nm CMOS
S. Y. Lee, S. Amakawa, N. Ishihara and K. Masu, Tokyo Tech (Japan)
A scalable, wide-frequency-range (2.62-10.5GHz) and low-noise injection-locked VCO is proposed. In this work, by using an injection locking technique, a 1-MHz-offset phase noise of −119dBc/Hz at 10GHz was achieved with comparable power consumption.

15:45 G-2-4
A 26GHz Transceiver Chipset for Short Range Radar using Post-Passivation Interconnection
S. Ujita, Y. Kawai, K. Kaibara, N. Negoro, T. Fukuda, H. Sakai, T. Ueda and T. Tanaka, Panasonic Corp. (Japan)
26GHz spread-spectrum transceiver chipset for short-range radar fabricated using post-passivation interconnection is presented. Frequency triplers lower the local oscillation frequency, which suppress the carrier leakage. Balun in Rx-IC increases the dynamic range.

4F 244

H-2: Growth of Grapheme for Electronics Applications (Area 8)

15:30 H-2-3
Synthesis of High Quality Graphene Using Diamond-Like Carbon (DLC) as Solid Carbon Source
B. Liu[1], G. Han[1], M. C. Yang[2], Q. Zhou[1], S. M. Koh[1] and Y. C. Yeo[1], [1]National University of Singapore and [2]Data Storage Institute (Singapore)
We report the first demonstration of synthesis of high quality graphene using Diamond-Like Carbon (DLC) as solid carbon source. DLC thickness, nickel thickness, SiO2 capping layer, and annealing temperature are demonstrated to affect graphene quality.

15:45 H-2-4
TEM characterization of epitaxial graphene formed on Si(111), Si(110), Si(100)
H. Handa[1], R. Takahashi[1], S. Abe[1], K. Imaizumi[1], M. H. Jung[1], S. Ito[2], H. Fukidome[1] and M. Suemitsu[1,3], [1]Tohoku Univ. and [2]CREST-JST (Japan)
Graphene forms on 3C-SiC thin films grown on Si substrates by annealing the SiC films in UHV. In this paper, we have conducted cross-sectional TEM measurements on graphene, focusing on the Si surface orientational dependence.

4F 245

I-2: GaN HEMTs (Area 8)

15:30 I-2-3
Suppression of gate leakage and enhancement of breakdown voltage using Al_2O_3 nano particles as gate dielectric for AlGaN/GaN MOS-HEMTs
J. Freedsman, T. Kubo, A. Watanabe, S. L. Selvaraj and T. Egawa, Nagoya Inst. of Tech. (Japan)
We have fabricated AlO nano particles based MOS-HEMT. The MOS-HEMT exhibit good pinch off features with reduced gate leakage and improved breakdown voltage when compared to conventional HEMT. The observed Id-max and gm-max for MIS-HEMT are 425 mA/mm and 121 mS/mm respectively.

15:45 I-2-4
In situ Silane Surface Passivation for Gate-First Undoped AlGaN/GaN HEMTs with Minimum Current Collapse and High-Permittivity Dielectric
X. Liu[1], H. C. Chin[1], E. K. F. Low[1], W. Liu[2], L. S. Tan[1] and Y. C. Yeo[1], [1]National University of Singapore and [2]Inst. of Materials Res. and Engineering, Agency for Sci. Tech. and Res. (Singapore)
An in situ surface passivation technology comprising vacuum anneal and silane treatment was integrated in the fabrication of undoped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs). Excellent DC characteristics with minimum current collapse at room temperature were obtained. DC characteristics at high temperatures were also investigated.

4F 246

J-2: Carbon Nanotube Properties and Transport (Area 13)

15:15 J-2-3
Doubly-suspended carbon nanotube resonator for ultrasensitive mass measurement
K. Oda[1], T. Arie[1,2] and S. Akita[1,2], [1]Osaka Prefecture Univ. and [2]CREST-JST (Japan)
We investigated the oscillation of the doubly-suspended CNT resonator in air and in vacuum by measuring the drain current. The resonant frequency increased with increasing the absolute value of the gate voltage.

15:30 J-2-4
Electronic transport of single-wall carbon nanotubes with superconducting contacts
M. Shimizu[1,2], H. Akimoto[1] and K. Ishibashi[1], [1]RIKEN and [2]Tokyo Univ. of Science (Japan)
We will report our on-going study of the electronic transport properties of the single wall carbon nanotube quantum dot with Al contacts in the high transparency regime and in the intermediate transparency regime (Kondo regime).

2F 222

K-2: Power Module Technology (Area 14)

2F 223

L-2: Silicon Based Biomedical Devices (Area 11)

15:30 L-2-3
Highly Accurate Optical Stimulation of Neuron using Si Neural Probe with Optical Waveguide
R. Kobayashi, S. Lee, S. Kanno, Y. Yukita, K. Lee, T. Fukushima, T. Ishizuka, H. Mushiake, H. Yao, M. Koyanagi and T. Tanaka, Tohoku Univ. (Japan)
A novel Si neural probe with micromachined optical waveguide for optical stimulation of neurons is proposed. We fabricated a carefully-designed Si neural probe and evaluated optical characteristics such as a propagation pattern and output patterns.

15:45 L-2-4
Fabrication and in vivo Evaluation of High Performance Stimulus Electrodes Employed in a CMOS Chip for Retinal Prosthesis
T. Noda[1], S. Tomimatsu[1], K. Sasagawa[1], T. Tokuda[1], Y. Terasawa[2], K. Nishida[3], T. Fujikado[3] and J. Ohta[1], [1]NAIST, [2]NIDEK Co., Ltd. and [3]Osaka Univ. (Japan)
Iridium oxide electrodes with high charge delivery capacity (CDC), employed in CMOS chips for retinal prosthesis, were fabricated. Relationship of fabrication process parameter with CDC was evaluated through electrochemical method. In vivo evaluation was performed using fabricated electrodes, and it confirmed that retinal stimulation was possible.

Special Plenary Session: A Half Century of Esaki Diode and Lasers (Tokyo Dome Hotel)

Special Plenary Session (17:00-18:30)
Chair: Y. Arakawa, Univ. of Tokyo, Japan

17:00 PL-2-1
50 Years of the Laser
K. Shimoda, Univ. of Tokyo, Japan

17:45 PL-2-2
In Half a Century of Research Career, What did I Explore?
L. Esaki, Yokohama College of Pharmacy / The Science and Technology Promotion Foundation of Ibaraki, Japan

18:30-20:00 Reception (Tokyo Dome Hotel)

Thursday, September 23

1F 211

A-3: Organic Light Emitting Diodes (Area 10)
(9:00-10:30)
Chairs: S. Naka (Univ. of Toyama)
S. Aratani (Hitachi, Ltd.)

9:00 A-3-1
Improved the power efficiency of white phosphorescent organic light-emitting diode with thin double emitting-layers and hole-trapping mechanism
F. S. Juang[1], S. H. Wang[1], Y. S. Tsai[1], M. H. Gao[1], Y. Chi[2] and H. P. Shieh[3], [1]National Formosa Univ., [2]National Tsing Hua Univ. and [3]National Chiao Tung Univ. (Taiwan)
Highly-efficiency white PHOLED can be achieved by using thin double-emission layers and doping red phosphor on interface between two emission layers. The yield and power efficiency reach 23.5 cd/A and 17.5 lm/w at 1000 cd/m^2.

9:15 A-3-2
Current Density Dependence of Transient Properties in Green Phosphorescent Organic Light-Emitting Diodes
H. Kajii, N. Takahota, Y. Wang and Y. Ohmori, Osaka Univ. (Japan)
We studied the current density dependence of transient characteristics of green phosphorescent OLEDs. We discussed the transient electroluminescence of green phosphorescent OLEDs using pulses of alternating current sine-waves with various frequencies.

9:30 A-3-3
High efficiency phosphorescent organic light-emitting diode by incorporating an electron transport material into emitting layer
F. S. Juang[1], S. H. Wang[1], Y. K. Tsai[1], B. S. Hsieh[1], Y. Chi[2] and H. P. Shieh[3], [1]National Formosa Univ., [2]National Tsing Hua Univ. and [3]National Chiao Tung Univ. (Taiwan)
Hole transport-type host (TCTA) and electron transport material (TmPyPB) incorporated as mixed-host structure to improve the injection of carriers. White PHOLED shown the yield of 32 cd/A and power efficiency of 20 lm/W (1000 cd/m2).

9:45 A-3-4
Enhancing Efficiency of Organic Light-Emitting Diodes Using a CsI-Doped Electron Transporting Layer
T. W. Kuo, S. H. Su, C. M. Wu and M. Yokoyama, I-Shou Univ. (Taiwan)
Metal compound (CsI) is firstly doped into Alq3 film as an ETL in OLED. It reveals an effective way to promote the electron injection into the EML and further enhance the luminous efficiency.

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B-3: High-k Gate Stack (Area 1)
(9:00-10:30)
Chairs: T. Nabatame (NIMS)
K. Shiraishi (Univ. of Tsukuba)

9:00 B-3-1 (Invited)
Atomic mechanism of Flat band voltage shifts by Oxide dipole Layers in High K-Metal Gate Stacks
J. Robertson and L. Lin, Cambridge Univ. (UK)
The atomic mechanism of the flat band voltage shifts by oxide capping layers is obtained from ab-initio calculations. It is due to the group electronegativity effect, and change of screening at the dielectric interface.

9:50 B-3-3
Fermi-level Pinning and NBTI Free of CMOS HfO_2 By Pre-CF_4 Plasma Passivation
H. H. Chiu, C. S. Lai and J. C. Wang, Chang Gung Univ. (Taiwan)
Advanced performance and reliability were achieved with a zero-IL CMOS by CF4 plasma pre-treatment. A new physical model of interfacial reaction suppression and F re-incorporation were presented to explain FLP free and turn-around NBTI phenomenon.

10:10 B-3-4
Enhanced Electrical Uniformity and Breakdown of Multi-Step Deposited and Annealed HfSiO-Insight by Scanning Tunneling Microscopy
K. S. Yew[1], D. S. Ang[1], K. L. Pey[1], G. Bersuker[2], P. S. Lysaght[2] and D. Heh[2], [1]Nanyang Tech. Univ. and [2]SEMATECH (Singapore)
Grain-boundaries in crystallized high-k film have been shown to induce higher voltage loading on underlying IL, therefore accelerating stack breakdown. Through STM characterization, we show directly multi-step deposition and annealing process improve electrical and breakdown performance of high-k film.

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C-3: Tunnel & Schottky-S/D FETs (Area 3)
(9:00-10:30)
Chairs: K. Okano (Toshiba Corp.)
T. Hase (Renesas Electronics Corp.)

9:00 C-3-1 (Invited)
Tunnel FET Promise and Challenges
T. -J. King Liu and S. H. Kim, Univ. of California Berkeley (USA)
This paper reviews recent advancements in tunnel field effect transistor (TFET) technology and assesses its promise for overcoming the energy efficiency limit of CMOS technology. Challenges for practical implementation of low-cost, low-power TFET digital logic are discussed.

9:30 C-3-2
Optimization of Silicon ρ-channel Tunnel FET with Dual κ Spacer
H. Virani, S. Gundapaneni and A. Kottantharayil, Indian Inst. of Tech. (India)
A dual-k spacer concept is proposed and evaluated in underlap and non-underlap p-channel Silicon tunnel FETs for the first time using extensive device simulations. The dual-k spacer consist of an inner layer made of a high k material and an outer layer made of a low-k material.

9:50 C-3-3
Drive Current Improvement in Si Tunnel Field Effect Transistors by means of Silicide Engineering
D. Leonelli[1,2], A. Vandooren[1], R. Rooyackers[1], A. S. Verhulst[1], S. De Gendt[1,2], M. M. Heyns[1,2] and G. Groeseneken[1,2], [1]IMEC and [2]Katholieke Univ. Leuven (Belgium)
We present a novel Si Multiple Gate Tunneling Field Effect Transistor (MuGTFET) with high-k gate dielectric and metal gate with enhanced electric field by silicide encroachment. The pTFET device exhibits a record on-state current of 7μA/μm at VDD of -0.9V and high I_{ON}/I_{OFF} ratio. Temperature measurements and TCAD simulations confirm the presence of multiple transport mechanisms which explain the degradation of the subthreshold swing.

10:10 C-3-4
Metal Schottky S/D Technology of Ultra Thin SOTB (Silicon on Thin Box) MOSFET
A. Shima, N. Sugii, N. Mise, D. Hisamoto, K. Takeda and K. Torii, Hitachi, Ltd. (Japan)
We reports a novel approach to decrease the parasitic resistance in UT-SOI MOSFET utilizing metal Schottky raised-S/D. Selectively deposited NiSi2 with dopant segregation fabricated by laser spike annealing lowered effective SBH and the contact resistance.

2F 221

D-3: GaN LED (Area 7)
(9:00-10:45)
Chairs: Y. Ishikawa (Univ. of Tokyo)
N. Iizuka (Toshiba Corp.)

9:00 D-3-1
InGaN-based Blue Light-Emitting Diodes with Electron Blocking Layer Fabricated on Patterned Sapphire Substrates
K. T. Liu[1], C. K. Hsu[2] and S. J. Chang[2], [1]Univ. of Cheng Shiu and [2]National Cheng Kung Univ. (Taiwan)
InGaN-based blue light-emitting diode (LED) with electron blocking layer (EBL) fabricated on patterned sapphire substrate (PSS) have been investigated. It is found that PSS-EBL LED have a 209% enhancement in light output power as compared with that of the conventional LED. The improvement can be attributed to the reduction in dislocation density and the better carrier confinement from EBL.

9:15 D-3-2
Enhanced Light Output of Vertical GaN-Based Light-Emitting Diodes with a Distributed Bragg Reflector and a Roughened GaO_x Surface Film
W. C. Lee[1], K. M. Uang[2], T. M. Chen, D. M. Kuo[1], P. R. Wang, P. H. Wang and S. J. Wang, [1]National Cheng Kung Univ. and [2]Wufeng Inst. of Tech. (Taiwan)
The use of a highly reflective DBR CB layer and surface roughening by KrF excimer laser for the fabrication of high-power VLEDs are demonstrated. Enhancement in Lop by 68% at 350 mA has been obtained.

9:30 D-3-3
Epitaxial-Lateral-Overgrowth of Gallium Nitride for Embedding the Micro-Mirror Array
H. M. Ku[1], C. Y. Huang[1,2], C. Z. Liao[2] and S. Chao[1], [1]National Tsing Hua Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
We showed the effect of temperature and pressure on the ELOG process for embedding a MMA in GaN. We demonstrated that nearly double the wall-plug efficiency can be obtained for the MQW-LED with the MMA structure.

9:45 D-3-4
High performance GaN-based light emitting diodes grown on 4-inch Si (111)
Y. Zhu, A. Watanabe, L. Lu, Z. Chen and T. Egawa, Nagoya Inst. of Tech. (Japan)
GaN-based LEDs grown on 4-inch Si (111) substrate by MOCVD have been demonstrated. The light output power can be improved by increasing the thickness of n-GaN with the maximum value of 1.7 mW.

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E-3: Flash Memory Ⅱ (Area 4)
(9:00-10:50)
Chairs: Y. Sasago (Hitachi, Ltd.)
M. Moniwa (Renesas Electronics Corp.)

9:00 E-3-1 (Invited)
Current Development Status and Future Challenges of Charge-Trapping NAND Flash
H. T. Lue, K. Y. Hsieh and C. Y. Lu, Macronix International Co., Ltd. (Taiwan)
Although conventional floating gate (FG) Flash memory has already gone into the 2Xnm node, the technology challenges are formidable beyond 20nm. 3D Charge-trapping (CT) NAND is forecasted as a promising solution to continue NAND Flash scaling for another decade. In this paper, technology challenges of 3D CT NAND and the poly-silicon thin film transistor (TFT) issues will be addressed in detail.

9:30 E-3-2
Collective Tunneling Model in Charge Trap Type NVM Cell
M. Muraguchi[1], Y. Sakurai[2], Y. Takada[2], Y. Shigeta[4], M. Ikeda[3], K. Makihara[3], S. Miyazaki[3], S. Nomura[2], K. Shiraishi[2], T. Endoh[1], [1]Tohoku Univ., [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Univ. of Hyogo (Japan)
We propose new tunneling model in the charge trap NVM cell, where the electron collectively tunnels to the trap sites in the programming mode. This insight is very important to design for MLC CT-cell.

10:10 E-3-4
Atomistic Design of Guiding Principles for High Quality MONOS Memories-First Principles Study of H and O Incorporation Effects for N Vacancies in SiN Charge Trap Layers-
K. Yamaguchi, A. Otake and K. Shiraishi, Univ. of Tsukuba (Japan)
We found N vacancies in SiN layer are suitable charge traps for MONOS-type memory based on first principles calculations. N vacancy maintains its high P/E endurance characteristics even when H and O atoms are incorporated.

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F-3: Spin Manipulation and Photon Detection (Area 9)
(9:00-10:45)
Chairs: H. Gotoh (NTT Corp.)
H. Kosaka (Tohoku Univ.)

9:00 F-3-1 (Invited)
Quantum media conversion from a photon to an electron spin
H. Kosaka, H. Shigyou, T. Inagaki, Y. Mitsumori, K. Edamatsu, T. Kutsuwa, M. Kuwahara, K. Ono, Y. Rikitake, N. Yokoshi and H. Imamura, Tohoku Univ. (Japan)
We present a way of quantum media conversion from a photon to an electron together with the reverse conversion from an electron to a photon using a semiconductor quantum structure.

9:30 F-3-2
Spin-relaxation Dynamics of Excited Trion States in an InAs Quantum Dot
Y. Igarashi[1,2], M. Shirane[1,2], Y. Ota[2,3], M. Nomura[2], N. Kumagai[2], S. Ohkouchi[2], A. Kirihara, S. Ishida, S. Iwamoto, S. Yorozu and Y. Arakawa[2,3], [1]NEC Corp., [2]INQIE and [3]Univ. of Tokyo (Japan)
We performed photoluminescence and photon cross-correlation measurements of charged (bi) exciton states in a quantum dot (QD). Compared with numerical simulations, we evaluated spin-relaxation rates of QD hole-spins.

9:45 F-3-3
Single-Photon Detection by Individual Dopants and the Effect of Channel Shape in SOI-FET
A. Udhiarto[1], D. Moraru[1], R. Nakamura[1], S. Miki[1], T. Mizuno[1], V. Mizeikis[2] and M. Tabe[1], [1]Univ. of Shizuoka and [2]Univ. of Shizuoka (Japan)
We demonstrated single-photon detection by individual dopants in SOI-FET based on trapping and de-trapping of single photo-generated electrons. We show that detection sensitivity can be controlled by channel shape.

10:00 F-3-4
Spin Resonant Tunneling through Quantum Dots with Engineered g-factors
S. M. Huang[1,2], Y. Tokura[3,4], H. Akimoto[1], K. Kono[1], J. J. Lin[2], S. Tarucha[4,5] and K. Ono[1,4], [1]Low temperature physics lab., RIKEN, [2]Inst. of Physics, National Chiao Tung Univ., [3]NTT basic research lab., NTT, [4]Quantum spin information project, ICORP-JST and [5]Univ. of Tokyo (Japan)
We investigate the resonance tunneling through double quantum dots with different g-factors. We found that it is suppressed even though one of the Zeeman sublevels is aligned. The level broadening effect releases the suppression.

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G-3: Modeling, Variation and Reliability (Area 5)
(9:00-10:50)
Chairs: J. C. Guo (National Chiao Tung Univ.)
K. Mizobuchi (Texas Instruments Japan Ltd.)

9:00 G-3-1 (Invited)
A Practical Modeling Solution for Nanodevices with Strain Engineering
D. Chen, R. Lee, U. C. Liu, M. Yeh, B. Huang, M. F. Wang, G. S. Lin, M. K. Tsai, J. H. Lai and C. S. Yeh, UMC (Taiwan)
A compact model solution for layout-dependent effects in advanced CMOS technologies with strain engineering is proposed. Without modeling these effects, the pre-layout and post-layout simulations may have more than 10% difference in device behaviors.

9:30 G-3-2
Analysis of Within-Die and Die-to-Die CMOS-Process Variation With Reconfigurable Ring-Oscillator Arrays
T. Ansari, W. Imafuku, A. Kawabata, M. Yasuda, T. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
Process variations for 180nm CMOS technology in horizontal and vertical chip direction are analyzed with a large ring-oscillator array. Measured within-die variations are found to correlate with simulation results based on the HiSIM model.

9:50 G-3-3
Large Scale Test Circuits for Systematic Evaluation of Variability and Noise of MOSFETs' Electrical Characteristics
Y. Kumagai, K. Abe, T. Fujisawa, S. Watabe, R. Kuroda, N. Miyamoto, T. Suwa, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)
Test circuits that statistically and systematically evaluate variability of Vth, noise, gate leakage current and junction leakage current of MOSFETs are reported.

10:10 G-3-4
A 65nm CMOS 400ns Measurement Delay NBTI-Recovery Sensor by Minimum Assist Circuit
T. Matsumoto[1], H. Makino[1], K. Kobayashi[2] and H. Onodera[1,3], [1]Kyoto Univ., [2]Kyoto Inst. of Tech. and [3]CREST-JST (Japan)
We proposed a NBTI-recovery sensor with 400ns measurement delay which is constructed from a PMOS DUT and two assist NMOSes. It enables high-fidelity NBTI recovery measurement and NBTI recovery follows log t from 400ns.

4F 244

H-3: Oxides and Nanowires (Area 8)
(9:00-10:30)
Chairs: A. Yamada (Tokyo Tech)
M. Nakada (OITDA)

9:00 H-3-1
Crack-Free Epitaxial ZnO film on Si(111) with $Gd_2O_3(Ga_2O_3)$ buffer layer
B. H. Lin[1,2], W. R. Liu[1,2], C. C. Kuo[1], C. H. Hsu[2,1], W. F Hsieh[1,3], M. Hong[4] and J. Kwo[4], [1]National Chiao Tung Univ., [2]National Synchrotron Radiation Research Center, [3]National Cheng Kung Univ. and [4]National Tsing Hua Univ. (Taiwan)
In this letter, we report the growth of crack-free epitaxial ZnO films on Si (111) substrates buffered with Gd2O3(Ga2O3) (GGO). The structural properties of ZnO/GGO/Si(111) hetero-epitaxial system was thoroughly examined by X-ray diffraction (XRD) and transmission electron microscopy (TEM).

9:15 H-3-2
Optical properties of ZnO/Au core/shell nano-tips
Y. H. Ko and J. S. Yu, Kyung Hee Univ. (Korea)
We fabricated the Au/ZnO core/shell nano-tips (NTs) by hydrothermal method and thermal evaporation because the Au has excellent stability for acid dye solution in ZnO based dye sensitized solar cells and good capacity to enhance the light absorption.

9:30 H-3-3
Conductance of Zinc Oxide Nanocontacts Studied by In Situ Transmission Electron Microscopy
T. Kase and T. Kizuka, Univ. of Tsukuba (Japan)
We investigated the relationship the structure and measured I-V characteristic of ZnO NCs by in situ TEM. The results show that the ZnO NC not has rectification property but liner relation showed by I-V curve.

9:45 H-3-4
The Role of Aluminum Catalyst Atoms in Shaping the Structural and Electrical Properties of Epitaxial Silicon Nanowires
O. Moutanabbir[1], S. Senz[1], M. Alexe[1], Y. Kim[1], R. Scholz[1], H. Blumtritt[1], C. Wiethoff[3], T. Nabbefeld[2], F. J. Meyer zu Heringdorf[2], M. Horn-von Hoegen[2], D. Isheim[3] and D. N. Seidman[3], [1]Max Planck Institute of Microstructure Physics, [2]Univ. Duisburg-Essen and [3]Northwestern Univ. (Germany)
To date, a variety of metals have been used to synthesis high-density epitaxial Si nanowires through metal-catalyzed vapor phase epitaxy. Understanding the impact of the catalyst on the intrinsic properties of nanowires is critical for precise manipulation of the emerging Si nanowire-based devices.

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I-3: III-V Device Technologies (Area 6)
(9:00-10:30)
Chairs: K. Maezawa (Univ. of Toyama)
Y. Miyamoto (Tokyo Tech)

9:00 I-3-1 (Invited)
Terahertz Oscillating InGaAs/AlAs Resonant Tunneling Diodes
S. Suzuki and M. Asada, Tokyo Tech (Japan)
We report on our recent results of terahertz oscillators using resonant tunnelling diodes. The characteristics of oscillation frequency, output power, and frequency change with bias voltage and frequency modulation utilizing this property are discussed.

9:30 I-3-2
InSb MOS Diodes on a Si (111) Substrate Grown by Surface Reconstruction Controlled Epitaxy
A. Kadoda, T. Iwasugi, K. Nakatani, K. Nakayama, M. Mori and K. Maezawa, Univ. of Toyama (Japan)
Al_2O_3/InSb MOS diodes were fabricated on a Si (111) substrate. Owing to the novel growth technique, good C-V characteristics showing inversion and accumulation were demonstrated.

9:45 I-3-3
Effect of Fluorine Incorporation on WSi_x/Al_2O_3/GaAs Gate Stack
B. S. Ong[1], K. L. Pey[1], C. Y. Ong[1], C. S. Tan[1], C. L. Gan[1], H. Cai[1], D. A. Antoniadis[2] and E. Fitzgerald[2], [1]Nanyang Tech. Univ. and [2]Massachusetts Institute of Technology (Singapore)
We study the effect of fluorine on the dielectric constant and the device performance on WSi_x/Al_2O_3/GaAs gate stack. The dielectric constant of Al_2O_3 decreases but the device performance improves after fluorine treatment.

10:00 I-3-4
Dependence of Optical Response Time on Gate-to-Source Voltage for InAlAs/InAs/InGaAs Pseudomorphic High Electron Mobility Transistors
T. Ando, H. taguchi, K. Uchimura, M. Mochiduki, T. Iida and Y. Takanashi, Tokyo Univ. of Sci. (Japan)
InAs-PHEMTs exhibited an ultra-high optical response, which the minimum value was as low as $8.1x10^{-12}$ s. From the calculation using the Auger recombination theory, it was found the concentration of holes reaches larger than $2.8x10^{18}cm^{-3}$.

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J-3: Graphene Photonics and Electronics (Area 13)
(9:00-10:30)
Chairs: T. Otsuji (Tohoku Univ.)
K. Nagashio (Univ. of Tokyo)

9:30 J-3-2
Size and Chirality Dependence on Thermoelectric Properties of Graphene Nanoribbons
W. Huang and G. Liang, National Univ. of Singapore (Singapore)
We have studied the thermoelectric properties of GNRs. We find that chirality plays an important role on thermoelectric properties of GNR, and the results show that GNR potentially can be applied to the cooling devices.

9:45 J-3-3
Performance Potentials of Bilayer Graphene and Graphene Nanoribbon FETs
H. Hosokawa, H. Ando and H. Tsuchiya, Kobe Univ. (Japan)
Graphene is expected as a new channel material for FETs. In this paper, we have performed a comparative study on performance potentials between bilayer graphene- and graphene nanoribbon-FETs based on a first-principles approach.

10:00 J-3-4
Epitaxial Graphene-On-Silicon Logic Inverter
A. E. Moutaouakil[1], H. C. Kang[1], H. Handa[1], H. Fukidome[1,3], T. Suemitsu[1,3], E. Sano[2,3], M. Suemitsu[1,3] and T. Otsuji[13], [1]Tohoku Univ., [2]Hokkaido Univ. and [3]CREST-JST (Japan)
We report on the complimentary logic inverter, using two neighboring back-gate epitaxial graphene-on-silicon FETs. The inverting operation was obtained at as low VDD bias as 0.1V, with a matched output/input voltage.

2F 222

K-3: Compound Power Semiconductor Devices (Area 14)
(9:00-10:30)
Chairs: P. Mawby (Univ. of Warwick)
I. Omura (Kyushu Inst. of Tech.)

9:00 K-3-1 (Invited)
Recent Progress in High Voltage MOS-gated Power Transistors in GaN
T. P. Chow, Rensselaer Polytechnic Institute (U.S.A.)
We review the progress in the development of high-voltage MOS-gated power switching FETs in GaN. We present the advantages and disadvantages of various device structures explored. We also discuss technology and reliability issues as well as future trend of GaN vs. SiC for power electronics.

9:30 K-3-2 (Invited)
Progress in SiC Power Semiconductor Devices
T. Shinohe, Toshiba Corp. (Japan)
Silicon carbide (SiC) power semiconductor devices are regarded as the next generation high performance power devices that realize high efficient compact power converters in the various application fields. This presentation shows the current development status of SiC power semiconductor devices and their applications.

10:00 K-3-3
Effects of surface and crystalline defects on reverse characteristics of 4H-SiC JBS diodes
T. Katsuno[1], Y. Watanabe, H. Fujiwara[2], M. Konishi, T. Yamamoto[3] and T. Endo, [1]Toyota Central R&D Labs., Inc., [2]Toyota Motor Corp. and [3]DENSO Corp. (Japan)
Good relations between the reverse characteristics of 4H-SiC JBS diodes and the surface defects were obtained. Micropipe and particle, and carrot-like defect were caused to the low blocking voltage and high leakage current, respectively. Furthermore, the leakage current depended on the threading dislocations.

10:15 K-3-4
High hole current achievement of hydrogen-terminated diamond MOSFETs coated with Poly-tetra-fluoro-ethylene
S. Sato, K. Tsuge, T. Tsuno, T. Ono and H. Kawarada, Waseda Univ. (Japan)
We report that a hydrogen-terminated diamond MOSFET coated with PTFE shows high drain current of -1.2 A/mm and transconductance of 430 mS/mm; the highest value reported in diamond FETs to date.

2F 223

L-3: Nano Structures and Devices (Area 11)
(9:00-10:30)
Chairs: M. Sasaki (Toyota Technological Inst.)
S. Sasaki (OMRON Corp.)

9:00 L-3-1 (Invited)
Applications of Nanotechnology in Biomedical Micro/Nano Devices
G. J. Wang, National Chung Hsing Univ. (Taiwan)
Nanobiotechnology is the branch of nanotechnology that has biological and biochemical applications. In this presentation, fabrications of biomedical micro/nano devices such as the orderly nanostructured PLGA scaffold, nano-patterned microvessel scaffold, high aspect ratio alumina-metal coaxial nanorod and nanotube, and high sensitive 3D nanobiosensor using the anodic aluminum oxide templates are introduced.

9:30 L-3-2
Development of Nanoscale Patterning Method of Self-Assembled Monolayer using Photothermal Desorption in Near-field
Y. Yamamoto, Y. Taguchi and Y. Nagasaka, Keio Univ. (Japan)
We have proposed a novel patterning method of self-assembled monolayer (SAM) in nanoscale using near-field photothermal desorption. This paper reports the patterning principle and the validity of the proposed method.

9:45 L-3-3
Positional control of crystal grains in silicon thin film utilizing cage shaped protein
Y. Tojo[1], A. Miura[1,2], I. Yamashita[1,3,4] and Y. Uraoka[1,4], [1]NAIST, [2]National Chiao Tung Univ., [3]Panasonic Corp. and [4]CREST (Japan)
We propose crystallization method of silicon thin film utilizing cage-shape protein. We performed the selective adsorption of Ni ferritins. The location control of crystal grain was successfully achieved with the optimal size at low temperature.

10:00 L-3-4
Control of Activation Energy for Electron Transport in Two-Dimensional Array of Si Nanodisks
M. Igarashi[1], C. H. Huang[1], T. Morie[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]Kyushu Inst. of Tech. (Japan)
The transformation from pulse input signals to decayed analog outputs through 2D array of Si-nanodisks was clearly observed. The activation energy for this transformation in this array could be controlled by changing the nanodisk thickness.

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A-3: Organic Light Emitting Diodes (Area 10)

10:00 A-3-5
Maskless Patterning of Vapor-Deposited Photosensitive Film and its Application to Organic Light-Emitting Diodes
M. Muroyama, W. Saito, S. Yokokura, K. Tanaka and H. Usui, Tokyo Univ. of Agri. and Tech. (Japan)
A patterned of emissive layer (EML) of organic light-emitting diode was prepared by coevaporating carbazole acrylate monomer and photoinitiator followed by UV exposure and rinsing in a solvent. It was found that the patterning process polymerizes the EML and stabilizes the device characteristics and can be repeated to prepare multiple patterns.

10:15 A-3-6
Direct Probing of Carrier Behavior in Electroluminescence IZO/α-NPD/Alq3/LiF/Al Diode by Time-Resolved Optical Second-Harmonic Generation
D. Taguchi, L. Zhang, J. Li, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
By using electric-field-induced optical second-harmonic generation and transient electroluminescence (EL) measurements, we directly probed carrier transient leading to EL in organic light-emitting diodes. The charging-/discharging-time at multi-layer interface was responsible for EL response time.

Short Presentation
P-10 (11:00-12:15)
Chairs: E. Itoh (Shinshu Univ.)
S. Naka (Univ. of Toyama)

1F 212

B-3: High-k Gate Stack (Area 1)

Short Presentation
P-1 (11:00-12:15)
Chairs: Y. Hayami (Fujitsu semiconductor Ltd.)
S. Tsujikawa (Sony Corp.)

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C-3: Tunnel & Schottky-S/D FETs (Area 3)

Short Presentation
P-3 (11:00-12:15)
Chairs: Y. Nishida (Renesas Electronics Corp.)
F. Boeuf (ST Microelectronics)

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D-3: GaN LED (Area 7)

10:00 D-3-5
GaN based Light Emitting Diode with Enhanced Optical Output and Improved Luminescence by employing Excimer Laser Irradiation in contact formation
G. H. Wang[1], T. Sudhiranjan, T. C. Wong, X. Wang[2], H. Y. Zheng, T. K. Chan[3], T. Osipowicz and Y. L. Foo[1], [1]Inst. of Materials Res. And Eng., [2]Singapore Inst. Of Manufacturing Tech. and [3]National Univ. of Singapore (Singapore)
We report the fabrication of laser annealed p contact on GaN for enhanced optical output from LEDs. At an optimal laser fluence, excimer laser irradiation led to contact resistivity reduction, resulting in a lower turn on voltage. LEDs with laser annealed contacts further show 2.3 times enhanced electroluminescence in the blue light region.

10:15 D-3-6
Light Emission Enhancement of GaN-Based Photonic Crystal With Ultraviolet AlN/AlGaN Distributed Bragg Reflector
C. C. Chen[1], J. R. Chen[1], Y. C. Yang[2], M. H. Shih[1,2] and H. C. Kuo[1], [1]National Chiao Tung Univ. and [2]RCAS (Taiwan)
We demonstrated two-dimensional photonic crystal band-edge coupling operation with an ultraviolet AlN/AlGaN distributed Bragg reflector (UVDBR). A five-fold enhancement in photoluminescence emission was also achieved at 374 nm wavelength. We also employed the photonic crystal band-edge mode examined with plane-wave expansion (PWE) simulation.

10:30 D-3-7
Light Output Enhancement of Ultraviolet Light Emitting Diodes with Pattern HfO_2/SiO_2 Distributed Bragg Reflector
B. S. Cheng[1], C. H. Chiu[1], M. H. Lo[1], H. C. Kuo[1], T. C. Lu[1], Y. J. Cheng[2] and S. C. Wang[1], [1]National Chiao Tung Univ. and [2]Academia Sinica (Taiwan)
The UVLEDs with pattern DBR structure were fabricated via an e-gun evaporation system and ELOG technique. The luminous intensity of this novel structure can be enhanced approximately 75% than the conventional UVLED structure.

Short Presentation
P-7 (11:00-12:15)
Chairs: J. Fujikata (NEC Corp.)
M. Tokushima (AIST)

4F 241

E-3: Flash Memory Ⅱ (Area 4)

10:30 E-3-5
Dynamics of the Charge Centroid in MONOS Memory Cells during Avalanche Injection and FN Injection Based on Incremental-Step-Pulse-Programming
J. Fujiki, T. Haimoto, N. Yasuda and M. Koyama, TOSHIBA Corp. (Japan)
we have extracted charge-centroid dynamics during avalanche injection, on the basis of ISPP analysis. We confirmed carriers are trapped near the middle of the charge layer at first and then reach the top interface of the charge layer. In contrast, with higher electric field, carriers are captured near the top interface of the charge layer.

Short Presentation
P-4 (11:00-12:15)
Chairs: M. Moniwa (Renesas Electronics Corp.)
T. Eshita (Fujitsu Semiconductor Ltd.)

4F 242

F-3: Spin Manipulation and Photon Detection (Area 9)

10:15 F-3-5
Coherent Manipulation and Bi-Directional Polarization of Nuclear Spins in a Quantum Dot Device
R. Takahashi[1,2], K. Kono[1,2], S. Tarucha[3,4] and K. Ono[2,5], [1]Tokyo Tech, [2]RIKEN. [3]Univ. of Tokyo, [4]ICORP-JST and [5]CREST-JST (Japan)
We introduce an electrically pumped bi-directional dynamic nuclear polarization with using a double quantum dot device. We confirmed that directions of this bi-directional polarization can be switched only source-drain voltage. In double quantum dot devices, this bi-directional polarization appears not depending on device structures and materials.

10:30 F-3-6
Transmission Characteristics of a Quantum Point Contact for Edge Magnetoplasmons
K. Washio[1], M. Hashisaka[1], H. Kamata[1,2], K. Muraki[2] and T. Fujisawa[1], [1]Tokyo Tech and [2]NTT Basic Res. Labs. (Japan)
We investigate transmission characteristics of edge magnetoplasmons at a quantum point contact acting as a beam splitter. The obtained transmission characteristics of edge magnetoplasmons are different from conventional tunneling characteristics.

Short Presentation
P-9 and P-12 (11:00-12:15)
Chairs: K. Ono (RIKEN)
Y. Uraoka (NAIST)
K. Yagami (Sony Corp.)
M. Oogane (Tohoku Univ.)

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

12:15-13:15 Lunch

Thursday, September 23

4F 243

G-3: Modeling, Variation and Reliability (Area 5)

10:30 G-3-5
Prediction of Circuit Degradation with Transient BTI and HC Simulations
D. Hagishima, T. Ishihara, K. Matsuzawa and K. Masuda, Toshiba Corp. (Japan)
We have developed the circuit simulation coupled with dynamic transistor degradations. Our simulation predicts the circuit characteristics more precisely than the conventional methods by self-consistent calculations between circuit and reliability simulations.

4F 244

H-3: Oxides and Nanowires (Area 8)

10:00 H-3-5
Growth and Characterization of GaAsP Nanowires on GaAs(111)B Substrate by Selective-Area Metal Organic Vapor Phase Epitaxy
S. Fujisawa, T. Sato, S. Hara, J. Motohisa, K. Hiruma and T. Fukui, Hokkaido Univ. (Japan)
To form vertical one-dimensional heterostructure, we fabricated GaAsP nanowires on GaAs(111) B substrates by using selective-area MOVPE. By analyzing the growth conditions, we succeeded in forming nanowire array with good crystal quality.

10:15 H-3-6
Fabrication of Rectifying Pt/TiO_x/Pt by RF-Magnetron Sputtering
N. Zhong[1,2], H. Shima[1,2] and H. Akinaga[1,2], [1]AIST and [2]CREST-JST (Japan)
Rectifying Pt/TiOx/Pt was prepared by RF-magnetron sputtering. An Ohmic contact is always found at BE/TiOx interface due to the intrinsic-dead layer. I-V characteristic of Pt/TiOx/Pt depends on the TiOx/TE interface. Devices with TiOx layer prepared closing to the oxide mode exhibit rectifying properties. By optimize post annealing treatment process, the rectifying ratio at ±1.0V increases from 20 to 4×10^3.

4F 245

I-3: III-V Device Technologies (Area 6)

10:15 I-3-5
Defect-free GaAs/AlGaAs Heterostucture Etching Process by Chlorine/Argon Mixed Gas Neutral Beam
X. Y. Wang[1,3], C. H. Huang[1,3], Y. Ohno[1,3], M. Igarashi[1,3], A. Murayama[2,3] and S. Samukawa[1,3], [1]Tohoku Univ., [2]Hokkaido Univ. and [3]CREST-JST (Japan)
Using chlorine/argon mixed gas neutral beam, we developed a dry etching process for fabricating GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructure with characteristics of defect-free, etching selectivity of GaAs/$Al_{0.3}Ga_{0.7}As$ closes to 1, atomically smooth etched surface, and vertical etch profile.

4F 246

J-3: Graphene Photonics and Electronics (Area 13)

10:15 J-3-5
Study of Hot Carriers in Optically Pumped Graphene
A. Satou[1,3], T. Otsuji[1,3] and V. Ryzhii[2,3], [1]Tohoku Univ., [2]Univ. of Aizu and [3]Japan Science and Technology Agency (Japan)
We studied theoretically hot carriers in optically pumped graphene which can be utilized as THz laser. We showed that the population inversion is possible with sufficiently strong pumping.

2F 222

K-3: Compound Power Semiconductor Devices (Area 14)

2F 223

L-3: Nano Structures and Devices (Area 11)

10:15 L-3-5
Optical Characteristics of Two-dimensional Array of Si Nano-disks Fabricated by Defect-free Neutral Beam Etching with Bio-template
C. H. Huang[1,4], M. Igarashi[1,4], M. F. Budiman[1], R. Oshima[2,4], I. Yamashita[3,4], Y. Okada[2,4] and S. Samukawa[1,4], [1]Tohoku Univ., [2]Univ. of Tokyo, [3]NAIST and [4]CREST (Japan)
We created a 2D Si-ND array with a high-density and well-ordered arrangement using bio-template. The *Eg* and PL emission peaks can be easily controlled by changing the ND thickness.

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
Short Presentation P-5 (11:00-12:15) Chairs: S. Sugawa (Tohoku Univ.) T. Koide (Hiroshima Univ.)	Short Presentation P-2 and P-8 (11:00-12:15) Chairs: Y. Hayashi (Renesas Electronics Corp.) N. Nakano (Keio Univ.) A. Yamada (Tokyo Tech) H. Hibino (NTT Basic Res. Labs.)	Short Presentation P-6 (11:00-12:15) Chairs: T. Hashizume (Hokkaido Univ.) S. Tanaka (Shibaura Inst. Tech.)	Short Presentation P-13 (11:00-12:15) Chairs: J. Motohisa (Hokkaido Univ.) S. Uno (Nagoya Univ.)	Short Presentation P-14 (11:00-12:15) Chairs: K. Ohdaira (JAIST) K. Nishioka (Univ. of Miyazaki)	Short Presentation P-11 (11:00-12:15) Chairs: Y. Taguchi (Keio University) I. Yamashita (NAIST)

12:15-13:15 Lunch

Thursday, September 23

1F 211

A-4: Organic Memory and Related Materials (Area 10)
(15:10-16:25)
Chairs: K. Kato (Niigata Univ.)
S. H. Su (I-Shou Univ.)

15:10 A-4-1 (Invited)
Molecular Memory Nano-interfaced with Organic Molecules
H. Lee[1] and M. H. Jung[2], [1]SungKyunkwan Univ. and [2]Electronics and Telecommunications Res. Inst. (Korea)
For the demonstration of new concept of organic nonvolatile memory devices, herein we report an OFET memory device built on a silicon wafer and based on films of pentacene and a SiO2 gate insulator that are separated by push-pull organic molecules (PPOMs) acting as a gate dielectric. We like to briefly report the design motif and synthesis of PPOMs.

15:40 A-4-2
The dry etching process for patterning P(VDF-TeFE) thin film with various conditions
D. Terashima, J. H. Jeong, C. Kimura and H. Aoki, Osaka Univ. (Japan)
We have used P(VDF-TeFE) thin film for piezoelectric micro-generator. Increasing the surface area, the film was etched by dry etching processes. In this study, we changed the dry etching conditions and observed its variation.

15:55 A-4-3
The influence of the intensity of an electric field on properties of P(VDF-TeFE) thin films during the annealing process
J. H. Jeong, D. Terashima, C. Kimura and H. Aoki, Osaka Univ. (Japan)
To improve properties of P(VDF-TeFE) thin film, we have carried out the annealing process at a temperature higher than melting point with an electric field. In this study, we have studied the relationship between the film properties and the intensity of an electric field on the annealing process.

16:10 A-4-4
Carrier Transport in Electrical Bistable Device based on Hyperbranched Polymer and Gold Nanoparticle Composite Thin Films
H. Ichikawa[1], K. Yasui[2], M. Ozawa[2], K. Ôdoi[2] and K. Fujita[1], [1]Kyushu Univ. and [2]Nissan Chemical Indus. Ltd. (Japan)
Organic electrical bistable devices utilizing hyperbranched polymer and metal nanoparticle composite has been investigated. It is suggested that the conductivity of this device depends on tunnel current, according to the temperature dependency.

1F 212

B-4: Process Integration (Area 1)
(15:10-16:20)
Chairs: J. Yugami (Renesas Electronics Corp.)
S. Tsujikawa (Sony Corp.)

15:10 B-4-1 (Invited)
High-k/Metal Gate Technology toward 14nm generation
M. Takayanagi, Toshiba America Electronic Components, Inc. (USA)
High-k/metal gate technology for current node is reviewed. In addition, remaining challenges and perspective to future node toward 14nm generation is discussed in this paper.

15:40 B-4-2
Analytical Approach for Enhancement of nMOSFET Performance with Si:C Source/Drain Formed by Molecular Carbon Ion Implantation and Laser Annealing
T. Yamaguchi, Y. Kawasaki, T. Yamashita, N. Miura, M. Mizuo, J. Tsuchimoto, K. Eikyu, K. Maekawa, M. Fujisawa and K. Asai, Renesas Electronics Corp. (Japan)
The channel strain induced by Si:C-S/D formed using molecular carbon ion implantation and laser annealing was successfully measured by UV Raman spectroscopy. It was also confirmed that the performance of nMOSFETs is effectively improved by strained Si:C-S/D.

16:00 B-4-3
Mechanism to Achieve PMOS and NMOS Band Edge Work Function using Low Temperature Tuning Process for Low Power Application
C. S. Park[1], G. Bersuker[1], T. Ngai[1], J. Huang[1], K. H. Lin[2], J. Barnett[1], J. Price[1], K. Rader[1], P. Lysaght[1], B. Taylor[1], P. D. Kirsch[1] and R. Jammy[1], [1]SEMATECH and [2]UMC (USA)
Band edge work function metal gates for N- and P-MOSFETs, respectively, were achieved at low EOT with excellent gate leakage through the low temperature process flow using WF tuning techniques.

1F 213

C-4: Tr & SRAM Variabilities (Area 3)
(15:10-16:25)
Chairs: T. Tanaka (Fujitsu Semiconductor Ltd.)
F. L. Yang (National Nano Device Labs.)

15:10 C-4-1
Effective Suppression of Random-Dopant-Induced Characteristic Fluctuation Using Dual Material Gate Technique for 16 nm MOSFET Devices
K. F. Lee, Y. Li, C. Y. Yiu and T. T. Khaing, National Chiao Tung Univ. (Taiwan)
Threshold voltage (Vth) fluctuation has become a crucial problem for nowadays nano-CMOS devices. The random dopant fluctuation (RDF) has shown as the major source of variation. Suppression of RD-induced Vth fluctuation is urgent for variability of sub-22-nm device technologies. Dual material gate (DMG) was recently proposed to improve device performance.

15:30 C-4-2
High Temperature Characteristic of Radom Variability of Drain Current in Scaled FETs
T. Tsunomura[1], A. Kumar[2], T. Mizutani[2], A. Nishida[1], K. Takeuchi[1], S. Inaba[1], S. Kamohara[1], K. Terada[3], T. Hiramoto and T. Mogami[1], [1]MIRAI-Selete, [2]Univ. of Tokyo and [3]Hiroshima City Univ. (Japan)
High temperature characteristic of random variability of drain current is analyzed. It is clarified that the drain current variability decreases at high temperature. This reduction is mainly due to the current onset component.

15:50 C-4-3
Device Engineering to Improve SRAM Static Noise Margin
J. Luo[1], L. Wei[1], F. Boeuf[2], D. Antoniadis[3], T. Skotnicki[2] and H. S. P. Wong[1], [1]Stanford Univ., [2]STMicroelectronics and [3]MIT (USA)
We examine the impact of device I-V characteristics on SRAM SNM by analyzing the switching trajectories. 12% improvement in both read and write SNM are achieved by decreasing the transistor DIBL from 150mV/V to 50mV/V.

16:10 C-4-4 (Late News)
Qualitative Differences Between Conduction Band Edge Excitonic States and Electron Tapping in (i) SiO_2 and (ii) Si_3N_4 and Si Oxynitride Alloy Films
G. Lucovsky, NC State Univ (USA)
Many electron wavefunctions and X-ray absorption spectrocopy are combined to provide sigifincant information about band edge, and O and N vacancy defects.

2F 221

D-4: Photonic Crystal Devices (Area 7)
(15:10-16:25)
Chairs: M. Tokushima (AIST)
N. Iizuka (Toshiba Corp.)

15:10 D-4-1 (Invited)
Information processing and sensing with photonic crystal microcavities in SOI
P. M. Fauchet, Univ. of Rochester (USA)
The optical transmission in 2-D photonic crystal microcavities made in SOI is strongly affected by a small change in the refractive index inside the defect hole. This principle has been used to develop biosensors capable of detecting tiny amounts of biological targets such as a single virus, and electro-optic (E-O) modulators that require only ~1 fJ of electrical energy to switch an optical bit.

15:40 D-4-2
Pulse selection by on-the-fly wavelength conversion in 2D photonic crystals
T. Asano, J. Upham, Y. Tanaka and S. Noda, Kyoto Univ. (Japan)
We propose and demonstrate an application of ultrafast on-the-fly wavelength conversion technique developed previously. We selectively deflect an input light pulse from a photonic crystal waveguide by combining that technique and a photonic crystal nanocavity.

15:55 D-4-3
Demonstration of a Silicon photonic Crystal Slab LED with Efficient Electroluminescence
S. Nakayama, S. Iwamoto, S. Ishida and Y. Arakawa, Univ. of Tokyo (Japan)
We report the first demonstration of silicon photonic crystal (PhC) LEDs. Lateral p-i-n diodes with PhC structures were fabricated and efficient electroluminescence was observed from this structure compared to that without PhC patterns.

16:10 D-4-4
Optimized Micro-Cavity and Photonic Crystal in GaN-based Thin-Film Light-Emitting Diodes for Highly Directional Beam Profiles
C. F. Lai, C. H. Chao and W. Y. Yeh, Indus. Tech. Res. Inst. (Taiwan)
Highly directional far-fields of GaN PhC ultra-thin film LED (uTFLED) have been demonstrated. Output power enhancement of ~3.78x compared to non-PhC uTFLED and highly directional far-field with half intensity angle of ±17°have been achieved.

4F 241

E-4: Flash Memory Ⅲ (Area 4)
(15:10-16:10)
Chairs: Y. C. Chen (Macronix International Co., Ltd.)
T. Endoh (Tohoku University)

15:10 E-4-1
Y-disturb Study of Charge-trapping Type Non-volatile Memory Cell for 45nm Generation Node
T. F. Ou, C. H. Cheng, W. C. Tzeng, G. D. Lee, S. H. Ku, C. H. Liu, K. W. Liu, N. K. Zous, W. J. Tsai, S. W. Huang, M. S. Chen, W. P. Lu, K. C. Chen and C. Y. Lu, Macronix Intl Co., Ltd. (Taiwan)
In 45nm virtual ground array, the disturbance in the width direction is mainly induced by secondary hot electrons. Fine tuning the junction implantations or increasing the program WL bias can effectively improve the disturbance.

15:30 E-4-2
In-Depth Study on Mechanism of the Performance Improvement by High Temperature Annealing of the Al_2O_3 in a Charge-Trap Type Flash Memory Device
J. K. Park[1], Y. Park[1], S. K. Lim[2], J. S. Oh[2], M. S. Joo[3], K. Hong[3] and B. J. Cho[1], [1]KAIST, [2]National Nanofab Center and [3]Hynix Semiconductor Inc. (Korea)
In TANOS device, enhanced retention property upon high temperature oxygen annealing can be contributed to not suppressing the trap-assisted tunneling current but changes of the conduction band offset of the crystallized Al2O3.

15:50 E-4-3
POST-BREAKDOWN RECOVERABLE METAL NANOCRYSTAL-BASED AL_2O_3/SIO_2GATE STACK FOR NON-VOLATILE MEMORY
*Y. N. Chen[1,2], K. L. Pey[1], K. E. J. Goh[2], Z. Z. Lwin[1], P. K. Singh[3], S. Mahapatra[3], Q. X. Wang[4] and J. Zhu[4], [1]Nanyang Tech. Univ., [2]Inst.of Material Res.and Eng., A*STAR, [3]Indian Inst.of Tech. and [4]GlobalFoundries Singapore Pte. Ltd (Singapore)*
Recovery of electrical performance in post-breakdown Ru metal nanocrystal-based high-k/SiO2 non-volatile memory gate stack is realized with electrical methods. A physical model based on oxygen vacancy annihilation is proposed for the recovery mechanism.

4F 242

F-4: Quantum Dots (Area 9)
(15:10-16:25)
Chairs: T. Fujisawa (Tokyo Tech.)
A. Dzurak (Univ. of New South Wales)

15:10 F-4-1 (Invited)
Spin-based Quantum Information Processing in Silicon
A. S. Dzurak, Univ. of New South Wales (Australia)
We review electron spin qubits in silicon based on both dopant atoms and gate-defined quantum dots. Single-shot readout of an electron spin in Si was demonstrated using implanted P donors tunnel-coupled to a Si SET. Readout fidelity was > 90% and spin lifetime T1 ~ 6 s. Measure-ments of valley splitting and spin filling in Si MOS quan-tum dots will also be discussed.

15:40 F-4-2
Simulation study of charge modulation in coupled quantum dots in silicon
T. Kambara[1], T. Kodera[1,2], G. Yamahata[1], K. Uchida[1] and S. Oda[1,2], [1]Tokyo Tech and [2]Univ. of Tokyo (Japan)
We have investigated the number of electrons in Si DQD by simulation with various applied voltages of the top gate and side gates. With optimum gates bias, a few-electron DQD is formed.

15:55 F-4-3
Preparation of SOI-based Double Quantum Dots Structure Defined by Geometry and Electrostatically
M. A. Sulthoni, T. Kodera, K. Uchida and S. Oda, Tokyo Tech (Japan)
We studied two aspects of the fabrication of silicon DQD structure. 3D numerical simulation is used to find optimum structure of such device, and fabrication using electron beam lithography is optimized experimentally.

16:10 F-4-4
Single Electron Transistors (SETs) for Reducing Source/Drain Resistance and MOS Current
J. E. LEE, W. B. Shim, J. G. Yun, K. C. Kang, J. H. Lee, H. Shin and B. G. Park, Seoul National Univ. (Korea)
Since a Metal-Oxide-Semiconductor (MOS) was developed, the scaling down of devices has been the most effective method for the improvement of device performance. However, as the scaling down of devices reaches sub-micron region, it reveals problems such as the short channel effect and power consumption.

Thursday, September 23

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G-4: Advanced Analog Circuits (Area 5)
(15:10-16:25)
Chairs: T. Hirose (Kobe Univ.)
T. Koide (Hiroshima Univ.)

15:10 G-4-1
A Gate-drain Coupling Distributed Amplifier in 90-nm CMOS Technology
C. Y. Hsiao, W. B. Y. Wang, T. Y. Su, Y. C. Wu and S. S. H. Hsu, National Tsing Hua Univ. (Taiwan)
This paper proposed a distributed amplifier in 90-nm CMOS technology, using the gate-drain transformer coupling and pattern ground folded layout method to achieve high gain-bandwidth of 137.2 GHz and minimized chip size of 0.97x0.42 mm2.

15:30 G-4-2
A 60dB SFDR Low-Noise Amplifier with Variable Bandwidth for Neural Recoding Systems
K. Sueishi[1], T. Yoshida[1], A. Iwata[2], K. Matsushita[3], M. Hirata[3] and T. Suzuki[4], [1]Hiroshima Univ., [2]A-R-Tech Corp., [3]Osaka Univ. and [4]Univ. of Tokyo (Japan)
Recently, a brain machine interface (BMI) /brain computer interface (BCI) has been researched in order to restore communication function for the severely disabled people due to amyotrophic lateral sclerosis, spinal injury, brain stroke etc. Especially, Electrocorticograms (EcoG) is attracting attention as a key signal to realize these systems.

15:50 G-4-3
Temperature Compensated Nano-Ampere CMOS Current Reference Circuit Using Small Offset Voltage
Y. Osaki, T. Hirose, N. Kuroki and M. Numa, Kobe Univ. (Japan)
We developed a low-power current reference circuit with little temperature dependence for micro-power LSIs in a 0.35-μm standard CMOS process.

16:10 G-4-4 (Late News)
Low-voltage Power Supply Regulator for Subthreshold-operated CMOS Digital LSIs
K. Ueno, H. Shimada, T. Asai and Y. Amemiya, Hokkaido Univ. (Japan)
Our regulator accepted a battery voltage (1-3.3V) and produced a minimum supply voltage (0.5-1.2V) for operating subthreshold logic circuits at a speed determined by a CR reference, regardless of PVT variations.

4F 244

H-4: Carbon Interconnect (Area 2)
(15:10-16:20)
Chairs: M. Nihei (AIST)
M. Matsuura (Renesas Electronics Corp.)

15:10 H-4-1 (Invited)
Thermal Transport in Graphene and Few-Layer Graphene: Applications in Thermal Management and Interconnects
A. A. Balandin, Univ. of California, Riverside (USA)
In this talk I will review the results of our experimental and theoretical investigation of thermal conduction in graphene and few-layer graphene. Graphene applications in interconnects, thermal management and 3D electronics will be discussed.

15:40 H-4-2
Plasma Discharge Condition Dependence of the Crystallographic Quality of Networked Nanographite Grown by the Photoemission-Assisted Plasma-Enhanced CVD
S. Ogawa[1,2], T. Kaga[1], Y. Ohtomo[1], M. Sato[2,3], M. Nihei[2,3] and Y. Takakuwa, [1]Tohoku Univ., [2]CREST-JST and [3]Fujitsu Ltd. (Japan)
In the photoemission-assisted plasma CVD, the crystallographic quality of networked graphite is improved with decreasing the plasma voltage. The considerable reasons are the decrease of growth rate, and the decrease of ion collision to the substrate.

16:00 H-4-3
Carbon Nanotube Growth for Vias and Interconnects
J. Robertson[1], C. S. Esconjauregui[1], B. C. Bayer[1], F. Yan[1], G. Zhong[1], J. Dijon[2] and H. Okuna[2], [1]Cambridge Univ. and [2]CEA (UK)
We achieve nanotube growth densities of 2E12 to 5E12 cm-2 by particular catalyst pre-treatments, for use in Vias and interconnects, the highest achieved to date.

4F 245

I-4: Silicon Carbide Devices (Area 6)
(15:10-16:25)
Chairs: R. Hattori (Mitsubishi Electric Corp.)
T. Hashizume (Hokkaido Univ.)

15:10 I-4-1 (Invited)
SiC Power devices – Recent progress and upcoming challenges
P. Friedrichs, SiCED Electronics Development GmbH & Co.KG (Germany)
The contribution will comment on the role of SiC power semiconductor devices in industrial electronics with a focus on high power densities and efficiency. Device concepts with their pro's and cons will be discussed. After an outlook into the future of high voltage components a discussion about short time applications for SiC devices will be given.

15:40 I-4-2
Recombination Model at Perimeter of Stacking Faults in 4H-SiC pin Diode with Forward Voltage Drift
K. Nakayama[1,3], Y. Sugawara[1], H. Tsuchida[2], C. Kimura[3] and H. Aoki[3], [1]The Kansai Electric Power Co., Inc., [2]Central Research Inst. Of Electric Power Industry and [3]Osaka Univ. (Japan)
The relation between the forward and the reverse recovery characteristics of the pin diode with the forward voltage drift was investigated. The recombination model at perimeter of the stacking faults was proposed and it was revealed that the hole lifetime of pin diode shortened by the recombination at perimeter of the stacking faults.

15:55 I-4-3
Influence of inserting AlN between AlSiON and 4H-SiC interface for the MIS structure on SiC
N. Komatsu, T. Satoh, M. Honjo, T. Futatuki, C. Kimura and H. Aoki, Osaka Univ. (Japan)
An interfacial roughness is suppressed by deposition of AlN on SiC. It is half of interfacial roughness between SiC and thermal oxide. Electrical property is developed by the crystallization of AlN.

16:10 I-4-4 (Late News)
Behavior of in-grown Stacking Faults in 4H-SiC Epitaxial Layer Through Annealing Process
R. Hattori, K. Hamano, J. Moritani, K. Sato and T. Oomori, Mitsubishi Electric Corp. (Japan)
We investigated the behavior of SFs in 4Hn-SiC epi-taxial layer during annealing process with PL topographic imaging inspection. As a conclusion, Single Shockley SFs could be completery recovered by the activation annealing process and other SFs still remain after the process.

4F 246

J-4: Graphene's Electrical Properties (Area 13)
(15:10-16:25)
Chairs: K. Maehashi (Osaka Univ.)
K. Nishiguchi (NTT Basic Res. Labs.)

15:10 J-4-1 (Invited)
DOS Bottleneck for Contact Resistance in Graphene FETs
K Nagashio, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)
The contact resistance between graphene and metal is crucially important for achieving potentially high performance of graphene from both physics and practical viewpoints. This paper discusses the metal/graphene contact properties by separating from the intrinsic conduction of graphene.

15:40 J-4-2
Graphene layers dependent vibrational property of metal-graphene heterostructures
S. Entani[1], S. Sakai[1], Y. Matsumoto[1], H. Naramoto[1], T. Hao[1], K. Takanashi[1,2] and Y. Maeda[1,3], [1]JAEA, [2]Tohoku Univ. and [3]Kyoto Univ. (Japan)
Influence of the formation of graphene with various metals on its vibrational properties was studied by micro-Raman spectroscopy.It was revealed that the interface interactions are dramatically different between single layer and multilayer graphenes, which will provide a clue to comprehensive understanding of graphene-based devices.

15:55 J-4-3
Observation of bandgap in epitaxial bilayer graphene field effect transistors
S. Tanabe, Y. Sekine, H. Kageshima, M. Nagase and H. Hibino, NTT Corp. (Japan)
Epitaxial bilayer graphene was grown on SiC. Electronic properties of the graphene were studied in a field effect transistor configuration. As a result, bandgap was observed in the transistor.

16:10 J-4-4
Bridging Growth and Electrical Properties of Single Carbon Nanowall
T. Kanda[1], H. Mikuni[1], K. Yamakawa[2], H. Kondo[1], M. Hiramatsu[3], M. Sekine[1] and M. Hori[1], [1]Nagoya Univ., [2]Katagiri Engineering Co., Ltd. and [3]Meijo Univ. (Japan)
Carbon nanowalls are two-dimensional carbon nanomaterials consisting of stacked graphene sheets. In this study, we fabricated a single bridging carbon nanowall and measured the electrical property.

2F 222

K-4: Next Generation Solar Cells (Area 14)
(15:10-16:25)
Chairs: C. A. Kaufmann (Helmhe. Its Zentrum Berlin)
K. Nishioka (Univ. of Miyazaki)

15:10 K-4-1
Optical and Photoelectrical Characterizations of Wide-gap Nanocrystalline Silicon Layers
R. Mentek, B. Gelloz, M. Kawabata and N. Koshida, Tokyo Univ. of Agri. And Tech. (Japan)
Nanocrystalline silicon fabricated by electrochemical etching is under investigation as a new material for wide-gap solar cells. Interesting properties such as band-gap widening and photo-conduction will be presented during this conference.

15:25 K-4-2
Carrier Transfer Simulation on Si/SiC interface in Quantum Dot Solar Cells
S. Hirose, I. Yamashita, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
In this study, we analyzed the carrier transfer on Si-QD/SiC interface by using the quantum chemical calculation and carrier transfer simulation to analyze the influence of interface defect on conversion efficency.

15:40 K-4-3
Development of Multi-Scale Simulation Method for Dye-Sensitized Solar Cells Including Effect of Photoelectrode Material Interface
M. Onodera, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
Dye-Sensitized Solar Cells (DSSCs) are regarded as next-generation solar cells. We have developed a multi-scale DSSC simulator. We developed the calculation part for the effect of the photoelectrode material interface and improved our DSSC simulator.

15:55 K-4-4 (Late News)
Crystalline Silicon Solar Cells Used with Al and Au Metals
T. Sameshima, K. Kogure and M. Hasumi, Tokyo Univ. of Agri. And Tech. (Japan)
We propose a simple crystalline silicon solar cell using Al and Au metals to cause an internal built-in potential in silicon because of their difference of the work functions. No PN junction is necessary. We also used 1.5 nm SiO2 layer for surface passivation. Solar cell characteristics were experimentally demonstrated well.

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A-4: Organic Memory and Related Materials (Area 10)	**B-4: Process Integration (Area 1)**	**C-4: Tr & SRAM Variabilities (Area 3)**	**D-4: Photonic Crystal Devices (Area 7)**	**E-4: Flash Memory Ⅲ (Area 4)**	**F-4: Quantum Dots (Area 9)**

Coffee Break (2F Forum)

A-5: Organic Electronics and Device Physics (Area 10) (16:50-18:05) Chairs: K. Fujita (Kyushu Univ.) H. Usui (Tokyo Univ. of Agri. & Tech.)	**B-5: Advanced Gate Dielectrics (Area 1)** (16:50-18:10) Chairs: S. Miyazaki (Nagoya Univ.) K. Shiraishi (Univ. of Tsukuba)	**C-5: Si Nanowire Technology (Area 3)** (16:50-18:10) Chairs: N. Mori (Osaka Univ.) F. L. Yang (National Nano Device Labs.)	**D-5: Quantum Dot (Area 7)** (16:50-18:05) Chairs: S. Saito (Hitachi, Ltd.) Y. Ishikawa (Univ. of Tokyo)	**E-5: Flash Memory Ⅳ (Area 4)** (16:50-17:30) Chairs: E. Yang (eMemory Technology Inc.) Y. Sasago (Hitachi, Ltd.)	**F-5: New Functional MOS Structures (Area 9)** (16:50-18:05) Chairs: Y. Takahashi (Hokkaido Univ.) Y. Uraoka (NAIST)
16:50 A-5-1 **Surface Manipulation of Precursor Carbazole Dendron Polymer Thin Films by Conducting-AFM Nanolithography** *A. Baba[1], R. Oyanagi[1], T. Mashima[1], Y. Ohdaira[1], K. Shinbo[1], K. Kato[1], F. Kaneko[1], G. Jiang[2] and R. Advincula[2], [1]Niigata Univ. and [2]Univ. of Houston (Japan)* In this study, conducting AFM nanolithography was used to manipulate the surface morphology of carbazole precursor dendron polymer thin films. Bias voltages were locally applied to the sample by using conducting AFM. We have successfully obtained the locally cross-linked conju-gated polymer due to the polymerization (Cross-linking) and the doping of the polycarbazole.	**16:50 B-5-1** **Asymmetric Gate-oxide Thickness Four-terminal FinFETs Fabricated using Low-Temperature and Atomically Flat interface Neutral-Beam Oxidation Process** *A. Wada[1], K. Endo[2], M. Masahara[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)* Flexibly Vth-controllable symmetric and asymmetric Tox 4T-FinFETs with low-temperature neutral beam oxidation process have been successfully fabricated. These results demonstrate the great potential of NBO process for fabricating three dimensional 4T-FinFETs.	**16:50 C-5-1** **Fully Quantum Study of Silicon Devices with Scattering Based on Wigner Monte Carlo Approach** *S. Koba, R. Aoyagi and H. Tsuchiya, Kobe Univ. (Japan)* In this study, we have developed a fully quantum Monte Carlo simulator based on the Wigner transport formalism, and discussed quantum and dissipative transport in Si nanoscale devices.	**16:50 D-5-1** **Light emission from a strongly coupled single quantum dot-photonic crystal nanobeam cavity system** *R. Ohta, Y. Ota, M. Nomura, N. Kumagai, S. Ishida, S. Iwamoto and Y. Arakawa, Univ. of Tokyo (Japan)* InGaAs single quantum dot-photonic crystal nanobeam cavity coupled system is fabricated and clear cavity QED effect is observed for the first time. PL spectra measured at various detunings show the strong coupling signature at 4K.	**16:50 E-5-1** **Investigation of Threshold Voltage Disturbance Caused by Programmed Adjacent Cell in Virtual Source/Drain NAND Flash Memory Device** *W. Kim, D. W. Kwon, J. H. Ji, J. H. Lee and B. G. Park, Seoul National Univ. (Korea)* In this paper, we investigate and minimize the threshold voltage disturbance caused by programmed adjacent cell in VSD NAND flash memory device, through the device simulation and measurement data of fabricated arch-shape devices.	**16:50 F-5-1** **Three Dimensional Floating Gate Memory with Multi-layered Nanodot Array Formed by Bio-LBL** *K. Ohara[1], B. Zheng[1,2], M. Uenuma[1,2], I. Yamashita[1,2] and Y. Uraoka[1,2], [1]NAIST and [2]CREST-JST (Japan)* I proposed the nanodot-type floating gate memories with multi-layered nanodot layers. Multi-layered nanodot arrays were achieved by Bio-Layer-By-Layer (Bio-LBL) method. Enlargement of memory window of memory was observed by stacking nanodot arrays.
17:05 A-5-2 **Computational Study of Electronic States around Defects in Organic Semiconductors** *T. Shimada[1], M. Ohtomo[2], T. Yanase[2] and T. Hasegawa[2], [1]Hokkaido Univ. and [2]Tokyo Univ. (Japan)* We evaluated the electronic states around defects in organic semiconductor crystals. It was found that the thermal fluctuation conceals shallow trap levels originating from defects at high temperature but the trap levels suddenly become active at lower temperatures.	**17:10 B-5-2** **Mobility Degradation and Interface Dipole Formation in Direct-Contact HfO_2/Si MOSFETs** *N. Miyata, H. Ishii, T. Itatani and T. Yasuda, AIST (Japan)* The effects of dipoles induced at direct-contact HfO_2/Si interfaces on MOSFTE characteristics was systematically investigated. Mobility degradation was observed in the direct-contact devices, which was attributed to high-k remote scattering rather than the dipole scattering.	**17:10 C-5-2** **Ultra-Thin (4nm) Gate-All-Around CMOS devices with High-k/Metal for Low Power Multimedia Applications** *J. L. Huguenin[1,2], S. Monfray[1], G. Bidal[1], S. Denorme[1], P. Perreau[3,1], N. Loubet[1], Y. Campidelli[1], M. P. Samson[3,1], C. Arvet[3,1], K. Benotmane[3], F. Leverd[1], P. Gouraud[1], B. Le-Gratiet[1], C. De-Buret[3,1], L. Pinzelli[1], R. Beneyton[1], S. Barnola[3], T. Morel[1], A. Halimaoui[1], F. Boeuf[1], G. Ghibaudo[2] and T. Skotnicki[1], [1]STMicroelectronics, [2]IMEP and [3]CEA-LETI (France)* We present the successfull integration of high-k/metal self-aligned planar Gate-All-Around with channel thickness down to 4nm. Our devices present state-of-the-art performances and excellent subthreshold characteristics thanks to its surrounding gate.	**17:05 D-5-2** **Excited State Bilayer Quantum Dot Lasers at 1.3μm** *M. A. Majid[1], D. T. D. Childs, H. Shahid, K. Kennedy, R. Airey, R. A. Hogg, E. Clarke[2], P. Spencer and R. Murray, [1]Univ. of Sheffield and [2]Imperial College (UK)* We report the realization of excited state bilayer QD lasers in the 1.31μm region,offering the opportunity for ultra-high modulation bandwidths. The extension of QD ground-state operating wavelengths to 1.45μm, spans the O and E-band.	**17:10 E-5-2** **Band Energy Engineered Metal Nanodots Nonvolatile Memory to Achieve Long Retention Characteristics** *T. Hiraki, Y. Pei, T. Kojima, J. C. Bea, H. Kino, M. Koyanagi and T. Tanaka, Tohoku Univ. (Japan)* We investigated band energy engineering of metal nanodots memories. We achieved long retention characteristics with tungsten/cobalt double stacked nanodots memory. This result was based on the difference of work-function between tungsten and cobalt.	**17:05 F-5-2** **Switching voltage reduction of resistance switching memory using Si/CaF_2/CdF_2 quantum-well structures** *M. Watanabe, Y. Nakashouji and K. Tsuchiya, Tokyo Tech (Japan)* Novel resistance switching diode using Si/CaF2/CdF2/CaF2/Si double heterostructure tunneling barriers and one quantum-well structure. Resistance switching voltage has been successfully reduced around 1V using doping control of a Si barrier layer, where 2.5 - 4V was required when using non-doped Si barrier layer.
17:20 A-5-3 **Preparation of a Hybrid Sensor of Surface Plasmon Resonance and Quartz Crystal Micorobalance by Using Imprinted Grating Structure** *K. Shinbo, K. Kuroki, Y. Tesuma, Y. Ohdaira, A. Baba, K. Kato and F. Kaneko, Niigata Univ. (Japan)* A hybrid sensor of QCM and SPR methods was prepared and its fundamental property was investigated. Grating structure of CD-R was imprinted on the QCM electrode, and the QCM and SPR property were observed simultaneously.	**17:30 B-5-3** **Robust Ultra-violet (UV) Analysis Technique for Band Diagram Extraction of Al/HfGdO/SiO_2/p-Si Structure with Different Hf/Gd Dual-sputtered Ratio** *P. C. Chou[1], J. C. Wang[1], C. S. Lai[1], J. Y. Lin[1], W. C. Chang[1], K. T. Chen[1], Y. C. Chung[1], Y. H. Lin[1], I. T. Wang[1], C. I. Wu[2] and P. S. Wang[2], [1]Chang Gung Univ. and [2]National Taiwan Univ. (Taiwan)* In this paper, we for the first time extract the energy band structure of HfGdO gate dielectric layer by using U-V analysis techniques. We successfully obtain the parameters such as energy band gap, valence band, electron affinity, Schottky barrier height, and electron effective mass of the HfGdO films.	**17:30 C-5-3** **Heavily-Doped Poly-Si Gate and Epi-First Source/Drain Extension Technique in Strained Si Nanowire MOSFETs with Reduced Papasitic Resistance** *Y. Nakabayashi[1], M. Saitoh[1], T. Ishihara[1], T. Numata[1], K. Uchida[2] and J. Koga[1], [1]Toshiba Corp. and [2]Tokyo Inst. of Tech. (Japan)* Parasitic resistance reduction and current drive enhancement were achieved in nanowire filed-effect-transistors with Epi-first process and compressive stress induced by heavily-doped poly-Si gate. 20% current drive enhancement was obtained compared to conventional process. Heavily-doped poly-Si gate process is additive to the tensile stress liner.	**17:20 D-5-3** **A tunnel injection structure for speeding up carrier dynamics in InAs/GaAs quantum dots using a GaNAs quantum-well injector** *C. Y. Jin[1], S. Ohta, M. Hopkinson[2], O. Kojima[1], T. Kita and O. Wada, [1]Kobe Univ. and [2]Univ. of Sheffield (Japan)* A tunnel injection structure has been employed to speeding up carrier dynamics in InAs/GaAs quantum-dots (QD) with a GaAsN quantum well (QW) as a carrier injector. The carrier capture time from the GaAsN QW to QD ground states has been evaluated by time-resolved photoluminescence.		**17:20 F-5-3** **Time dependent analysis of the applied voltage operation for ensuring 10-year lifetime with SiN MOSFET noise source device** *M. Matsumoto, T. Tanamoto, S. Yasuda, R. Ohba and S. Fujita, Toshiba Corp. (Japan)* We have theoretically evaluated long-term change in device characteristics of SiN MOSFET from device measurement data on short-term change. It has been found that, to improve the endurance, it is necessary to preclude electron trapping at deep levels by shortening.

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G-4: Advanced Analog Circuits (Area 5)	**H-4: Carbon Interconnect (Area 2)**	**I-4: Silicon Carbide Devices (Area 6)**	**J-4: Graphene's Electrical Properties (Area 13)**	**K-4: Next Generation Solar Cells (Area 14)**	
Coffee Break (2F Forum)					
G-5: Integrated MEMS/Bio Sensors (Area 5 & 11) (16:50-18:05) Chairs: H. Toshiyoshi (Univ. of Tokyo) K. Sawada (Toyohashi Univ. of Tech.)	**H-5: Cu/Low-k Integration (Area 2)** (16:50-18:00) Chairs: S. Matsumoto (Panasonic Corp.) T. Hasegawa (Sony Corp.)	**I-5: Oxide Devices (Area 6)** (16:50-17:50) Chairs: S. Sasa (Osaka Inst. of Tech.) T. Hashizume (Hokkaido Univ.)	**J-5: Graphene Devices(Area 13)** (16:50-18:05) Chairs: K. Ishibashi (RIKEN) S. Sato (AIST)	**K-5: Compound Semiconductor Solar Cells (Area 14)** (16:50-18:05) Chairs: A. Yamada (Tokyo Tech) T. Minemoto (Ritsumeikan Univ.)	
16:50 G-5-1 (Invited) **Integrated CMOS-MEMS Technology and its Application.** *K. Machida and H. Morimura, [1]NTT AT and [2]NTT Microsystem Integration Laboratories (Japan)* The paper describes the integrated CMOS-MEMS technology and its applications. We discuss the features of the technology. MEMS fingerprint sensor and Low-voltage RF CMOS-MEMS switch are demonstrated as the applications.	**16:50 H-5-1 (Invited)** **Advanced Organic Polymers for the Aggressive Scaling of Low-k Materials** *M. Pantouvaki[1], L. Zhao[2], C. Huffman[1], N. Heylen[1], Y. Ono[3], M. Nakajima[3], K. Nakatani[3], G. P. Beyer[1] and M. R. Baklanov[1], [1]IMEC, [2]Intel Corp. and [3]Sumitomo Bikelite Co., Ltd. (Belgium)* In this paper the scalability of an organic polymer of k-value of 2.2 is studied in single damascene structures with dielectric spacings ranging from 75 to 30 nm, both with and without Cu diffusion barriers.	**16:50 I-5-1** **High-Mobility a-IGZO Thin-Film Transistor Using Ta_2O_5 Gate Dielectric** *C. J. Chiu, S. P. Chang, C. Y. Lu and S. J. Chang, National Cheng Kung Univ. (Taiwan)* In this paper, we have reported the high performance of an amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor with a high-k dielectric layer on a glass substrate.	**16:50 J-5-1** **Label-Free Immunosensors Based on Aptamer-Modified Graphene Field-Effect Transistors** *Y. Ohno, K. Maehashi and K. Matsumoto, Osaka Univ. (Japan)* Aptamer-modified G-FETs were successfully fabricated for label-free immunosensors. IgE aptamers can be immobilized on the graphene surface using linker, which was confirmed by AFM and electrical characteristics. The aptamer-modified G-FETs were electrically detected only target IgE molecules.	**16:50 K-5-1 (Invited)** **Flexible Cu(In,Ga)Se_2 Thin Film Solar Cells and Challenges for Low Temperature Growth** *C. A. Kaufmann, R. Caballero, T. Rissom, T. Eisenbarth, T. Unold, R. Klenk and H. W. Schock, Helmholtz Zentrum Berlin für Materialien und Energie (Germany)* Flexible Cu(In,Ga)Se2 (CIGSe) thin film solar cells attract growing interest. Due to light weight, robustness and low cost they are expected to increase the range of terrestrial and space applications. The talk focuses on the fabrication of CIGSe at low process temperatures and the challenges related to this approach.	
17:20 G-5-2 **Polarization Analyzing Image Sensor with Monolithically Embedded Polarizer using 65nm CMOS Process** *S. Shishido, T. Noda, K. Sasagawa, T. Tokuda and J. Ohta, NAIST (Japan)* The polarization analyzing sensor is expected to be a solution for analyses of optically active compounds. We designed a polarization analyzing image sensor using 65nm CMOS process. By this sensor, polarization characteristics are successfully measured.	**17:20 H-5-2** **DMOTMDS/MTMOS Multi-Stacked SiOCH films for Super-Low-k and Sufficient Modulus Formed by Damage-free Neutral Beam Enhanced CVD** *T. Sasaki[1], S. Yasuhara[1], T. Shimayama[2], K. Tajima[2], H. Yano[2], S. Kadomura[2], M. Yoshimaru[2], N. Matsunaga[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]STARC (Japan)* Multi-stacked film was successfully fabricated by depositing lower k-value and higher modulus layers alternately. By optimizing multi-stacked film, we could obtain a super low-k film with k-value of 1.8 and sufficient modulus of 7Gpa simultaneously.	**17:05 I-5-2** **ZnO thin film fabricated by plasma assisted atomic layer deposition** *Y. Kawamura[1] and Y. Uraoka[1,2], [1]NAIST and [2]CREST-JST (Japan)* In this study, we fabricated ZnO thin-films using plasma-assisted ALD to improve the performance. Excellent properties were obtained. The effects of plasma condition on film properties were also investigated.	**17:05 J-5-2** **Performance Evaluation of Graphene Nanoribbon Heterojunction Tunneling Field Effect Transistors with various Source/Drain Doping Concentration and Heterojunction structure** *H. Da[1], K. T. Lam[1], S. K. Chin[2], G. S. Samudra[1], Y. C. Yeo[1] and G. Liang[1], [1]National Univ. of Singapore and [2]Institute of High Performance Computing (Singapore)* The influence of doping concentration and geometrical parameters on the current-voltage characteristics of HJ GNR TFETs has been theoretically investigated by performing Dirac NEGF approach. It is shown that ION as well as SS can be enhanced by controlling the doping concentration and geometrical parameters.	**17:20 K-5-2** **First principles calculations of defect formation in In-free photovoltaic semiconductors Cu_2ZnSnS_4 and $Cu_2ZnSnSe_4$** *T. Maeda, S. Nakamura and T. Wada, Ryukoku Univ. (Japan)* We calculate the vacancy formation energy in Cu2ZnSnSe4 (CZTSe), and Cu2ZnSnSe4 (CZTS) by first-principles calculation. We compare the defect formation in In-free photovoltaic semiconductors CZTSe and CZTS with that of CuInSe2.	
17:35 G-5-3 **Design and Fabrication of Smart All-in-one Chip for Electrochemical Measurement** *T. Yamazaki[1,2], T. Ikeda[1], M. Ishida[1,3] and K. Sawada[1,3], [1]Toyohashi Univ. of Tech., [2]HIOKI E.E. E. Corp. and [3]JST-CREST (Japan)* An electro-chemical sensor chip with a signal input circuit, a potentiostat and sensor electrodes incorporated was designed and fabricated for the first time. Cyclic voltammetry was demonstrated to acquire electrochemical signals using well-studied ferricyanide solution.	**17:40 H-5-3** **Improvement of Variability and Reliability in Low-k/Cu Interconnects by Selectivity Control in Dry-Etching Process** *I. Kume, M. Ueki, N. Inoue, J. Kawahara, N. Ikarashi, N. Furutake, S. Saitoh and Y. Hayashi, Renesas Electronics Corp. (Japan)* As dimension of the LSI scales down, precise control of the patterning profile in low-k films becomes a key to keep high reliability and small variability in Cu dual damascene interconnects. Carbon-rich MPS-SiOCH film, along with control of the etching gas, achieved highly selective RIE processes for small variability and high reliability.	**17:20 I-5-3** **The Unique Phenomenon in the Amorphous In_2O_3-Ga_2O_3-ZnO TFTs Degradation under the Dynamic Stress** *M. Fujii[1], J. S. Jung[2], J. Y. Kwon[2] and Y. Uraoka[1,3], [1]NAIST, [2]Samsung Advanced Inst. of Tech. and [3]CREST-JST (Japan)* We investigated the degradation of a-IGZO TFTs caused by the AC stress. We found that the S value change under the AC stress and this degradation caused by the Negatively-charged Donor like traps.	**17:20 J-5-3** **Impact of Surface Treatment of SiO_2/Si Substrate on Mechanically Exfoliated Graphene** *T. Yamashita, J. Fujita, K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)* The interaction between graphene and SiO_2 surface is critical to improve the mobility as well as the size of graphene. We study the effect of O_2 plasma treatment for SiO_2 surface on the interaction.	**17:35 K-5-3** **Kinetics of strain relaxation in lattice-mismatched $In_xGa_{1-x}As$/GaAs heteroepitaxy** *T. Sasaki[1], H. Suzuki[2], M. Takahasi[3], S. Fujikawa, I. Kamiya[1], Y. Ohshita and M. Yamaguchi, [1]Toyota Tech. Inst., [2]Univ. of Miyazaki and [3]JAEA (Japan)* In situ X-ray reciprocal space mapping during lattice-mismatched In0.08Ga0.92As/GaAs(001) growth and growth interruption is performed to investigate the extent to which the strain relaxation process is kinetically limited.	

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A-5: Organic Electronics and Device Physics (Area 10)	**B-5: Advanced Gate Dielectrics (Area 1)**	**C-5: Si Nanowire Technology (Area 3)**	**D-5: Quantum Dot (Area 7)**	**E-5: Flash Memory Ⅳ (Area 4)**	**F-5: New Functional MOS Structures (Area 9)**
17:35 A-5-4 (Late News) **Nonvolatile memory thin film transistors using triple polymeric dielectric layers** *Y. C. Chen[1], C. Y. Huang[2], C. Y. Cheng[1], H. C. Yu[1], Y. K. Su[1] and T. H. Chang[1], [1]National Cheng Kung Univ. and [2]National Taitung Univ. (Taiwan)* The nonvolatile memory OTFTs with triple dielectric layers have been demonstrated. In our device configuration, the memory effect originates from the charges stored in the interfaces between the dielectric layers and in the -OH groups inside the polymer dielectrics. The transistors have a switchable channel current and long retention time.	**17:50 B-5-4** **Stability origin of metastable higher-k phase HfO_2 at room temperature** *Y. Nakajima, K. Kita, T. Nishimura, K. Nagashio and A. Toriumi, Univ. of Tokyo (Japan)* The stability origin of the metastable higher-k phase HfO2, and a plausible mechanism of Si-cap PDA to obtain that phase were investigated.	**17:50 C-5-4** **Low GIDL and Its Physical Origins in Si Nanowire Transistors** *K. Zaitsu, M. Saitoh, Y. Nakabayashi, T. Ishihara and T. Numata, Toshiba Corp. (Japan)* Gate-induced drain leakage (GIDL) in Si nanowire transistors fabricated on SOI substrates is systematically studied. GIDL current is drastically reduced in nanowire FETs with the nanowire width of around 10 nm, which realizes extremely small off-current devices.	**17:35 D-5-4 (Late News)** **Stimulated Emission in Silicon Fin Light-Emitting Diode** *S. Saito[1,3], K. Tani[1,3], T. Takahama[1], M. Takahashi[1], E. Nomoto[1], Y. Matsuoka[1], J. Yamamoto[2,3], Y. Suwa[1], D. Hisamoto[1], S. Kimura[1], H. Arimoto[1,3], T. Sugawara[1], M. Aoki[1], K. Torii[1] and T. Ido[1,3], [1]Hitachi, Ltd., Central Res. Lab., [2]Hitachi Advanced Res. Lab. and [3]PECST (Japan)* We have proposed a Si fin light-emitting diode to realize multiple quantum wells fabricated by Si technologies. The experimental results demonstrate the excellent transport characteristics and efficient electroluminescence in the infrared regime.		**17:35 F-5-4** **Strong Stark effect of electroluminescence in thin SOI MOSFETs** *J. Noborisaka, K. Nishiguchi, Y. Ono, H. Kageshima and A. Fujiwara, NTT Corp. (Japan)* We report electroluminescence from thin SOI MOSFETs when electrons are injected into a thin SOI layer. We observed a large Stark shift of up to approximately 50 meV by applying an electric field normal to the thin SOI layer. Stark effect indicates that quantum confinement in the Si/SiO2 system plays an important role in light emission.
17:50 A-5-5 (Late News) **Passivation Effect of Diamond Like Carbon Films for Organic Light-Emitting Diodes** *H. Butou, H. Okada and S. Naka, Univ. of Toyama (Japan)* We have studied OLEDs with double-layered inorganic/ DLC as a passivation films. By adding the MoO3 as passivation layer for reducing plasma damage, identical durability that compared to the glass encapsulation was observed.			**17:50 D-5-5 (Late News)** **Effects of tunneling barrier width on the electrical characteristic in Si-QD LEDs** *T. Y. Kim[1,3], N. M. Park[1], C. J. Choi[2], C. Huh[1], C. G. Ahn[1], G. Y. Sung[1], I. K. You[1] and M. Suemitsu[3], [1]Electronics and Telecommunications Res. Inst., [2]Univ. of Chonbuk and [3]Tohoku Univ. (Korea)* In this work, we investigated the impacts of nitride source on the electrical properties of the Si-QD LEDs. Two nitrogen sources, nitrogen (N2) and ammonia (NH3), have been compared for the PECVD growth of the silicon nitride film, while silane (SiH4) has been commonly used as the silicon source.		**17:50 F-5-5** **Drive Current Enhancement with Invasive Source in Double Gate Tunneling Field-Effect Transistors** *Y. Yang, P. F. Guo, G. Q. Han, C. L. Zhan, L. Fan and Y. C. Yeo, National Univ. of Singapore (Singapore)* We studied the dependence of TFET performance on source design using a 2D TCAD simulation tool. Use of an invasive source with an optimized shape could be used to realize an increased tunneling region, giving a higher Ion. Applying the invasive source in Ge-source Si-body TFET can further enhance the device performance.

Rump Session (Sanjo Conference Hall)

Rump Sessions (18:30-20:00)

Session A (1st Floor)
"Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?"
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

Session B (Basement Floor)
"Silicon Solar Cells -Their key technologies and future prospects-"
Organizer: T. Fukui, (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech) , A. Masuda (AIST)

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4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-5: Integrated MEMS/Bio Sensors (Area 5 & 11)	**H-5: Cu/Low-k Integration (Area 2)**	**I-5: Oxide Devices (Area 6)**	**J-5: Graphene Devices(Area 13)**	**K-5: Compound Semiconductor Solar Cells (Area 14)**	
17:50 G-5-4 **Amperometric Electrochemical Sensor Array for On-Chip Simultaneous Imaging: Circuit and Microelectrode Design Considerations** *J. Hasegawa, S. Uno and K. Nakazato, Nagoya Univ. (Japan)* We introduce amperometric sensor circuit array for rapid and simultaneous electrochemical imaging, and also propose a novel microelectrode structure to reduce the time to reach the steady-state current, which is verified by computer simulation.		**17:35 I-5-4** **Novel Passivation Layer for Improvement of Reliability In Amorphous Indium Gallium Zinc Oxide Thin Film Transistors (TFTs)** *S. H. Choi, Y. W. Lee, J. Y. Kwon and M. K. Han, Seoul National Univ. (Korea)* We have proposed and fabricated the a-IGZO TFTs with novel passivation layer consisting of sub-layers with different substrate temperatures. And we have verified that the proposed device could improve bias-illumination stability and enhance the electrical characteristics of a-IGZO TFTs.	**17:35 J-5-4** **Graphene based transversal-gated field effect transistor due to band gap modulation** *S. B. Kumar, T. Fujita and G. Liang, National Univ. of Singapore (Singapore)* We explore a transversal-gated-FET in which an asymmetric electrochemical potential is applied. This potential causes a reduction in the band gap of the AGNR, thus resulting in larger current flow across the device. The device performance is improved by introducing vacancies at the top edge. **17:50 J-5-5 (Late News)** **Effect of Oxidation-induced Tensile Strain on Gate-all-Around Silicon Nanowire Based Single-electron Transistor Fabricated using Optical Lithography** *Y. Sun[1,2], Rusli[1] and N. Singh[2], [1]Nanyang Tech. Univ. and [2]Inst. of Microelectronics (Singapore)* Room temperature silicon nanowire-based single electron transistor was fabricated using optical lithography. Coulomb oscillation is weakened for SiNWs of shorter length, attributed to the lowering of the tunneling barriers due to reduced oxidation-induced tensile strain.	**17:50 K-5-4** **Numerical Analysis of a Solar Cell with a Tensile-Strained Ge as a Novel Narrow Band Gap Absorber** *Y. Hoshina, M. Shimizu, A. Yamada and M. Konagai, Tokyo Tech (Japan)* The solar cell performances of the InGaAs /tensile-strained Ge/ InGaAs double-hetero structure are numerically demonstrated as a thin, low-cost, and lattice-adjustable narrow band gap absorber in future multijunction solar cells.	

Rump Session (Sanjo Conference Hall)

Rump Sessions (18:30-20:00)

Session A (1st Floor)
"Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?"
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

Session B (Basement Floor)
"Silicon Solar Cells -Their key technologies and future prospects-"
Organizer: T. Fukui, (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech) , A. Masuda (AIST)

POSTER SESSION (13:15-14:45, Takeda Bldg.)

Area 1: Advanced Si Processing & Materials Science

(26 Papers)

P-1-1

Strained Si with Smooth and Uniformly Strained Surface Formed by Sputter Epitaxy

H. Hanafusa[1], N. Hirose[2], A. Kasamatsu[2], T. Mimura[2], T. Matsui[2], H. M. H. Chong[3], H. Mizuta[3] and Y. Suda[1], [1]Tokyo Univ. of Agri. And Tech., [2]National Inst. of Info. and Commun. Tech. and [3]Univ. of Southampton (Japan)

Strained Si formed by our sputter epitaxy shows a smoother and more uniformly strained surface than with GS-MBE, which has been first clarified on the nanometer scale with a combination of AFM and Enhanced-Raman Spectroscopy.

P-1-2

Enhancement of Stress Memorization Technique (SMT) by High Thermal Annealing Temperature

H. Y. Chang and J. C. S. Woo, University of California, Los Angeles (USA)

In this paper, different annealing temperature at gate memorizing strain step is studied. Device performance shows SMT device with higher annealing temperature (1150ºC) can induce more strain memorized in the gate. The experimental data of SMT device with higher annealing temperature shows significant improvement of electron mobility compared to lower annealing temperature (1000ºC).

P-1-3

Evaluation of Si/SiO_2 Interface Properties for CMOS Fabricated on Hybrid Orientation Substrate with Amorphization/Templated Recrystallization Method

P. C. Huang[1], S. L. Wu[2], S. J. Chang[1], J. F. Chen[1], Y. T. Huang[1], D. G. Hong[2], C. Y. Chang[1], C. Y. Wu[2], C. T. Lin[3], M. Ma[3] and O. Cheng[3], [1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]UMC (Taiwan)

For the HOT substrates, we find that ATR-induced defects on (100) regions can be repaired further by extending defect-removal annealing time, and no appreciable impact on (110) regions is observed.

P-1-4

Efficient Activation of As in Ultrashallow Junction Induced by Thermal Plasma Jet Microsecond Annealing

K. Matsumoto, S. Higashi, H. Murakami and S. Miyazaki, Hiroshima Univ. (Japan)

We carried out generation of high power density TPJ for microsecond RTA by using an orifice of 0.8 mm diameter instead of 2.0 mm to concentrate TPJ and could be annealing a range of microsecond annealing. We activated As in Si wafers by this annealing technique using μ-TPJ and could be efficient activation of As in comparison to TPJ irradiation.

P-1-5

Depth Profile and Retained Dose in SiO_2/Si Structure for $B_{18}H_X^+$ Implantation

Y. Kawasaki[1,2], H. Yoshimura[1], K. Asai[1] and K. Shibahara[2], [1]Renesas Electronics Corp. and [2]Hiroshima Univ. (Japan)

Retained dose for $B_{18}H_X^+$ implantation and surface sputtering was investigated. The surface sputtering was negligible for both SiO_2 and Si. However the retained boron dose remarkably decreased due to the surface SiO_2.

P-1-6

Effects of Al Incorporation into Pr-oxides Formed by Atomic Layer Deposition

K. Furuta, W. Takeuchi, M. Sakashita, K. Kato, H. Kondo, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)

We examined PAO layers on Si substrates with ALD method and investigated the crystalline and electric properties. The oxide trap density and interface state density decrease by incorporation of Al into Pr oxide.

P-1-7

Analysis of Local Leakage Current of Pr Oxide Thin Films with Conductive Atomic Force Microscopy

M. Adachi, M. Sakashita, H. Kondo, W. Takeuchi, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)

We have investigated local leakage current in Pr oxide films by using C-AFM. We considered that leakage spots observed in C-AFM current images is strongly related to oxygen vacancy in the Pr oxide films.

P-1-8

In-situ Formation of HfN/HfSiON Gate Stacks with 0.5 nm EOT Utilizing ECR Sputtering on Three-Dimensional Si Structures

T. Sano and S. Ohmi, Tokyo Tech (Japan)

In-situ formation of HfN/HfSiON gate stacks by ECR sputtering was investigated. Annealing temperature was important parameter and the temperature of 600°C is suitable to suppress the D_{it} and the frequency dispersion.

P-1-9

The Influence of La and Zr Doping on TDDB Characteristics of HfO_2 Thin Films

H. W. Chen[1], C. H. Liu[2], S. Y. Chen[1], Y. W. Liao[1], H. W. Hsu[1], H. S. Huang[1] and L. W. Cheng[3], [1]National Taipei Univ. of Tech., [2]National Taiwan Normal Univ. and [3]UMC (Taiwan)

Although time-dependent-dielectric-breakdown (TDDB) reliability is one major concern in advanced technology, it has not yet been fully understood for Hf-based high-κ dielectrics, especially La-incorporated HfZrO2 (HfZrLaO) thin films.

P-1-10

Temperature Dependence of Exclusive SiO_2Formation during Thermal Oxidation of Si_{1-X} Ge_X Alloy Layer on Si(001) Surfaces

H. Hozumi[1], S. Ogawa[1], A. Yoshigoe[2], S. Ishidzuka[3], J. R. Harries[2] and Y. Teraoka[2], Y. Takakuwa[1], [1]Tohoku Univ., [2]JAEA and [3]Akita Nat. Col. Tech. (Japan)

Qpix v.1 possesses 400 pixels and compact readout structure to guarantee that all stored data in the pixels can be read out in 2.6 μs in parallel mode and 54 μs in serial mode. A charge collection pad is included in each pixel to realize large area applications. The SAR ADC in each pixel is optimized to 10 bit 10 MSps without area increase. The power consumption has been reduced to 187.5 μW/pixel.

P-1-11

Fabrication of Ge-MOS Capacitors with High-Quality Interface by Ultra-Thin SiO_2/GeO_2 Bi-Layer Passivation

K. Hirayama, R. Ueno, Y. Iwamura, K. Yoshino, D. Wang, H. Yang and H. Nakashima, Kyushu Univ. (Japan)

We established an effective electrical passivation method of Ge surface by ultra-thin SiO_2 /GeO_2 bi-layer. By using this method, we achieved the density of interface states of 3.7×10^{11} cm^{-2} eV^{-1} at around midgap for MOS capacitors.

P-1-12

Improvement of The Property of FET Having The HfO_2/Ge Structure Fabricated by Photo-Assisted MOCVD with Fluorine Treatment

D. Lee, H. Imajo, T. Kanashima and M. Okuyama, Osaka Univ. (Japan)

This paper describes about improvement of The HfO_2/Ge MISFET device by fluorine treatment. The device was treated by F_2 gas before each HfO_2 deposition on the few bottom layers. Therefore, we were able to fabricate a high speed Ge-based MISFET device.

P-1-13

Study on Native Oxidation of Ge (111) and (100) Surfaces

S. K. Sahari, H. Murakami, T. Fujioka, T. Bando, A. Ohta, K. Makihara, S. Higashi and S. Miyazaki, Hiroshima Univ. (Japan)

We have studied the growth of native oxides on HCl-last and HF-last Ge surfaces and examined the influence of crystallographic orientation and conduction type on the native oxidation.

P-1-14

Annealing Effects on Ge/SiO_2 interface Structure in wafer-bonded germanium-on-insulator substrates

O. Yoshitake[1], J. Kikkawa[1], Y. Nakamura[1], A. Sakai[1], E. Toyoda[2], H. Isogai[2] and K. Izunome[2], [1]Osaka Univ. and [2]Covalent Silicon Co., Ltd. (Japan)

We have investigated annealing effects on Ge/SiO^2 interfaces in wafer-bonded Germanium (Ge) on Insulator (GOI) substrates using transmission electron microscopy and electron energy-loss spectroscopy.

P-1-15

Electrical characterization of wafer-bonded germanium-on-insulator substrates using a four-point-probe pseudo-MOSFET

Y. Iwasaki[1], Y. Nakamura[1], J. Kikkawa[1], A. Sakai[1], M. Sato[2], E. Toyoda[2], H. Isogai[2] and K. Izunome[2], [1]Osaka Univ. and [2]Covalent Silicon Co., Ltd. (Japan)

The electrical characteristics of wafer-bonded GOI substrates were investigated using a pseudo-MOSFET. Annealing process in vacuum strongly influenced their electrical characteristics, which is explained by defect-induced energy band bending near the interface.

P-1-16

New Concept of Plasma-induced Damage in MNOS FET during Thick Dielectric Film Etching Using Fluorocarbon Gas Plasma

Y. Ichihashi, Y. Ishikawa and S. Samukawa, Tohoku Univ. (Japan)

We investigated the mechanism of damage by perfluorocarbon gas plasma. We found that charged carriers in SiO2 film were generated by UV irradiation of CF4 plasma and were trapped at Si dangling bonds.

P-1-17

A Novel Hot DI Water Rinse on SOD Filled Self-Aligned Shallow Trench Isolation for Highly Reliable NAND Flash Memory

C. H. Liu, Y. M. Lin, R. T. Peng, H. C. Wei, H. J. Chien, Y. T. Chiu, L. T. Kuo, H. P. Hwang, M. S. Lee and S. Pittikoun, Powerchip Semiconductor Corp. (Taiwan)

Significant improvements on 42nm node NAND flash memory with SOD filled STI by hot deionized water rinse technology: (1) Most good block ratio can be increased > 15%. (2)Better endurance/ retention: 0.37V less cell Vth shift after 10k cycling and 36.7% less Vt shift by retention test. (2) Stress induced leakage current life time is extended 54%.

P-1-18

High-Performance Poly-Si TFTs with Novel FinFet-like Channel

Y. H. Lue, P. Y. Kuo, Y. H. Wu and T. S. Chao, National Chiao Tung Univ. (Taiwan)

High performance TFTs with novel FinFet-like channel structure (called FL-TFTs) exhibit VTH~0.5V, good S.S.~ 240mV/dec. and high Iratio>107 without any hydrogen-related plasma treatments. Ni-salicidation and hydrogen-related plasma treatments further enhance S.S. to 190 mV/dec. and Iratio>108.

P-1-19

Fluorescence XAFS analysis of thermal stability for Ru/HfSiON/SiON/Si gate stack structure

H. Ofuchi[1], H. Kamada[2], S. Toyoda[2,3,4], H. Kumigashira[2,3,4], T. Sukegawa[5], K. Iwamoto[5], Z. Liu[5] and M. Oshima[2,3,4], [1]JASRI, [2]Univ. of Tokyo, [3]UT-SRRO, [4]JST-CREST and [5]STARC (Japan)

Thermal stability of geometric structures for Ru/HfSiON/SiON/Si films was investigated by fluorescence XAFS. The XAFS analysis has revealed that the appropriate annealing condition prevent the oxidation and silicidation of the metal gate Ru layer.

P-1-20

Strain and stress tensor evaluation in global and local strained-Si by electron back scattering pattern

M. Tomita[1], D. Kosemura[1,2], M. Takei[1], K. Nagata[1], H. Akamatsu[1] and A. Ogura[1], [1]Meiji Univ. and [2]Research Fellow of the JSPS (Japan)

SSOI and Si substrates with patterned SiN films were evaluated by EBSP. Shear stresses were observed in both of the samples. Clear two-dimensional stress distribution was obtained, which was comparable to that obtained by UV-Raman.

P-1-21

Development of an STM simulator for quantitative dopant profiling

M. Nishizawa[1,2], L. Bolotov[2], T. Tada[1,2], H. Fukutome[2], H. Arimoto[2] and T. Kanayama[1,2], [1]MIRAI-AIST and [2]NIRC-AIST (Japan)

In order to realize quantitative dopant profiling by STM, we developed an STM simulator. Our simulation reproduced the experimental topographic profile and I-V curves obtained at a p-n junction.

P-1-22 (Late News)

Many-electron charge transfer multiplet theory: O-atom vacancies in high-k dielectrics

G. Lucovsky, L. Miotti and K. Paz Bastos, North Carolina State Univ (USA)

Soft X-ray absorption and photoemission spectroscopies (XAS and XPES) have been used to study conduction band edge, and O-vacancy defect states in HfO2.The d-state occupancy in O-vacancy d^2 defects is described Tanabe-Sugano diagrams for d to d' transitions forthe excited states of these defects, as well as the negative ion states which act as electron traps

P-1-23 (Late News)

Momentum Transfer Implantation for Sidewall Doping of FinFET's

G. Fuse[1], M. Sugitani[1], H. Matsushita[1], H. Murooka[1], M. Kuriyama[2] and M. Tanaka[2], [1]SEN corporation and [2]Sumitomo Heavy Industry (Japan)

As new doping technique into FinFET sidewalls, Momentum Transfer Implantation (MTI) is introduced. MTI consists of two processes; dopant film deposition and grazing angle implantation by heavy ions. Simulation and experiment results will be reported.

P-1-24 (Late News)

MIM Capacitors with Stacked TiO_2/Y_2O_3 Insulator Featuring High Capacitance Density and Low Leakage Current

C. C. Lin, Y. C. Hu, L. L. Chen, M. L. Wu, J. R. Wu and Y. H. Wu, National Tsing Hua Univ. (Taiwan)

High-κ dielectrics have been perceived as the enabling technology to implement high performance radio frequency and analog metal-insulator-metal (MIM) capacitors. Applications of HfO2 and ZrO2-based materials to MIM capacitors have been extensively studied.

P-1-25 (Late News)

Fabrication of hp 25nm Si Pillar Using New Multiple Double Patterning Technique

M. Kushibiki[1,4], A. Hara[2,4], E. Nishimura[1,4] and T. Endoh[3,4], [1]Tokyo Electron AT Ltd., [2]Tokyo Electron Ltd., [3]Tohoku Univ. and [4]JST-CREST (Japan)

Novel method to fabricate hp 25nm pitch dense Si pillar that would apply to the fabrication of vertical cell devices was developed. By using proposed multiple double patterning technique, the hp25 Si pillar etching profile has enough uniformity in 300mm wafer.

P-1-26 (Late News)
Effect of Valence State of Pr on Interfacial Structure and Electrical Properties of Pr-oxide/PrON/Ge Gate Stack Structure
K. Kato, M. Sakashita, W. Takeuchi, H. Kondo, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)
We investigated the relationship between the electrical properties and the valence state of Pr in Al/Pr-oxide/PrON/Ge stacked structures, and discussed the importance of controlling the chemical bonding structure to suppress degradation of MOS characteristics.

Area 2: Advanced Interconnect /3-D Integration Science
(10 Papers)

P-2-1
Development of Versatile Backside Via Technology for 3D System on Chip
Y. Ohara, K. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We develop several key technologies in backside via to realize 3D LSIs. We apply them to a test chip with daisy chain. Fine sized Cu TSVs in diameter 10 μm and 30 μm depth are successfully formed.

P-2-2
RF Modeling of Through Silicon Vias (TSVs) in 3D IC
C. W. Luo, Y. C. Wu and J. Y. Wang and S. S. H. Hsu, National Tsing Hua Univ. (Taiwan)
This paper proposed the TSV one-port test structures to extract the physical-based equivalent circuit model. The differences of S21 and S11 between the EM-simulation and the model are smaller than 0.03 dB and 2 dB.

P-2-3
Stress Mapping of Silicon Surrounded by Various Through Silicon Via (TSV) Patterns using Polychromator-Based Multi-Wavelength Raman Spectroscopy
A. D. Trigg[1], L. H. Yu[1], C. C. Kuo[1], R. Kumar[1], D. L. Kwong[1], T. Ueda[2], T. Ishigaki[2], K. Kang[2] and W. S. Yoo[2], [1]Insitute of Microelectronics and [2]WaferMasters, Inc. (Singapore)
We have studied the stress distribution in Si surrounded by TSVs, with various dimensions and pitches, to understand the potential impact of TSV layouts on device performance and reliability. The stress measurement and 3D stress mapping was successfully demonstrated using a polychromator-based, multi-wavelength Raman spectroscopy (MRS-300) system.

P-2-4
Above-CMOS Metal-Pattern Technique for Flexible Inductance Adjustment in Rapid Prototyping of RF SoCs
K. Kotani, A. Sugimoto, Y. Omiya and T. Ito, Tohoku Univ. (Japan)
Very simple yet flexible inductance adjustment scheme has been developed using above-CMOS metal pattern formation for rapid prototyping of RF SoCs. Above-CMOS simple processing with chip-by-chip manner can both increase and decrease the on-chip inductances.

P-2-5
Modeling and Co-Design of Novel Packaging Interposer with IPD Layers
S. M. Wu[1], T. Y. Wu[1], B. H. Yu[1] and C. C. Wang[2], [1]National Univ. of Kaohsiung and [2]Electrical Lab., Corp. Design Division, Corporate R&D, Advanced Semiconductor Engineering (ASE) Inc., Kaohsiung (Taiwan)
Two innovations topics will be presented in this research. First, structure of packaging interposer with IPD layers is proposed and broad-band equivalent model of TSV will be extracted too. Second, co-design case, coplanar waveguide transfer layers from top to bottom by TSV, is simulated by equivalent model we performed and compared with full wave EM simulation.

P-2-6
Multi-Line De-Embedding Technique for Millimeter-Wave Circuit Design
Q. H. Bu, N. Li, N. Takayama, K. Okada and A. Matsuzawa, Tokyo Tech (Japan)
A multi-line de-embedding method has been proposed up to millimeter wave. The de-embedding procedure is explained in the paper. Experimental results using the proposed method is shown.

P-2-7
Numerical Simulation of Organic Low-*k* Etching in H_2/N_2 Plasma
T. Yagisawa[1] and T. Makabe[1], Keio Univ. (Japan)
Organic low-k material is one of the promising solutions for RC signal delay problem in the multilayer interconnect. The characteristics of organic low-k film by using H_2/N_2 plasma has been numerically investigated.

P-2-8
Smooth Patterning of Ru Film by Electrochemical Etching using Organic based Solution
L. Yang[1], R. Sakae[1], M. Yashimaru[2], M. Yamaguchi[2], I. Kanno[2], M. Tanaka[2], C. Kimura[1] and H. Aoki[1], [1]Osaka Univ. and [2]STARC (Japan)
In this paper, to avoid the bubbles generation and having smooth etching area, we have proposed an etching of Ru film using electrochemical etching in the organic based solution.

P-2-9
Effect of Annealing on Electrical Properties of Networked-Nanographite Wire Grown by Metal-Photoemission-assisted Plasma-enhanced CVD
M. Sato[1,2,3], S. Ogawa[3,4], T. Kaga[4], E. Ikenaga[3,5], Y. Takakuwa[3,4], M. Nihei and N. Yokoyama[2], [1]Fujitsu Ltd., [2]Fujitsu Labs Ltd., [3]CREST-JST, [4]Tohoku Univ. and [5]JASRI (Japan)
The annealing effect on the electrical properties of networked-nanographite (NNG) wires has been investigated using a TEM, Raman spectroscopy and resistivity measurement. The resistivity of NNG decreases as the annealing temperature increases.

P-2-10
In Situ High-Resolution Transmission Electron Microscopy of Electromigration in Silver Nano-contacts
H. Masuda and T. Kizuka, Univ. of Tsukuba (Japan)
EM in Ag NCs was directly observed by in situ TEM. The relationships between the structural modification, current density and stress were simultaneously analyzed. The threshold bias voltage was ~100 mV . In this experiment, we in situ observed the thinning process of the NCs.

Area 3: CMOS Devices / Device Physics
(22 Papers)

P-3-1
Experimental Investigations on Ballistic Transport in Multi-Bridged Channel Field Effect Transistors (MBCFETs)
Y. C. Jung[1], B. H. Hong[1], L. Choi[1], S. W. Hwang[1], K. H. Cho[2], S. Y. Lee[2], D. W. Kim[2], G. Y. Jin[2] and K. S. Oh[2], [1]Korea Univ. and [2]Samsung Electronics Co., Ltd. (Korea)
We present the experimental evidences of ballistic transport in MBCFET by investigating the device characteristics as a function of the gate length ranging from 48 to 500nm and temperature ranging from 300 to 4K.

P-3-2
The Effects of Quantum Confinement on Electrical Characteristics of 12-nm Silicon-on-Insulator (SOI) FinFETs by Quantum Transport Analysis
K. M. Liu, National Dong Hua Univ. (Taiwan)
The quantum confinement effects on the electrical characteristics of 12-nm SOI FinFETs are simulated and discussed by an in-house quantum transport simulator. Both the ballistic limit and the scattering effects are examined.

P-3-3
Technology Computer Aided Design of 65nm SOI MOSFETs through Integrated Process and Device Simulations
E. M. Bazizi[1,2], P. F. Fazzini[1], F. Cristiano[1], A. Pakfar[2], C. Tavernier[2], C. Zechner[3], N. Zographos[3] and A. Claverie[1], [1]CNRS-LAAS, [2]STMicroelectronics, [3]Synopsys Switzerland LLC and [4]CEMES/CNRS (France)
Integrated process and device simulations were performed within a unique simulation tool to predict sub-65nm SOI device performance. Physically based process models were used to reproduce successfully the electrical characteristics of SOI devices

P-3-5
The Observation of the Random Dopant Fluctuation in Strained-SOI Devices
C. Y. Cheng[1], E. R. Hsieh[1], S. S. Chung[1], R. M. Huang[2], Y. H. Lin[2], C. T. Tsai[2], G. H. Ma[2] and C. W. Liang[2], [1]National Chiao Tung Univ. and [2]UMC (Taiwan)
The device performance and Vth variation of the MOS devices on the SOI and strained-SOI (SSOI) have been examined. For SSOIs, it shows the expected drain current enhancement and smaller B_{VT} than SOI ones. Furthermore, SSOIs exhibit a weak dependence of V_{th} variation on the drain bias as a result of the strain effect.

P-3-7
InGaAs and InGaAs-On-Insulator *n*-Channel MOSFETs Fabricated by Self-Align Gate First Process with Ni/Al_2O_3 Gate Stacks
S. Lee[1], R. Iida[1], S. H. Kim[1], M. Yokoyama[1], N. Taoka[1], Y. Urabe[2], T. Yasuda[2], H. Takagi[2], H. Ishii[2], N. Miyata[2], H. Yamada[3], N. Fukuhara[3], M. Hata[3], M. Takenaka[1] and S. Takagi[1], [1]Univ. of Tokyo, [2]NAIST and [3]Sumitomo Chemical Co., Ltd. (Japan)
We demonstrated self-align gate first InGaAs-on-insulator MOSFETs on Si substrates, fabricated by direct wafer bonding, for the first time. We found that III-V-on-insulator structure is a quite promising MOS structure for future technology nodes.

P-3-9
Characterization of Tunneling Resistance in Vertical Tunneling FETs
A. Tura and J. C. S. Woo, Univ. of California, Los Angeles (USA)
In this paper, the tunneling resistances of vertical p-i-n and p-n-p-n source tunneling nMOSFETs are experimentally investigated at different temperatures and gate voltages. Results show significant tunneling resistance reduction due to the n-type dopant pocket.

P-3-10
Improvement of High-k/metal gate pMOSFET performances and reliability with optimism Si cap/SiGe channel structure
C. W. Hsu[1], Y. K. Fang[1], C. Y. Chen[1], W. K. Yeh[2], C. T. Lin[3] and P. Y. Chen[4], [1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung, [3]UMC and [4]I-Shou Univ. (Taiwan)
The Hf-based high-k/metal gate SiGe pMOSFET with an optimism channel stack ratio has low V_{th} [~ -0.3V] and C-V hysteresis (< 5mV), superior Ion-Ioff, and V_{th} roll-off. Besides, it achieves good NBTI and HCI reliability.

P-3-12
Development of a Multi-Scale Time Dependent Dielectric Breakdown Simulator Based on TBQC and KMC Method: Application to the Evaluation of a Gate Oxide Film for CMOS Technology
H. Tsuboi, K. Inaba, Y. Hayashi, H. Sato, Y. Obara, Y. Suzuki, T. Miyagawa, S. Nakamura, R. Nagumo, R. Miura, A. Suzuki, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
We have succeeded in the development of a new multi-scale time dependent dielectric breakdown simulator using kinetic Monte Carlo method considering impact ionization, together with a tight-binding quantum chemical calculation to evaluate the trap depth.

P-3-13
Investigation of Low-Cost Stress Memorization Process on Layout and Low-Frequency Noise Performance for Strained-Si nMOSFETs
C. W. Kuo[1], S. L. Wu[2], H. Y. Lin[1], Y. T. Huang[1], S. J. Chang[1], D. G. Hong[2], C. Y. Wu[2], Y. C. Cheng[3] and O. Cheng[3], [1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]UMC (Taiwan)
Impact of low-cost stress-memorization technique (SMT) on layout and low frequency noise of nMOSFETs performance is investigated. The DC characteristics of SMT device become more sensitive to the layout as the device is scaled down. Moreover, both devices show comparable noise level, indicating the SMT process will not degrade interface quality.

P-3-14
Characterization the random telegraph noise in 32nm high-k/metal gate CMOSFETs
W. K.Yeh[1], C. W. Hsu[2], Y. K. Fang[2], C. Y. Chen[1], C. T. Lin[3] and P. Y. Chen[4], [1]National Univ. of Kaohsiung, [2]National Cheng Kung Univ., [3]UMC and [4]I-Shou Univ. (Taiwan)
We find that the RTN fluctuation (ΔI_D) in nMOSFETs is larger than it in pMOSFETs, especially with device scaling down. Drain current instability in 32nm generation and beyond should be considered more carefully for nMOSFETs.

P-3-15
Low-Frequency Noise Behavior of La-Doped Hf-Based Dielectric nMOSFETs
D. Y. Choi[1], C. W. Sohn[1], H. C. Sagong[1], M. S. Park[1], K. T. Lee[1], R. H. Baek[1], C. Y. Kang[2] and Y. H. Jeong[1], [1]POSTECH and [2]SEMATECH (Korea)
We investigated the low-frequency noise behavior of nMOSFETs with La-doped Hf-based gate dielectrics. They showed enhanced contribution of mobility fluctuation compared to the nMOSFETs without La.

P-3-16
The Compact Modeling of Zero Temperature Coefficient (ZTC) Point of DTMOS
K. T. Wang, W. C. Lin and T. S. Chao, National Chiao Tung Univ. (Taiwan)
For the first time, the compact analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. Newly analytical formulations are developed for both linear and saturation regions of DTMOS transistor operation.

P-3-17
A Simple Model for Threshold Voltage of Surrounding-gate MOSFETs With Interface Trapped Charges
T. K. Chiang, J. F. Lai and M. J. Yang, National Univ. of Kaohsiung (Taiwan)
Based on perimeter-weighted-sum method and scaling theory, a simple threshold voltage model for surrounding -gate MOSFETs with interface trapped charges is developed by considering the effects of equivalent oxide charges on the flat-band voltage. The model shows how various charge conditions and device structure parameters affect the threshold voltage behavior. The model is verified by the device simulator and can be efficiently used to explore the hot-carrier-induced threshold voltage degradation of the charge-trapped memory device.

P-3-18
A Forward Body Bias Characterization for Low Voltage CMOS Circuits
H. Aoki[1], M. Shimasue[1], M. Miyahara[2] and A. Matsuzawa[2], [1]MODECH Inc. and [2]Tokyo Tech (Japan)
This paper proposes a modified transistor model to improve the accuracy under the forward body bias operation that is vital for low voltage circuits to reduce the power consumption of CMOS LSI.

P-3-19
Investigation of Illuminated High-Frequency Capacitance-Voltage Response in Deep Depletion of HfO_2 and SiO_2 MOS Capacitors with Ultra-thin Gate Oxides
J. Y. Cheng and J. G. Hwu, National Taiwan Univ. (Taiwan)
The correlation between illuminated C-V response and deep depletion was demonstrated in MOS structure via local depletion capacitance model. The smaller initiation voltage (0.12V) of deep depletion in HfO2 is observed from magnified C-V curves and the non-uniform area ratio increases in MOS device after the illumination was also investigated.

P-3-21
Investigation of SACVD-Based STI Process on Electrical Characteristics of Nanoscale NMOSFETs
H. Y. Lin[1], S. L. Wu[2], C. W. Kuo[1], Y. T. Huang[1], S. J. Chang[1], D. G. Hong[2], C. Y. Wu[2], C. T. Huang[3] and O. Cheng[3], [1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]United Microelectronics Corp. (Taiwan)
Based on a detailed physical and electrical analysis, we have demonstrated that an improved densification anneal process of Sub-Atmospheric Chemical Vapor Deposition (SACVD)-based STI process to enhance NMOSFETs performance can be used in 40-nm node and beyond. Moreover, it would not affect on active gate oxide edge reliability for devices.

P-3-22
Calibration of Linear Piezo Resistance Coefficients using 3-Dimensional Stress Simulation of Si-MOSFETs Structures
A. Satoh[1], T. Tada[1], V. Poborchii[1], T. Kanayama[1], S. Satoh[2] and H. Arimoto[1], [1]AIST and [2]Fujitsu Semiconductor Ltd. (Japan)
The linear Piezo resistance model was calibrated using stress tensor by a well calibrated 3-dimensional stress simulation. By using of precise stress distribution in channel region of Si-MOSFET, the calibrated mobility model could predict mobility dependencies on layout parameters of Si-MOSFET.

P-3-23
Investigation of Different Capping Layers and Strain Sources for SMT Process
C. C. Liao, M. C. Lin and T. S. Chao, National Chiao Tung Univ. (Taiwan)
The compressive nitride is a promising technique for strain coupling,gate leakage, and hot carrier immunity concern for SMT application. The mechanisms of strain source and hydrogen diffusion are also clarified.

P-3-24
X-Ray Radiation Effects on CMOS Image Sensor In-Pixel Devices
J. Tan[1], B. Buttgen[1] and A. J. P. Theuwissen[1,2], [1]Delft Univ. of Tech. and [2]Harvest Imaging (the Netherlands)
This paper presents new results of radiation-induced degradation on 4-Transistor CMOS Image Sensor In-Pixel devices with the pinned photodiode and transfer-gate transistor due to the interface trap generation and trapped charges in the shallow trench isolation oxide during the radiation damage.

P-3-25
High-Performance (S. S.<100 mV/dec) Poly-Si TFTs with Laser Annealed Channel and High-κ Metal-Gate on Glass Substrate
Y. H. Lue[1], C. H. Chien[1], P. Y. Kuo[1], M. J. Yang[1], H. Y. Lin[2] and T. S. Chao[1], [1]National Chiao Tung Univ. and [2]Toppoly Optoelectronics Corp. (Taiwan)
We demonstrate high performance LTPS-TFTs with a TaN/HfO2 and laser-annealed channel to combine glass substrate (called GSHM-TFTs). The GSHM-TFTs exhibit a low V_{TH}, steep S.S.~ 95, 154mV/dec. and high Iratio>10^7, 10^8 for N and P channel, respectively. The impact of grain boundaries in poly-Si is also investigated.

P-3-26 (Late News)
Electron and hole mobility comparison in a single Ge-MOSFET fabricated on 50 nm-thick GeOI substrate
D. D. Zhao[1], C. H. Lee[1], T. Nishimura[1,2], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
We show a direct comparison of electron mobility with hole one in a single MOSFET fabricated on 50 nm-thick low-doped GeOI by using the modified double Lm method.

P-3-27 (Late News)
Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16-nm CMOS Devices
Y. Li[1,2], C. H. Yu[1], M. H. Han[1] and H. W. Cheng[1], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)
We estimate metal-gate-work-function fluctuations using full 3D device simulation which is different from the result of averaged work-function method due to localized random work-functions. Effects of number and position for different grain orientation are analyzed.

Area 4: Advanced Memory Technology
(10 Papers)

P-4-1
Impedance analysis of controlled-polarization-type ferroelectric-gate TFT using RC distributed constant circuit
T. Fukushima, K. Maeda, T. Yoshimura, A. Ashida and N. Fujimura, Osaka Prefecture Univ. (Japan)
By using RC-distribution-constant-circuit, it was analyzed that the reversal of PSFe in ferroelectric-gate TFT was occurred only at the region near the source electrode
by negative VG, and entire channel region by positive VG.

P-4-2
Effect of MIM type selection device on readout margin of cross-point bipolar ReRAM
J. Shin, I. Kim, J. Park, J. Lee, M. Jo, K. P. Biju, S. Jung, W. Lee, S. Kim, S. Park, D. Lee and H. Hwang, Gwangju Inst. of Sci. and Tech. (Korea)
We investigated an MIM type selection device that can alleviate the cross-talk effect in cross-point arrays. Also, a readout margin was analyzed depending on the memory size and an existence of a selection device.

P-4-3
One-Diode-One-Resistor Titanium-Oxide RRAM Fabricated at Room Temperature
C. W. Kuo, J. J. Huang, W. C. Chang and T. H. Hou, National Chiao Tung Univ. (Taiwan)
A nonpolar Pt/TiO2/Pt RRAM and a high forward-current Ti/TiO2/Pt oxide diode are realized using identical TiO2 by room-temperature evaporation. Excellent characteristics are reported for the individual diode, RRAM, and diode / RRAM in series.

P-4-4
Improved Resistive Switching Uniformity of a Bilayer TiO_2 Films
I. Kim, S. Jung, J. Shin, K. P. Biju, K. Seo, M. Siddik, X. J. Liu, J. Kong, K. Lee and H. Hwang, Gwangju Inst. of Sci.and Tech. (Korea)
We investigated the resistive switching properties of bilayer TiO2 films. To solve inferior electrical problems of sol-gel process, we deposited additional thin ALD TiO2 layer. Also, switching mechanism is suggested based on exchange oxygen ions.

P-4-5
Miniaturization Limit of Memory Cell in Polycrystalline-NiO-ReRAM
K. Dobashi[1], K. Kinoshita[1,2], T. Yoda[1] and S. Kishida[1,2], [1]Tottori Univ. and [2]Tottori Univ. Electronic Display Research Center (Japan)
Localized current distributions of polycrystalline NiO films were investigated by using C-AFM. It was suggested the minimum unit to generate the resistance change effect of polycrystalline NiO films was one crystal grain.

P-4-6
The observation of "Conduction Spot" on NiO resistance RAM
T. Fujii[1], H. Kondo[1], H. Kaji[1], M. Arita[1], M. Moniwa[2], T. Yamaguchi[2], I. Fujiwara[2], M. Yoshimaru[2] and Y. Takahashi[1], [1]Hokkaido Univ. and [2]STARC (Japan)
We successfully demonstrate and observe the conduction spot (CS) which includes filamentary path. The CS size can be controlled. The results suggest NiO ReRAM device size will be reduced by reducing the forming power.

P-4-7
Impact of Engineered Buried Ti layer on the Memory Performance of HfOx RRAM
P. S. Chen[1], H. Y. Lee[2,3], Y. S. Chen[2,3], P. Y. Gu[2], F. Chen[2] and M. J, Tsai[2], [1]MingShin University of Science & Technology, [2]Indus. Tech. Res. Inst. and [3]National Tsing Hua Univ. (Taiwan)
Impact of engineered Ti layer on the memory performance of 5-nm-thick HfOx RRAM devices are investigated. Two stacked layer, consisted of Ti/HfOx/TiN and TiN/HfOx/Ti, were prepared.With a Ti of 10 nm, more oxygen atoms in HfOx films are captured during the capping of Ti overlayer.

P-4-8
High Efficiency Charge Storage Layer for MLC NAND Non-Volatile Memory
S. H. Liu[1], W. L. Yang[1], C. W. Chiu[1] and T. S. Chao[2], [1]Feng Chia Univ. and [2]National Chiao Tung Univ. (Taiwan)
Recently, multi-level cell (MLC) as a promising technique has been researching to increase the storage density of SONOS-type NAND non-volatile memory. However, the main challenge of MLC operation is an electrical reliability problem because charge data retention and device endurance influence discrimination of multi bit. Therefore, the level of voltage offset between state and state (11, 10, 01, and 00) plays one of the key factors for MLC.

P-4-9
Evaluation of ALD grown strontium-doped HfO_2 thin films as capacitor dielectric for 40nm DRAM Device and beyond
J. S. Lim, J. H. Choi, S. J. Chung, S. Y. Kang, M. Y. Park, Y. Kim, K. Cho and C. Y. Yoo, Samsung Electronics Co., Ltd. (Korea)
Sr doped HfO2 (Sr-HfO2) films with tetragonal crystal structure was fabricated by atomic layer deposition method and 550°C post deposition anneal. The specific dielectric constant of the tetragonal Sr-HfO2 film was as high as 40.

P-4-10 (Late News)
Organic Nonvolatile Memories Based on PMMA and PHEMA Dielectric Layers
Y. C. Chen[1], C. Y. Huang[2], H. C. Yu[1], C. Y. Cheng[1], Y. K. Su[1] and T. H. Chang[1], [1]National Cheng Kung Univ. and [2]National Taitung Univ. (Taiwan)
We have fabricated the resistor-type memories with poly(2-hydroxyethyl methacrylate) PHEMA and poly(methyl methacrylate) PMMA active layer, respectively. From the I-V characteristics, the devices with PMMA active layer have a lower erasing voltage (1.9 V) than that (2.6 V) of PHEMA- devices.

Area 5: Advanced Circuits and Systems
(13 Papers)

P-5-2
A 1 Gb/s Differential Input Threshold Detection Based BPSK Receiver For IR-UWB Communication Using 180 nm CMOS Technology
M. Hafiz, N. Sasaki and T. Kikkawa, Hiroshima Univ. (Japan)
A complete non-coherent differential input threshold detection based receiver for UWB-IR communication is demonstrated. The chip developed in 180 nm CMOS technology, occupying an area of 3.4 mm^2, retrieves a BPSK data of 1 Gb/s using a supply voltage of 1.8 V while consuming 76 pJ/bit.

P-5-3
A Fractional-N Frequency Synthesizer-Based Multi-standard I/Q Carrier Generation System in 0.13um CMOS
W. Lou, X. Yan, Z. Geng and N. Wu, Institute of Semiconductors, Chinese Academy of Sciences (China)
This paper presents a carrier generation system based on fractional-N frequency synthesizer with three Quadrature VCOs and it generates I/Q LO frequency. The locked frequency range is 2.8-6.1GHz. And successive divide_by _2 prescalers make the frequency from 0.7 to 6.1 GHz continuously by the reasonable frequency planning.

P-5-5
The Effect of Field-Plate Technique on CMOS Ring Oscillator
H. C. Chen[1], C. H. Kuo[1] and S. S. Lu[2], [1]National Taiwan Univ. of Sci. and Tech. and [2]National Taiwan Univ. (Taiwan)
Field-plate technique is applied to ring oscillators in 0.35-μm CMOS technology. Ring oscillators constructed from field-plate transistors and standard ones achieve phase noises of -85.4/-82.9 dBc/Hz at 100-kHz offset, respectively. It improves the oscillator phase noise by 2-3 dB in the $1/f^3$ region but it makes no difference over the $1/f^2$ region.

P-5-6
A 12b Two-Stage Single-Slope ADC with Time to Digital Converter
M. Shin, M. Ikebe, J. Motohisa and E. Sano, Hokkaido Univ. (Japan)
Applying a TDC with multi-phase-clock signals reduced the number of circuit elements, achieved consistency between a single-slope ADC and the TDC, and realized robust meta-stability. We designed a 12-bit ADC by using 0.25-μm CMOS process.

P-5-7
Self-Dithered Digital Delta-Sigma Modulators for Fractional-N PLL Synthesizers
Z. Xu, J. G. Lee and S. Masui, Tohoku Univ. (Japan)
We propose a novel dithering method with simple implementation and non-hardware overhead to eliminate spurs of digital delta-sigma modulators (MASH and single-loop) applied in PLL applications. Simulation results compared with conventional solutions prove its effectiveness.

P-5-8
g_m/I_D Lookup Table Based Operational Transconductance Amplifier Design Featuring Settling Time Optimization
T. Kashimura, T. Konishi and S. Masui, Tohoku Univ. (Japan)
We propose the gm/I_D lookup table based OTA design method featuring settling time optimization, which can achieve the target settling time with the minimum power consumption by employing an iterative design sequence.

P-5-9
A Novel Soft-Start Control Circuit for Current-Mode Buck DC-DC Converters
K. Shibata and C. K. Pham, The University of Electro-Communications (Japan)
This paper proposes a soft-start control circuit for Current-Mode DC-DC Converters. The circuit achieved the soft-start characteristics of 150 µs. The control circuit is not sensitive to the input voltage, operating temperature and inductor value.

P-5-10
A Multiple Time Programmable On-chip Trimming Technique for CMOS Bandgap Reference Circuits
C. H. Wu, H. Lin and M. K. Wang, National Chung Hsing Univ. (Taiwan)
An alternative trimming technique for voltage reference circuits using multiple time programmable (MTP) devices is proposed using TSMC 0.35µm CMOS process in smaller chip area with more flexibility. The measurement results demonstrate the variation of reference voltages could be reduces from 120mV to 20mV after the trimming method was applied.

P-5-11
A Sub-nanoampere Two-stage Power Management Circuit in 0.35-µm CMOS for Dust-Size Batteryless Sensor Nodes
M. Ugajin, T. Shimamura, S. Mutoh and M. Harada, NTT Corp. (Japan)
A sub-nanoampere two-stage power management circuit that uses off-chip capacitors for energy accumulation is presented. The simulated and experimental results for the power management circuit describe the operation for a 1-nA current source.

P-5-12
An Energy Harvest Current-Mode Demodulator for Low Power 3-D Stacked Retinal Prosthesis
K. Kiyoyama[1,2], T. Fukushima[2], M. Koyanagi[2] and T. Tanaka[2], [1]Nagasaki Institute of Applied Science and [2]Tohoku Univ. (Japan)
In this paper, the proposed current-mode demodulator using clamped current which is usually disposed thermal energy at clamp circuit is described.

P-5-13
A Novel RectifierArchitecture for UHF RFID Transponder
J. Cui, J. Akita and A. Kitagawa, Univ. of Kanazawa (Japan)
This paper presents a novel rectifier structure for wireless biomedical temperature monitoring tags. The proposed rectifier has an advance in realizing high power conversion efficiency (PCE) as well as gaining high output voltage simultaneously. This circuit has been fabricated in a standard CMOS process. Measurement results show a PCE of 32% at -30dBm incident power.

P-5-14
Distribution of Characteristic Changes in MOSFETs Induced by Resin-Molded Packaging Stress
N. Ueda, E. Nishiyama and H. Watanabe, RICOH Company, Ltd. (Japan)
Packaging-induced performance reductions for a small-scale IC are evaluated using specially designed test chips. The results reveal that not only MOSFET selection but also the orientation should be considered for increasing the precision of ICs.

P-5-15 (Late News)
Low-Voltage and High-Speed Voltage-Controlled Ring Oscillator with Widely Tuning Range in 0.18µm CMOS
Y. S. Tiao, M. L. Sheu and L. J. Tsao, National Chi-Nan Univ. (Taiwan)
A new differential delay cell with a complementary current control to increase the control voltage range as well as the operation frequency is proposed for low-voltage op-eration. The measured results show that a wide operation frequency range with a best FOM from 8.36GHz to 1.29GHz and from 4.09GHz to 0.479GHz are achieved at the full range control voltage of 1.8V and 1V, respectively.

Area 6: Compound Semiconductor Electron Devices and Related Technologies
(11 Papers)

P-6-1
Characterization of SiGe Thin Films Deposited by RF Magnetron Sputtering for Infrared Imaging Sensor
K. Yamaki[1], S. Sekino[2], T. Tai[1], S. Nakamura[2], T. Yoshitake[2] and A. Furukawa[1], [1]Tokyo Univ. of Sci. and [2]NEC Corp. (Japan)
An alternating multi-stacked SiGe film was deposited by using RF magnetron sputtering technique for infrared imaging sensor. The film annealed in an Ar atmosphere exhibited a large TCR and a high conductivity.

P-6-3
The low frequency noise analysis in bottom-gated ZnO Thin film Transistors with different active layer thickness
K. S. Jeong[1], Y. S. Kim[2], J. G. Park[1], S. D. Yang[1], Y. M. Kim[1], H. J. Yun[1], H. D. Lee[1] and G. W. Lee[1], [1]Chungnam National Univ. and [2]National NanoFab Center (Korea)
In this paper, 1/f noise is analyzed to characterize the quality of the active layer of ZnO TFTs with different thicknesses of 40 nm and 80 nm. The extracted Hooge's parameter (aH) indicates that the ZnO film of 80nm with the larger grain size has better quality, which explains well the inferior Vth instability of the ZnO film of 40nm.

P-6-5
Short Channel Effect of Indium-Gallium-Zinc-Oxide Thin Film Transistors
S. H. Kuk, D. W. Kang, J. S. Lee, S. J. Kim, J. Y. Kwon and M. K. Han, Seoul National Univ. (Korea)
We have fabricated and investigated short channel IGZO TFTs. And we have investigated the current conduction mechanism of IGZO TFTs. When we design IGZO TFTs, we should consider the whole active layer, because IGZO films have high mobility and high carrier concentration.

P-6-6
Physics-Based Modeling and Analysis of Compound Semiconductor Devices and Circuits in Extreme Environments
M. Turowski, A. Raman and A. Fedoseyev, CFD Research Corp. (CFDRC) (USA)
Mixed-mode simulations combining 3D device physics with external load circuit enable prediction of transient radiation effects in circuits with III-V HEMTs and SiGe HBTs. Including circuit parasitics is critical for computing results matching experimental data.

P-6-8
10-Gb/s InGaAs P-I-N photodetector with planar buried heterostructure
Y. S. Wang[1,3], S. J. Chang[1], Y. Z. Chiou[2], S. P. Chang[1], Y. H. Wu[3], R. T. Hsu[3] and W. Lin[3], [1]National Cheng Kung Univ., [2]Southern Taiwan University and [3]LandMark Optoelectronics Corp. (Taiwan)
The authors report the fabrication of high performance planar InGaAs P-I-N buried heterostructure photodetectors (BH-PD) by introducing mesa etching and refilling with semi-insulating InP. It was found that measured 3-dB bandwidth for the fabricated BH-PD was 12.4 GHz.

P-6-9
Enhanced Device Performance of AlGaN/GaN MOSHEMT with Thermal Oxidation
S. Liu[1], J. Wang[1], R. Gong[1], Z. Dong[1], M. Yu[1], C. P. Wen[1], C. Zeng[2], Y. Cai[2] and B. Zhang[2], [1]Peking Univ. and [2]Suzhou Inst. of Nano-tech and Nano-bionics (China)
Bottom-gated thin-film transistors (TFTs) were fabricated on Corning 1737 glass substrates using ZnO channel layer grown by MOCVD and Si3N4 gate dielectric by PECVD. It is demonstrated that the VI/II ratio used for the growth of ZnO film as well as the incorporation of a thin MgZnO layer at the ZnO/Si3N4 interface affects TFT performance.

P-6-12
Normally-off GaN MOSFET with ITO Schottky Barrier Source/Drain and $(NH_4)_2S_X$ Surface Treatment
T. H. Kim[1], C. J. Lee[1], D. S. Kim[1], S. Y. Sung[1], B. K. Jung[2], Y. W. Heo[1], J. H. Lee[1] and S. H. Hahm[1], [1]Kyungbook National Univ. and [2]Electronics and Telecommunications Res. Inst. (Korea)
We demonstrated the schottky barrier metal oxide semiconductor field effect transistor applying indium-tin-oxide to the source and drain for the first time on the highly resistive GaN layer grown on silicon substrate. Using the $(NH_4)_2S_X$ pretreatment of GaN substrate, the I-V characteristics were improved.

P-6-13
Improved optical properties of a-plane InGaN/GaN multiple quantum wells with gradient-stages MQW structure
H. C. Hsu[1], Y. K. Su[2], S. J. Huang[1], C. Y. Cheng[1], H. C. Chen[1], J. H. Hong[1], K. C. Chen[1], Y. J. Wang[3], C. Y. Wu[3] and M. C. Chou[3], [1]National Cheng Kung Univ., [2]Kun Shan Univ. of Tech. and [3]ITRI South Micro Systems Tech. Center (Taiwan)
In this paper, the crystal quality of a-plane InGaN ＼ GaN MQWs was further improved by implanting the gradient-stage MQWs before the active region. The a-palne InGaN ＼ GaN MQWs with N (N=0, 5, 8, and 11) pairs of gradient-stage MQWs structure was also investigated.

P-6-14
Investigation of Bias Temperature Instability in HfInZnO Thin Film Transistor
J. S. Chang[1], S. W. Kim[1], D. W. Kwon[1], J. H. Kim[1], J. C. Park[2], I. Song[2], U. I. Jung[2], C. J. Kim[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Adv. Inst. of Tech. (Korea)
In the HfInZnO TFT, some reliability issues such as NBTI and PBTI are investigated. PBTI causes threshold voltage shift, and it is attributed to electron injection and hopping into SiO2 bulk layer.

P-6-15
Study of the CeO_2/HfO_2/InAs metal-oxide-semiconductor capacitors with different post-deposition-annealing temperatures
T. E. Shie[1], C. H. Chang[1], Y. C. Lin[1], K. Kakushima[2], H. Iwai[2], P. C. Lu[1], T. C. Lin[1], G. N. Huang[1] and E. Y. Chang[1], [1]National Chiao Tung Univ. and [2]Tokyo Inst. of Tech. (Taiwan)
We have fabricated CeO2/HfO2/InAs two layers high-k dielectric MOS capacitor. The device shows the good C-V characteristics and higher capacitance value than HfO2/InAs. It is an candidate for high performance low power logic device applications.

P-6-16 (Late News)
Transparent oxide thin-film transistors using modulation-doped heterostructures
S. Taniguchi[1], M. Yokozeki[1], M. Ikeda[1] and T. Suzuki[2], [1]Sony Corp. and [2]JAIST (Japan)
Employing n-ITO / IGZO modulation-doped het-erostructures, we confirmed enhancements of electron mo-bilities and TFT performances. Modulation doping is a promising method for improvements of TFT characteristics using TOSs.

Area 7: Photonic Devices and Optoelectronic Integration
(21 Papers)

P-7-1
Electrorefractive Effect in Strained InGaAs/InAlAs Five-Layer Asymmetric Coupled Quantum Well
T. Wajima[1], T. Arakawa and K. Tada[2], [1]Yokohama National Univ. and [2]Kanazawa Inst. Of Tech. (Japan)
We theoretically analyze an InGaAs/InAlAs strained five-layer asymmetric coupled quantum well for optical modulators based on phase modulation. It is expected to exhibit large electrorefractive index change over a wide wavelength range with low voltage.

P-7-2
Modification of Material Parameters for InGaAs/InAlAs Quantum Wells
H. Yamada, Y. Iseri and T. Arakawa, Yokohama National Univ. (Japan)
We discuss material parameters for InGaAs/InAlAs quantum wells comparing experimental and calculated data. Using the modified material parameters, we succeeded in obtaining the calculated absorption coefficient spectra more consistent with the experimental.

P-7-3
Influence of Intrinsic Layer Impurity in InGaAs/InAlAs Asymmetric Triple Coupled Quantum Well on Its Electrorefractive Index Change
Y. Amma, K. Ema and T. Arakawa, Yokohama National Univ. (Japan)
We theoretically discuss the electrorefractive effect in an InGaAs/InAlAs ATCQW for 1.55-um-wavelength regions and the influence of intrinsic layer impurity on the electrorefractive index change of the ATCQW.

P-7-4
Dry Etching of Al-rich $Al_xGa_{1-x}As$ Holes with High Aspect Ratio for Photonic Crystal Fabrication
M. Mochizuki, T. Nakajima, D. Satoi, F. Ishikawa, M. Kondow, M. Hara and H. Aoki, Osaka Univ. (Japan)
We investigate ICP dry etching of AlxGa1-xAs for Photonic crystals fabrication. Avoiding the formation of oxide deposition, we obtain the air holes having its aspect ratio of 8 with its small diameter 110 nm.

P-7-5
Two-terminal device based on white-light emitting in GaAs single layer
S. Choi[1], Y. W. Lee[2], B. J. Kim[1], J. Choi, G. W. Seo[3] and H. T. Kim[1], [1]ETRI, [2]Pukyong National Univ. and [3]Univ. of Science and Tech. (Korea)
The two-terminal based on p-type GaAs single layer shows a white light emission(WLE) with a wavelength of 500~800 nm in visible ray. The light intensity can be controlled by isolation size of film, thickness of film, and carrier concentration. Furthermore, a WLE can be applied as quantum dot laser source, various light fixtures, and photo-diodes.

P-7-6
Optical Characterization of Broadband Asymmetrical Quantum Well for Laser Array Application
W. L. Chen, National Changhua Univ. of Edu. (Taiwan)
A 98nm photoluminescence bandwidth centered at 1520nm was achieved by an AlGaInAs asymmetrical quantum well design and transition features have been identified by photoreflectance. The performance of DFB laser array was compared with optical characterization.

P-7-7
The Output Characteristics of a Soliton Cavity Laser Diode
M. C. Shih, W. C. Su and C. S. Chen, National Univ. of Kaohsiung (Taiwan)
We present the output characteristics of a novel semiconductor laser diode with an intra cavity of solitons waveguide. It shows a different output characteristics from the traditional linear laser stripe lasers.

P-7-8
Enhanced Light Output of Vertical GaN-Based LEDs with Surface Roughening Using Sizu-Controllable SiO_2 Nanotube Arrays
D. M. Kuo[1], S. J. Wang, K. M. Uang[2], T. M. Chen, W. C. Lee[1] and P. R. Lee, [1]National Cheng Kung Univ. and [2]Wufeng Inst. of Tech. (Taiwan)
The use of SiO2 nanotube arrays for nano-roughened n-GaN surface to improve the optoelectronic properties of vertical structure GaN-based LEDs shown a typical increase in light output power by 49.8% at 350 mA

P-7-10
An Investigation of GaN-Based LED with MBE Grown Nanopillars by MOCVD.
K. L. Chuang, J. R. Chang, P. M. Tu, C. H. Chiu, Y. J. Li, H. W. Zan, H. C. Kuo and C. Y. Chang, National Chiao Tung Univ. (Taiwan)
High quality GaN-based LED was fabricated by MOCVD using MBE GaN NPs template. Room temperature Raman shift and TEM demonstrated great reduction in the strain of sample and the quality enhancement mechanism, void-induced dislocation-gathering and stress-relaxation.

P-7-11
High Quality Vertical LEDs Fabrication by Means of Mechanical Lift-off
P. M. Tu[1], S. C. Hsu[2], M. H. Lo[1], H. W. Zan, H. C. Kuo, S. C. Wang, Y. J. Cheng[3] and C. Y. Cheng[1], [1]National Chiao Tung Univ., [2]Tamkang Univ. and [3]Academia Sinica (Taiwan)
We report the fabrication of mechanical lift-off high quality thin GaN by using Hexagonal Inversed Pyramid (HIP) structures as a sacrificial layer during wafer bonding process for vertical light emitting diodes.

P-7-12
The Improvement of Light Intensity for Nitride-Based MQW LEDs by Gradient-Stage Emitter Layer
S. J. Huang, Y. K. Su, C. Y. Tseng, S. C. Lin and H. C. Hsu, National Cheng Kung Univ. (Taiwan)
The light intensity of nitride-based LEDs is improved by an emitter layer (EL) with gradient depth of quantum wells (QWs). The results shows about 20% increment compared to dual-stage LED.

P-7-13
Manipulative Polarization of a-plane InGaN/GaN Photonic Crystals for Enhanced Spontaneous Emission
Y. C. Lee[1], H. H. Huang[2], Y. R. Wu and P. Yu[1], [1]National Chiao Tung Univ. and [2]National Taiwan Univ. (Taiwan)
Polarization characteristics of a-plane InGaN/GaN photonic crystal microcavities are manipulated to enhance spontaneous emission (SpE) without compromising cavity Q and modal volume. Enhanced SpE rates are investigated for different quantum well thicknesses and indium compositions

P-7-14
Reduction in efficiency droop in InGaN/GaN MQWs light-emitting diodes grown on free standing GaN substrate
C. H. Chiu[1], C. L. Chao[1,2], D. W. Lin[1], Z. Y. Li, H. C. Kuo, T. C. Lu and S. C. Wang, [1]National Chiao Tung Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
The LEDs fabricated on the free-standing GaN template exhibit smaller EL peak wavelength blue shift (1.2 nm), great enhancement of the light output and reduced efficiency droop compared with the conventional LEDs.

P-7-15
Estimating the Junction Temperature of InGaN and AlGaInP LEDs
Y. J. Lee, C. J. Lee and C. H. Chen, National Taiwan Normal Univ. (Taiwan)
This work proposes an approach for directly determining the dependence of junction temperature on injected currents in InGaN and AlGaInP LEDs. Various important physical parameters that affect the junction temperature of an LED are also considered.

P-7-16
Characteristics of μ-Slice InGaN/GaN Light Emitting Diodes Formed by Focused Ion Beam Process
C. K. Hsu[1], J. K. Sheu, J. K. Wang, M. L. Lee[2], K. H. Chang[1], S. J. Tu and W. C. Lai, [1]National Cheng Kung Univ. and [2]Southern Taiwan Univ. (Taiwan)
In this study, we used focused ion beam to mill GaN/InGaN LED wafer into single micro scale device. The electrical and optical properties have been studied to investigate the damage caused by the ion beam.

P-7-17
GaN-based MIS Ultra-violet Photodetectors with the ZrO_2 Insulating Layer
C. H. Chen, Y. H. Tsai, S. Y. Tsai and C. F. Cheng, Cheng Shiu Univ. (Taiwan)
GaN MIS UV photodetectors with ZrO2 insulating layer were successfully fabricated and characterized. It was found that we can achieve the small dark current and large photocurrent to dark current contrast ratio from the proposed device with the use of ZrO2 insulating layer.

P-7-18
Fabrication of Multi-Stack Ge Quantum-Dots for Blue to Near-Ultraviolet MOS Photodetectors
R. H. Yeh[1], S. Y. Lo[2], C. H. Yang, J. T. Horng and J. W. Hong, [1]Asia Univ. and [2]National Central Univ. (Taiwan)
Metal-oxide-semiconductor photodetectors (PDs) with multi-stack and discrete Ge quantum dots (QDs) embedded in a-SiON/SiO2 matrix for visible to near-ultraviolet photodetection have been fabricated with thermal anneal of as-deposited amorphous alloy layers.

P-7-20
Mach-Zehnder Electro-Optic Modulator Fabricated on Silicon-on-Insulator (SOI) Substrate Based on the Multimode Interference (MMI) Effect
R. W. Chuang[1,3], M. T. Hsu[1], Y. C. Chang, S. H. Chou[3] and Y. J. Lee[2], [1]National Cheng Kung Univ. , [2]National Nano Device Laboratories, Hsinchu City and [3]National Nano Device Laboratories, Tainan (Taiwan)
The design of MMI-based 3dB MZI power splitter/combiner with dimensions of 6000um x 40um was proposed and analyzed. The operation of this device was based on the carrier injection effect, from which an approximate extinction ratio of -18.3 dB was obtained using BPM simulation. As for the device measurements, when the driving power was set at 0.2 W, the first π phase shift was observed.

P-7-21
Low loss junction of Si-wire waveguides and silica based waveguides for a hybrid waveguide photonic integrated circuit
Y. Wakayama, T. Kita and H. Yamada, Tohoku Univ. (Japan)
The concept of the proposed hybrid waveguide photonic integrated circuit is that silica based waveguide is used for long distance optical interconnection and Si-wire waveguides are used for making sharp bend.

P-7-22
Migration-limited relaxation in $Er_xY_{2-x}SiO_5$ crystals
T. Nakajima, T. Kimura and H. Isshiki, Univ. of Electro-Communications (Japan)
Er_2iO_5 crystal is a key light source material for Si-photonics. In this system, the energy transfer can occurred between Er^{3+}-Er^{3+} in $^4I_{13/2}$.

P-7-23
Transmission enhancement of metal-patterned resonant filters on silicon substrates in terahertz frequencies
P. K. Chung, H. C. Huang and S. T. Yen, National Chiao Tung Univ. (China)
We demonstrated a substrate-supported metal-patterned resonant filter with peak transmittance approaching transmittance of the substrate. The filter showed over 10 % increase in the peak transmittance and a comparable quality factor comparing with conventional filters.

Area 8: Advanced Material Synthesis and Crystal Growth Technology

(16 Papers)

P-8-1
Growth of semipolar InN (10-13) on $LaAlO_3$(112) substrate
W. C. Chen[1, 4], S. Y. Kuo[2], W. T. Lin[3], J. S. Tian[4], F. I. Lai[3], C. N. Hsiao[1] and L. Chang[4], [1]National Applied Research Labs., [2]Chang Gung Univ., [3]Yuan-Ze Univ. and [4]National Chiao Tung Univ. (Taiwan)
In this study, we report the growth and characterization of semipolar (10-13) InN films grown on LaAlO3 (112) substrate by metalorganic molecular beam epitaxy. InN films were grown at various substrate temperatures in the range of 465~540 °C.

P-8-2
Growth Mechanism of Nonpolar A-Plane GaN on Patterned M-Plane Sapphire
K. L. Chuang, J. R. Chang, S. P. Chang, P. M. Tu, Y. C. Hsu, W. Y. Chen, H. W. Zan, T. C. Lu, H. C,. Kuo and C. Y. Chang, National Chiao Tung Univ. (Taiwan)
Growth mechanism of a-GaN on trench-patterned m-sapphire by MOCVD under different V/III ratio was demonstrated. For V/III ratio from 350 up to 9000, growth of GaN from +c plane sidewalls is dominated.

P-8-4
Laser Treatment of AlN Co-doped ZnO Film for p-type ZnO Fabrication
L. W. Lai, K. W. Lin, C. H. Chang and J. T. Chen, Indus. Tech. Res. Inst. (Taiwan)
High quality p-type ZnO film can be obtained by co-sputtering of ZnO and AlN targets under adequate N2/Ar flow ratio of 4% and laser activation energy density at 150mJ/cm2.

P-8-5
Zinc oxide (ZnO) grown by Vertical-Plasma-Enhanced Metal Organic Chemical Vapor Deposition (VPEMOCVD)
P. H. Lei, H. F. Kao, F. S. Juang and X. M. Wu, National Formosa Univ. (Taiwan)
In this article, we have successfully fabricated ZnO film by VPEMOCVD. The growth temperature changed from 300 to 600 °C under the growth pressure of 30 mtorr and RF power of 100mW. The optical and electrical measurement indicated that the optimum growth temperature is around 500 °C.

P-8-6
Fabrication of transparent p-NiO/n-ZnO heterojunction diodes for ultraviolet photodetector
S. Y. Tsai[1], M. H. Hon[1] and Y. M. Lu[2], [1]National Cheng Kung Univ. and [2]National University of Tainan (Taiwan)
The fabrication and the properties of an optically transparent p-n heterojunction photodiode consisting of p-NiO and n-ZnO thin films. The structural and optical properties of the n-ZnO/p-NiO heterojunction were characterized by X-ray diffraction (XRD), UV-visible spectroscopy, Hall measurement, and I-V photocurrent measurements.

P-8-7
Preparation and Characterization of white ZnS:Pr,Mn,KCl Phosphor
S. H. Yang, C. H. Wang, Y. H. Ling and C. F. Do, National Kaohsiung University of Applied Sciences (Taiwan)
Approaches of mixing complementary phosphors and codoping of activators were used to prepare white ZnS-based phosphors. Photoluminescence of the phosphor prepared by codoping was higher than that of the phosphor prepared by complementary mixing.

P-8-8
Growing evaporated Ge dots with high crystallinity on patterned Si substrate by post thermal annealing
C. W. Chiu, T. W. Liao, H. J. Huang, J. H. Lin and C. H. Kuan, National Taiwan Univ. (Taiwan)
To obtain the evaporated Ge dots with high crystallinity on Si substrate, a method of using nano-structure and post thermal annealing is demonstrated. With well-designed hole-array pitch, the distribution of oxygen and quality of Ge QDs can be optimized. The processed Ge QDs size is over 20 nm which is estimated with the phonon confinement model of Raman scattering and confirmed by TEM image.

P-8-9
Site- and shape-controlled growth of single and pair of InAs quantum dots using AFM anodic oxidation
K. M. Cha[1], K. Shibata[1], I. Horiuchi[1], T. Ueda[1] and K. Hirakawa[1,2], [1]IIS/INQIE, Univ. of Tokyo and [2]CREST-JST (Japan)
Site- and shape-controlled InAs QDs have been fabricated by AFM-assisted anodic oxidation at various applied voltages. It was found that site-controlled QDs have clear facets, suggesting their excellent crystalline quality. The size-control of InAs QDs was carried out by changing the applied voltage V and found that the lateral size of the QDs can be reproducibly controlled over a range of 30-140 nm simply by tuning V.

P-8-10
Graphene Layers on Sapphire Substrates Grown by Alcohol CVD method
Y. Miyasaka, A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan)
We evaluated graphene layers on sapphire substrates synthesized by alcohol CVD using UV-VIS spectral transmittance measurement and Raman spectroscopy. The results indicates a significance of a certain amount of thermal energy to form graphene networks on sapphire substrates.

P-8-11
High electron mobility InSb films grown on Si (111) substrate via √7×√3-In and 2×2-In surface reconstructions
S. Khamseh, K. Nakatani, K. Nakayama, M. Mori and K. Maezawa, Univ. of Toyama (Japan)
The heteroepitaxial growth of InSb films with high electron mobility achieved via InSb bi-layer with two step growth procedure. This study shows the efficiency of the InSb bi-layer and two-step growth procedure for the improvement of the electrical property of the InSb films.

P-8-12
Facile Fabrication of Two-dimensional Assemblies of Gold Nanoparticles by Using Solvent evaporation method
K. Sugawa, Y. Tanoue, D. Tanaka and T. Sakai, Nihon Univ. (Japan)
A novel approach for the rapid and facile preparation of thetwo-dimensional assemblies of gold nanoparticles by solventevaporation method was established. The detailed structures of the assemblies were confirmed by absorption spectra and SEM.

P-8-13
Fabrication and Photoelectrochemical Properties of Multilayer Assemblies Consisting of Silver-nanoparticles, Polydiacetylene, and Polyions
T. Akiyama[1], A. Masuhara[2], Y. Matsuda[3], T. Arakawa[4], T. Munaoka[4], T. Onodera[3], H. Okikawa[3] and S. Yamada[4], [1]The University of Shiga Prefecture, [2]Yamagata Univ., [3]Tohoku Univ. and [4]Kyushu Univ. (Japan)
We attempted to fabricate multilayer assemblies, which consisted of Ag NPs, polydiacetylene, and polyions by the LbL technique. Furthermore, we evaluated the photon-to-current conversion efficiency of the multilayer assemblies fabricated on ITO electrodes.

P-8-15
Efficient Preparation of Size-Controlled Nanoparticles using Thin Film Laser Ablation in Water
M. Fukudome and H. Ikenoue, Kochi Nat`l Col. of Tech. (Japan)
We could successfully develop a novel method for efficient preparation of size-controlled nanoparticles with narrow size distribution using thin film laser ablation in water.

P-8-16
Degradation Mechanism for CLC Poly-Si n-TFTs under Low Vertical-Field HC Stress with Different Laser Annealing Powers
S. Y. Chang[1], M. C. Wang[1,2], Z. Y. Hsieh[2] and C. Chen[3], [1]Ming Hsin University of Science & Technology, [2]National Taipei Univ. of Tech. and [3]National Chiao Tung Univ. (Taiwan)
The CLC poly-Si n-TFT with various laser annealing powers was investigated in this research. The degradation mechanism of device under voltage stress is dominated by HCE at the low vertical field.

P-8-17
Polarized Thermoreflectance and Reflectance Study of ReS_2 and ReS_2:Au Single Crystals
T. P. Huang[1], D. Y. Lin[1], J. D. Wu[2] and Y. S. Huang[2], [1]National Changhua Univ. of Edu. and [2]National Taiwan Univ. of Sci. and Tech. (Taiwan)
We have presented optical characterization of ReS2 and ReS2:Au by using PTR and R measurements. The indirect band gaps and direct band edge excitonic transitions at various polarization angles have been observed. The temperature dependences, broadening parameters and doping effects are discussed.

P-8-19 (Late News)
Fabrication of coaxial p-copper oxide/n-ZnO nanowire photodiodes
H. T. Hsueh[1,2], S. J. Chang[1], F. Y. Hung[1] and T. J. Hsueh[2], [1]National Cheng Kung Univ. and [2]National Nano Device Labs. (Taiwan)
The authors report the fabrication of p-copper oxide/n-ZnO nanowire photodiodes. It was found that we can achieve Cu2O/ZnO, Cu4O3/ZnO and CuO/ZnO nanowire photodiode by changing the O2 flow rate. The responses were also discussed.

Area 9: Physics and Application of Novel Functional Devices and Materials
(14 Papers)

P-9-1
Full-dimensional analysis of coherent spin dynamics in a semiconductor
T. Inagaki[1,2], H. Kosaka[1,2], Y. Rikitake[3,2], H. Imamura[4,2], Y. Mitsumori[1,2] and K. Edamatsu[1], [1]Tohoku Univ., [2]CREST-JST, [3]Sendai National College of Technology and [4]AIST (Japan)
We demonstrate full-dimensional analysis of electron spin dynamics by applying the developed TKR method. The analysis clarified that the spin x-state, which is parallel to the applied magnetic field, only decays without the Larmor precession, and the spin lifetime of any prepared spin state are approximately equal to 600 ps without significant basis dependency.

P-9-2
Ultrasonic wave induced mechanoluminescence
N. Terasaki[1], H. Yamada[1] and C. N. Xu[2], [1]AIST and [2]JST (Japan)
Mechanoluminescent particles emit intensive light under application of mechanical stress. From the viewpoint of a ubiquitous light source, we have investigated mechanoluminescence induced by ultrasonic wave, non-destructive and non-inventive stimulation, and successfully detect it.

P-9-3
Effects of interface grading on electronic states and optical transitions in GaAb type-II quantum dots in GaAs
T. Kawazu[1] and H. Sakaki[1,2], [1]NIMS and [2]Toyota Technological Inst. (Japan)
We theoretically analyze the effects of the Sb/As intermixing on a GaSb/GaAs type-II QD system and discuss how the spatial overlap of holes and electrons and the PL intensity is affected by the intermixing.

P-9-4
Source Engineering for Tunnel Field-Effect Transistor: Elevated Source with Vertical Silicon-Germanium/Germanium Heterostructure
G. Han, P. Guo, Y. Yang, L. Fan, Y. S. Yee, C. Zhan and Y. C. Yeo, National Univ. of Singapore (Singapore)
Source engineering for TFET with in situ B-doped Si0.5Ge0.5 source was investigated. A Ge layer inserted beneath the Si0.5Ge0.5 source effectively increased the ION and subthreshold swing of the TFET due to the reduction of tunnel barrier and the suppression of B diffusion into Si channel.

P-9-5
NIS tunneling junction fabricated by superconducting Boron-doped diamond
R. Nomura[1], S. Kitagoh[1], M. Watanabe[1], Y. Takano[2], T. Yamaguchi[2] and H. Kawarada[1], [1]Waseda Univ. and [2]NIMS (Japan)
We fabricated Normal conductor ― Insulator ― Superconductor (NIS) tunneling junction operates with heavily boron doped diamond layer as superconductor. The typical characteristics of current-voltage and dI/dV-voltage are observed. We thought this junction has a potential to be a promising detector or some such devices.

P-9-6
Improved Characteristics of MOCVD Grown ZnO TFTs by Controlling VI/II Ratio of ZnO Film Growth and Using a Modified TFT Layer Structure
K. Remashan, Y. S. Choi, S. J. Park and J. H. Jang, GIST (Korea)
The incorporation of the MgZnO layer and the use of higher VI/II ratio grown ZnO channel greatly enhanced TFT performance in terms of μ_{FE}, S, and on/off current ratio. This is due to the larger grains in, and lower growth rate of the ZnO film.

P-9-7
High-Performance Polycrystalline Silicon Thin-Film Transistor with Nickel-Titanium Oxide by Sol-Gel Spin-Coating and Fluorine Implantation
S. C. Wu[1], T. H. Hou[1], S. H. Chuang[2], H. C. Chou[2], P. Y. Kuo[1], T. S. Chao[1] and T. F. Lei[1], [1]National Chiao Tung Univ. and [2]National Univ. of Kaohsiung (Taiwan)
A high-performance poly-Si TFTs is reported without additional hydrogenation or advanced phase crystallization techniques. Excellent electrical characteristics are attributed to the promising high-k NiTiO3 by sol-gel spin-coating and the trap passivation by fluorine implantation.

P-9-8
Correlating phonon frequency shift with magnetoelectric effect in the $PbTiO_3$-$CoFe_2O_4$ multiferroic system due to interfacial stress
C. Y. Tsai[1], T. C. Huang[2] and W. F. Hsieh[1,3], [1]National Chiao Tung Univ., [2]National Taiwan Normal Univ. and [3]National Cheng Kung Univ. (Taiwan)
We report on the correlation between local behavior of interfacial phonon and ferromagnetic properties in three multiferroic consisting of different geometric shapes of ferromagnetic CoFe2O4 (CFO) embedded in the ferroelectric matrix of PbTiO3 (PTO) by using micro-Raman spectroscopy and SQUID.

P-9-9
Light Enhancement of Si-Nanocrystals-Embedded SiOx film on Silicon-on-Insulator Substrate
C. C. Chen[1], Y. H. Lin[2], M. H. Shih[3], G. R. Lin[2] and H. C. Kuo[1], [1]National Chiao Tung Univ., [2]National Taiwan Univ. and [3]Academia Sinica (Taiwan)
We reported light enhancement from a Si-nanocrystals-embedded SiOx film on a silicon-on-insulator substrate in visible light range. Compared with SiOx film on a Si substrate, A strong emission from the SOI substrate was observed from SiOx film on SOI substrate was observed.

P-9-10
Multistep Electron Injection in a PtSi-Nanodots/Silicon-Quantum-Dots Hybrid Floating Gate in nMOSFETs
M. Ikeda, S. Nakanishi, N. Morisawa, A. Kawanami, K. Makihara and S. Miyazaki, Hiroshima Univ. (Japan)
The multistep electrons injection in an nMOSFET with a PtSi-NDs/Si-QDs hybrid floating FG has been demonstrated. This result can be interpreted in terms of the electron injection into the PtSi-NDs through the discrete charged states of Si-QDs.

P-9-11
Monolithic Integration of Ni-SPC Poly-Si TFTs and Lateral Large-grained Poly-Si TFTs
A. Hara, K. Kondo, T. Sato and T. Sato, Tohoku Gakuin Univ. (Japan)
In this paper, Ni-SPC poly-Si TFTs and lateral large-grained poly-Si TFTs were fabricated on different regions of a glass substrate, and then, the performance of each was evaluated.

P-9-12
Electric properties of SONOS memories with embedded silicon nanocrystals in nitride
M. C. Hsieh, T. Y. Chiang, H. A. Dai, C. C. Chen, C. H. Chiang, J. F. Wang, Y. J. Lin, J. Y. He, Y. N. Chen, T. S. Chao and J. F. Chen, National Chiao Tung Univ. (Taiwan)
Interface states at the SiO2/Si-substrate interface are identified by experiment and simulation. Embedded Si-NCs in nitride are confirmed as a formation of Si-quantum dots in nitride. The Si-NCs form quantum confined states above conduction band.

P-9-13
Analysis of MOSFET Electrometer Sensitivity by Radio-Frequency Reflection
M. Kawai, V. Singh, M. Nagasaka, H. Satoh and H. Inokawa, Shizuoka Univ. (Japan)
By the use of the RF reflection, electrometer consisting of 70-nm-gate MOSFET could operate at the speed of 25 MHz with a charge sensitivity of 5E-3 e/Hz^0.5 at room temperature. It was also found that the down scaling of the gate length is effective in improvement of the charge sensi-tivity.

P-9-14 (Late News)
Room-Temperature Number-Resolving Single-Photon Detection by SOI MOSFET
W. Du, H. Inokawa and H. Satoh, Shizuoka Univ. (Japan)
SOI MOSFET was evaluated as a single-photon detector. The device showed dark counts less than 0.02 cps even at 300 K, and the output waveforms exhibited clear separation of current levels, indicating the possibility of photon-number resolution. The recombination mechanism of the holes was also investigated, and indirect transition was suggested.

Area 10: Organic Materials Science, Device Physics, and Applications
(20 Papers)

P-10-1
A stacked organic/inorganic vapor barrier structure encapsulated flexible plastic substrates prepared using plasma-enhanced chemical vapor deposition
M. S. Jeng[1], C. S. Chuang[2], L. W. Lai[2], B. Y. Lin[1] and D. S. Liu[1], [1]National Formosa Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
A stacked organosilicon/SiOx layered-structure prepared by PECVD using the TMS monomer was applied to encapsulate the plastic substrate. An ultra-low WVTR was achieved from the PET substrate coated with a six-pair organosilicon/SiOx barrier structure.

P-10-2
Roll-type Micro-contact printing process with PDMS stamp for patterning conductive Metal Line with Ag ink
J. H. Kim, M. Y. Lee, Y. J. Park and C. K. Song, Dong-A Univ. (Korea)
In this paper, we fabricated the conductive metal line by roll type micro-contact printing with PDMS stamp using nano Silver ink. The ink transfer characteristic during printing was improved by optimizing a coating condition, inking speed, printing speed, printing pressure and Ag content. As a result, printed a line width of 30um, thickness of ~300nm, roughness less than 40nm.

P-10-3
Synthesis and Optical Properties of Polysilanes Containing Anthryl Groups
S. Ishibe, T. Mizuno and H. Tachibana, AIST (Japan)
Liner and network polysilane possessing anthlyl group were synthesized, and the effect of heat and/or treatment on UV-vis-NIR spectroscopy is investigated. The result indicates heat treatment afford lower energy shift of the polymer absorption.

P-10-5
Estimation of Electron Injection Barrier Height at Metal/ Polymer Interface by Internal Photoemission Spectroscopy and its Schottky Current Analysis
E. Itoh and S. Takaishi, Shinshu Univ. (Japan)
We have estimated the electron injection barrier height at metal/ polyfluorene based polymer interface by internal photoemission spectroscopy technique and current analysis as a function of electronegativity of cathode materials and the interfacial mid-gap states.

P-10-6
Extraction of Energy Density Profile of Bulk and Interface Trap States in Pentacene
S. H. Jeong and C. K. Song, Dong-A Univ. (Korea)
We extracted energy density of bulk and interface trap states in pentacene on PVP by using temperature dependent space charge limited current and temperature dependent transfer characteristics respectively. The bulk trap states exhibited a large state at 1.3 eV and the interface trap states also produced a large energy states at 1.2 eV.

P-10-7
Effect of Device Structure on Electrical Conduction of Terphenyl-based Molecule
T. Goto[1], H. Inokawa[2], Y. Ono[1], A. Fujiwara[1] and K. Torimitsu[1], [1]NTT Basic Res Labs. NTT Corp. and [2]Shizuoka Univ. (Japan)
A recent study of phenylene-based molecular devices has revealed many intriguing features. In this report, a phenylene-based molecule is selected, and the effect of device structure on electrical conduction is investigated.

P-10-8
High Efficiency Electrophosphorescence Red OLEDs Using a Thin BPY-OXD Cleaving Layer in an Ir-complex Doped Emitter Layer
C. H. Chen, K. R. Wang, Y. H. Tsai, S. F. Yen, P. Y. Su and C. F. Cheng, Cheng Shiu Univ. (Taiwan)
The authors demonstrate a considerable increase in current efficiency of Ir(piq)2(acac) doped phosphorescent organic red-light emitting device in which a thin Bpy-OXD layer acts as a cleaving layer. When a 5 nm Bpy-OXD layer divides the emitting layer (EML) into two sub-EMLs, a maximum luminance of 9830 cd/m2 and current efficiency of 4.36 cd/A were obtained, which is higher than that of the device without it.

P-10-9
Oriented PFO Films Dye-Doped for Whitening of Polarized EL Devices
C. Heck, T. Mizokuro and N. Tanigaki, AIST (Japan)
We report on the combination of vapor transportation and friction transfer methods for doping linear fluorescent dyes into oriented polymer films. The ultimate aim is to produce white polarized EL devices by doping an orange dye into a blue emitting oriented PFO film in a way that the dye orientation is parallel to the orientation of the PFO film.

P-10-10
Application of a Porous Titanium Film to a Counter Electrode of a Dye-sensitized Solar Cell
M. Rahman, R. Kojima, M. E. F. Fihry, Y. Kimura and M. Niwano, Tohoku Univ. (Japan)
Here we developed a new counter electrode with porous Ti film for dye sensitized solar cells. It is seen that DSC with porous Ti shows better performance than that of usual Pt counter electrode.

P-10-11
Annealing Effects on Polymer Solar Cells with High Polythiophene- fullerene Concentrations
C. S. Ho[1], E. L. Huang[1], W. C. Hsu[1], C. S. Lee[2], Y. N. Lai[1] and W. H. Lai[1], [1]National Cheng Kung Univ. and [2]Feng Chia Univ. (Taiwan)
Composites of conjugated P3HT and PCBM with 3 and 5 wt% concentrations are prepared to study the thermal annealing effect at different temperatures. In the case of 3 wt% film, absorption spectrum shows a small increase of intensity upon annealing between 110 and 150°C whereas an obvious degradation as the temperature is higher than 170°C.

P-10-12
Construction and Evaluation of Organic Solar Cells Using a Spray-Coating Method
Y. Murakami, H. Ishihara, T. Mizutani, K. Kojima and S. Ochiai, Aich Inst. of Tech (Japan)
In this study, we fabricated orgnic solar cells by spray-coating method. As a result, the short circuit current density is 2.07mA/cm^2, the open circuit voltage is 0.45V, and the power conversion efficiency 0.35%.

P-10-13
Silver Nanoparticle-Assisted Photocurrent Generation in Polythiophene-Fullerene Thin Films
J. You, T. Arakawa, H. Yoneda, T. Akiyama and S. Yamada, Kyushu Univ. (Japan)
We have tried to use LSPR of silver nanoparticles in order to enhance light absorption and resultant photocurrent generation from polythiophene-fullerene thin films. The effects of LSPR were verified.

P-10-14
Performance Improvement of OTFT by controlling Crystal Morphology of TIPS-Pentacene
M. J. Kim, G. S. Ryu, J. W. Hwang and C. K. Song, Dong-A Univ. (Korea)
In this paper, we controlled crystal morphology of TIPS pentacene by adjusting the moving velocity of edge contact line of droplet to be matched with the velocity of crystal formation at the edge.

P-10-15
Numerical Simulation of Contact Resistance in Organic Field-Effect Transistors
S. Nishigami, T. Nagase, T. Kobayashi and H. Naito, Osaka Prefecture Univ. (Japan)
We have carried out the two dimensional simulation of top-contact and bottom-contact OFETs in the presence of localized states and disorder regions in order to investigate the origin of contact resistance .

P-10-16
Frequency Response of Polymer Field-Effect Transistors Fabricated by a Self-Aligned Method
H. Hatta[1], Y. Miyagawa[1], T. Nagase[1,2], T. Kobayashi[1,2], S. Murakami[3], M. Watanabe[4], K. Matsukawa[4] and H. Naito, [1]Osaka Prefecture Univ. , [2]The Res. Inst. for Molecular Electronic Device, [3]Tech. Res. Inst. of Osaka Prefecture and [4]Osaka Municipal Technical Res. Inst. (Japan)
We have investigated frequency characteristics of po-lymer-based OFETs fabricated by the self-aligned method. The impedance spectroscopy of the self-aligned OFETs reveals the three-orders-of-magnitude decrease in parasitic capacitance from conventional OFETs and frequency de-pendence of channel formation process in OFETs.

P-10-17
UV-patternable polymer dielectric for organic thin film transistors
C. M. Wu, H. T. Wang, S. H. Su and M. Yokoyama, I-Shou Univ. (Taiwan)
The OTFTs using a UV-patternable polymer material, mr-UVCur06, as the gate dielectric have been fabricated and characterized. The pattern resolution can reach 3 μm and the pentacene-based OTFTs exhibit an on-off ratio around 105.

P-10-18
Improvement of Pentacene Organic Thin-Film Transistor Considering Quantum Effect
A. Heya and N. Matsuo, Univ. of Hyogo (Japan)
Carrier transport in organic thin-film transistors (OTFTs) was investigated by using pentacene OTFT and sample for vertical transport evaluation with various film thickness from 1 to 50nm. The Ion of 3nm OTFT was higher than that of 50nm OTFT. It is considered that the triangle potential was formed at interface between pentacene and SiO2.

P-10-19
Temperature Dependence of Charge Transport in Polythiophene-Based Field-Effect Transistors
M. Yoshikawa[1], T. Banno[1], T. Nagase[1], T. Kobayashi[1], S. Murakami[2] and H. Naito, [1]Osaka Prefecture Univ. and [2]Tech. Res. Inst. of Osaka Prefecture (Japan)
Field-effect transistor (FET) measurements of Organic FETs based on regioregular polythiophenes in a wide temperature range from 9 K to 300 K have been performed to investigate charge transport mechanism in OFETs.

P-10-20
Reverser off-set Printing Process for Gate Electrodes of OTFT-Backplane
J. E. Park, M. Y. Lee and C. K. Song, Dong-A Univ. (Korea)
For gate electrodes and lines of OTFT-backplane, first, screen printing was applied to uniformly deposit Ag ink thin film over the area of substrate, and then etching resist was patterned by reverse off-set printing. The final gate electrodes were obtained through etching Ag ink layer. By using this process the line feature of 50 um was obtained with the resistance of 1 W/square over 6" substrate.

P-10-21
Wettability Improvement by Silica Nanoparticle Addition in Solution-Processed TIPS-Pentacene Field-Effect Transistors
S. Yamazaki[1,2], T. Hamada[2], S. Tokai[1], M. Yoshikawa[2], T. Nagase[2,3], T. Kobayashi, Y. Michiwaki[4], S. Watase[5], M. Watanabe[5], K. Matsukawa[5] and H. Naito[2,3], [1]Citizen Holdings Co., LTD., [2]Osaka Prefecture Univ., [3]Res. Inst. Molecular Electronic Dev., [4]Fuso Chemical Co., LTD. and [5]Osaka Municipal Technical Res. Inst. (Japan)
We report the improvement of the wettability of soluble organic semiconductors of TIPS-pentacene on hydrophobic poly(methylsilsesquioxane) gate dielectrics by the addition of silica nanoparticles. Silica nanoparticle addition also allows the direct patterning with ink-jet process.

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)
(13 Papers)

P-11-1
Detection of Antigen-Antibody Reaction Using Si Ring Optical Resonators Functionalized with an Immobilized Antibody-Binding Protein
M. Nishida, M. Fukuyama, Y. Abe, Y. Amemiya, T. Ikeda, A. Kuroda and S. Yokoyama, Hiroshima Univ. (Japan)
Rapid immobilization technique for variety of antibodies on Si-ring optical-resonator biosensor has been developed using Si-tagged protein A, which leads to the integrated high-throughput biosensors. Green fluorescent protein and prostate specific antigens were actually detected

P-11-2
Control of Supported Lipid Bilayer Self-Spreading through Nanogap by Local Electric Field
Y. Kashimura, K. Furukawa and K. Torimitsu, NTT Basic Res. Labs. NTT Corporation (Japan)
We demonstrated that the development of the self-spreading lipid bilayers could be controlled by the temporal switching of the electric field applied to a nanogap.

P-11-3
Surface Infrared Spctroscopic Study of ATP Synthesis in Mitochondria
Y. Aonuma[1], R. Yamaguchi[1], M. Abe[1], A. Hirano-Iwata[2], Y. Kimura[1], Y. Shinohara[3] and M. Niwano[1,2], [1]Tohoku Univ., [2]JST and [3]Univ. of Tokushima (Japan)
We have monitored ATP synthesis in isolated mitochondria by using IRAS in the multiple internal reflection (MIR) geometry. Through real-time monitoring of oxidative phosphorylation in mitochondria, it is demonstrated that conversion processes between ADP and ATP can be detected by the IR spectral changes of phosphate groups in adenine nucleotides.

P-11-4
Rapid Biosensing Platform based on Monitoring Changes in the Optical Reflectance of Porous Silicon due to Penetration by Functionalized Superparamagnetic Beads
P. J. Ko[1,2], Y. Morimoto[1], R. Ishikawa[1,2], B. Cho[3], H. Sohn[3] and A. Sandhu[1,2,4], [1]Tokyo Tech, [2]Tokyo Tech. Global COE program, [3]Chosun Univ. and [4]Toyohashi Univ. of Tech. (Japan)
We demonstrated the feasibility of a novel biosensing method utilizing superparamagnetic beads for medium varying index reflectivity of PSi.

P-11-5
Differential setup of light-addressable potentiometric sensor with an enzyme reactor
K. Miyamoto[1], M. Yoshida[1], T. Wagner[1], Y. Tatsuo[1] and M. J. Schöning[2,3], [1]Tohoku Univ., [2]Aachen Univ. of Applied Sciences and [3]Research Centre Jülich (Japan)
The light-addressable potentiometric sensor was applied for the differential measurement in flow channels to detect enzymatic reactions. The differential measurement was demonstrated to suppress the drift in the sensor signal.

P-11-6
Optimization of Urea-EnFET Based on Ta_2O_5 Layer with Post Annealing
T. C. Yu[1], C. E. Lue[1], W. Y. Chuang[1], C. M. Yang[2], D. Pijanowska[3] and C. S. Lai[1], [1]Chang Gung Univ., [2]Device Section, Department of WAT and Devices, Inotera Memories Inc. and [3]Institute of Biocybernetics and Biomedical Engineering, Polish Academy of Sciences (Taiwan)
In this study, the highest performance of pH sensitivity, hysteresis, drift, and light induced drift, were observed on Ta2O5-ISFET with post N2 annealing. In addition, for the application of urea detection, the best sensing properties were also performed on the EnFET based on the annealed Ta2O5 layer.

P-11-7
A study of olfactory signal sensing with FET biosensor
M. S. Kim[1], W. J. Cho[1], J. Y. Choi[2] and J. O. Lim[2], [1]Kwangwoon Univ. and [2]Kyungpook National Univ. (Korea)
In this study, we fabricated and investigated field effect transistors (FETs) with living olfactory neural cells of rat pup (day 0.5~1) for real-time diagnosis of chronic obstructive pulmonary disease.

P-11-8
Impact of Quantum Mechanical Effects on Silicon Nanowire Biosensors
B. K. Y. Lu and P. Su, National Chiao Tung Univ. (Taiwan)
In this work, we investigate the impact of Quantum mechanical effects on Si-NW biosensors. Our results indicate that by exploiting the Q.M. effect, the sensitivity of Si-NW biosensors can be enhanced.

P-11-10
Novel Reference Electrode-Insulator-Nitride-Oxide-Semiconductor (RINOS) Structure with Sm_2O_3 Sensing Membrane for pH-sensor Application
H. Y. Shih, J. C. Wang, T. F. Lu, C. S. Lai, C. H. Kao and T. M. Pan, Chang Gung Univ. (Taiwan)
In this article, a novel RINOS device with ONO (oxide- nitride-oxide) structure was proposed with the Sm2O3 as the sensing membrane. Through voltage stress, the great improvement on the pH-sensitivity compared with the fresh sample is obtained.

P-11-11
Compact Electro-Magnetically Operated Microfluidic System for Detection of sub-200 nm Magnetic Labels for Biosensing without External Pumps
T. Takamura[1], Y. Morimoto[1] and A. Sandhu[1,2], [1]Tokyo Tech and [2]Toyohashi Univ. of Tech. (Japan)
We demonstrated a novel biosensing protocol based on mon-itoring the electrostatic manipulation and magnetic capture of 2.8 micrometer diameter superparamagnetic columnar beads used as a probe by the 130-nm-diameter target beads in pumpless liquid microchannels.

P-11-12
Monodisperse silver nanoparticles of controlled size for biomedical applications
A. P. Z. Stevenson[1], D. B. Bea[2], S. A. Contera[1], A. I. Cerbeto[2] and S. Trigueros[1], [1]Univ. of Oxford and [2]National Center for Scientific Research (UK)
We present the characterization of monodisperse silver, silver-functionalized and silver-alloy nanoparticles of controlled size synthesized via a novel one-step optimization of the citrate-reduction method.

P-11-13
Fabrication of various metallic nanogap electrodes using molecular ruler technique
T. Nishino[1,2], R. Negishi[3], H. Tanaka[3], T. Ogawa[3] and K. Ishibashi[1,2], [1]RIKEN, [2]Chiba Univ. and [3]Osaka Univ. (Japan)
In addition to conventional nanogap electrodes, Au-Au and Pt-Pt, we demonstrated the fabrications of Al-Al, Nb-Nb, Co-Co, and asymmetric Nb-Co nanogap electrodes using molecular ruler technique the methods of which were improved. We show these methods and single electron transport properties of nanogap applying device.

P-11-14
Study of electronic structure of catalyst at Triple Phase Boundary in the cathode catalyst layer of PEFCs by using computational chemistry method
D. Kim, H. Kobayashi, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
It is necessary to design high-efficient catalyst for implementation of polymer electrolyte fuel cells expected as a sustainable energy technology. It is important to study about the Triple Phase Boundary of catalyst layer and estimate the effect of interface on catalyst properties. In this study, we constructed the TPB model and analyzed the catalyst properties by using computational chemistry method.

Area 12: Spintronic Materials and Devices
(6 Papers)

P-12-1
Power-Aware Bit-Serial Binary Content-Addressable Memory Using Magnetic-Tunnel-Junction-Based Fine-Grained Power-Gating Scheme
S. Matsunaga, M. Natsui, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)
Ultra-low-standby-power bit-serial binary content-addressable memory (CAM) is proposed by using a nonvolatile MTJ-based fine-grained power-gating scheme. Since a single MTJ device is used as not only a storage element, but also a logic-operation element, 1T-1R CAM cell is implemented with simplicity of bit-cell level fine-grained power gating.

P-12-2
Fan-out Value in a Current-Field Driven Spin Transistor
K. Konishi[1], T. Nozaki[1], H. Kubota[2], A. Fukushima[2], S. Yuasa[2], M. Shiraishi[1] and Y. Suzuki[1], [1]Osaka Univ. and [2]AIST (Japan)
We proposed novel type of spin transistor, which is driven by current induced magnetic field. We obtained fan-out of 1.2 in this device with an assisting ac magnetic field.

P-12-3
Operational Conditions of Proposed Spin-Photon Memory
V. Zayets, H. Saito, S. Yuasa and K. Ando, AIST (Japan)
High-speed non-volatile optical memory was proposed. It was proved that the recording speed of the memory can reach 2.2 TBit/sec. The low-resistivity contact between Fe nanomagnet and n-GaAs was successfully fabricated.

P-12-4
HCP-disordered CoPt electrode and exchange control layer for MgO based perpendicular magnetic tunnel junctions
W. Lim, S. C. Oh, J. H. Jeong, W. J. Kim, Y. H. Kim, H. J. Shin, J. E. Lee, S. Choi and C. Chung, Samsung Electronics Co., Ltd. (Korea)
This letter presents a study of the perpendicular magnetic tunnel junction consisting of HCP-disordered CoPt electrode and non-magnetic exchange control layer (NM ECL). The insertion of NM ECL such as Ti, Mg, Ru, or Al improved the texture of CoFeB/MgO as well as enhanced the perpendicular magnetization anisotropy of CoPt/CoFeB.

P-12-5
Co Doping Enhanced Giant Magnetocaloric Effect In $Mn_{1-x}Co_xAs$ Films Epitaxied On GaAs
P. Xu, S. Nie, K. Meng, S. Wang, L. Chen and J. Zhao, State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences (China)
We found that the Co-doped MnAs films grown on GaAs exhibit enhanced magnetocaloric effect around room temperature with transition temperature tunable by varying Co content, which may be applied in construction of layered magnetic regenerator refrigerators with drastically enhanced refrigerating power.

P-12-6
Magnetic properties of quaternary magnetic semiconductor (Cd,Mn,Cr)Te grown by MBE
K. Ishikawa and S. Kuroda, Univ. of Tsukuba (Japan)
The magnetic properties of a quaternary DMS compound (Cd,Mn,Cr)Te were investigated. Thin films of $Cd_{1-x-y}Mn_xCr_yTe$ with a fixed Mn content $x \sim 0.2$ and varied Cr contents in the range of $y = 0 \sim 0.07$ were epitaxially grown on a GaAs (001) substrate by MBE. In the magnetization measurements, a ferromagnetic behavior, such as hysteretic loops in the *M-H* curves, as well as superparamagnetic features such as the blocking phenomenon in the *M-T* curves, were observed in $Cd_{1-x-y}Mn_xCr_yTe$ containing Cr contents less than 1%. The paramagnetic Curie temperature Θ_p changes its sign from negative to positive with the incorporation of Cr. These results suggest that the interaction between Mn spins becomes ferromagnetic due to the presence of a small amount of Cr.

Area 13: Application of Nanotubes, Nanowires, and Graphene
(13 Papers)

P-13-1
Operation Mechanism of Single-Wall Carbon Nanotube Network FET Studied by Scanning Gate Microscopy
N. Aoki, T. Yahagi, K. Maeda and Y. Ochiai, Chiba Univ. (Japan)
SWNT network FET has been observed by a high resolution SGM. The SGM responses are obtained only at some specific junctions of SWNTs in the channel region. Such junctions would play an important role for the FET operation.

P-13-2
Simple Fabrication Technique for an Array of Field-effect Transistors Using High-quality as-grown Single-walled Carbon Nanotubes from Dip-coated Catalyst by Substrate Surface Modification
S. Aikawa[1,2], R. Xiang[1], E. Einarsson[1], S. Chiashi[1], J. Shiomi[1], E. Nishikawa[2] and S. Maruyama[1], [1]Univ. of Tokyo and [2]Tokyo Univ. of Sci. (Japan)
We selectively coated catalyst at the edge of pre-formed electrode by using self-assembled monolayer. An array of field-effect transistor having an as-grown single-walled carbon nanotube from dip-coated catalyst was fabricated and evaluated the properties.

P-13-3
Electrical Performance Improvement of Carbon Nanotube Network Transistors by Direct Microwave Treatment
J. Y. Han[1], U. J. Kim[2] and W. Park[1], [1]Hanyang Univ. and [2]Samsung Advanced. Inst. of Tech. (Korea)
This is about the I-V improvement of carbon nanotube network transistor using microwave treatment. Through this method, we dramatically increased on-off ratio of carbon nanotube transistor.

P-13-4
DFT Study on the Adsorption and Dissociation of Hydrogen Peroxide on Fe-filled Single-walled Carbon Nanotubes
J. Moreno[1,2], M. David[2], T. Roman[1], M. Sakaue[1] and H. Kasai[1], [1]Osaka Univ. and [2]De La Salle Univ. (Japan)
The adsorption possibilities for hydrogen peroxide on Fe-filled single-walled carbon nanotubes were investigated through density functional theory calculations. Results indicated molecular adsorption followed by dissociative chemisorption where hydrogen peroxide dissociated into hydroxyl radicals.

P-13-5
Investigation of UV Polymerized Fullerene Nano Whisker by ESR and FET Characteristics
T. Doi[1], K. Koyama[1], N. Aoki[1], J. P. Bird[2] and Y. Ochiai[1], [1]Chiba Univ. and [2]Univ. at Buffalo (Japan)
We have studied on UV polymerized FNW-FET which remain to perform in air. The results of electron transport qualitatively correspond with ESR results which FNW polymer is closer to metallic.

P-13-6
Dependency of Young's modulus on diameter in Crystalline C_{70} Nanotubes
T. Tokumine[1], K. Miyazawa[2] and T. Kizuka[1], [1]Univ. of Tsukuba and [2]National Institute for Material Science (Japan)
We performed bending tests of individual C70 NTs by in situ TEM. From the measurements of the force-flexure relationships of the C70 NTs, the Young's modulus was estimated to be 61-110 GPa.

P-13-7
Epitaxial Graphene Field Effect Transistors on SiC substrate with Polymer Gate Dielectric
M. H. Jung, H. Handa, R. Takahashi, H. Fukidome and M. Suemitsu, Tohoku Univ. (Japan)
We investigated the electrical characteristics of the graphene FET with a polymer gate dielectric on SiC substrate. The graphene FET shows negative Vdirac shift and a carrier mobility of 580 cm^2/Vs.

P-13-8
Study on the graphene transfer process from graphitized SiC substrates
S. K. Lim[1], C. H. Cho[1], S. Y. Lee[1], H. J. Hwang[1], C. G. Kang[1], Y. G. Lee[1], J. Ahn[2] and B. H. Lee[1], [1]Gwangju Inst. of Sci.and Tech. and [2]Hanyang Univ. (Korea)
Graphene has attracted a great deal of attention due to excellent electrical properties and unique physical charac-teristics. However, the physical and chemical exfoliation of graphite can produce only a tiny piece of graphene. Thus, the processes to fabricate a large area, high quality, single layer graphene have been studied intensively.

P-13-10
Ellipsoidal Band Structure Effects on Maximum Ballistic Current in Silicon Nanowires
N. Mori[1,3], H. Minari[1,3], S. Uno[2,3] and J. Hattori[2,3], [1]Osaka Univ., [2]Nagoya Univ. and [3]CREST-JST (Japan)
An isotropic effective-mass approximation is often used for calculating the subband levels in a silicon nanowire (SiNW) with circular cross-section. In the present study, we investigate the validity and limitation of the isotropic approximations by comparing the maximum ballistic current densities in SiNWs.

P-13-12
Co-existence of Random Telegraph Noise and Single-Hole-Tunneling State in Gate- All-Around PMOS Silicon Nanowire Field-Effect-Transistors
B. H. Hong[1], S. J. Lee[1], S. W. Hwang[1], Y. Y. Lee[2], D. Ahn[2], K. H. Cho[3], K. H. Yeo[3], D. W. Kim[3], G. Y. Jin[3] and D. Park[3], [1]Korea Univ., [2]Univ. of Seoul and [3]Samsung Electronics Co., Ltd. (Korea)
we report the co-existence of RTN and single hole tunneling (SHT) state in a PMOS gate-all-around (GAA) silicon nanowire field effect transistors (SNWFWTs). We successfully identify dual SHT states which are switching between themselves by single hole trapping of a hole trap state.

P-13-13
Performance Comparisons of Schottky Barrier Transistors Using Si-, Ge- and Ge-Si Core-Shell Nanowires as Channels
J. Pu, L. Sun and R. Han, Peking Univ. (China)
The characteristics of Si-, Ge- and Ge-Si core-shell nanowire Schottky barrier transistors are simulated. For core-shell devices, most holes tunnel at the source near the heterojuction and transport in the Ge core region, and the drain current is relatively insensitive to barrier heights of source/drain contact.

P-13-15
Enhanced Efficiency of ZnO Nanowires Based Dye-Sensitized Solar Cells with Hetrosensitizer
P. H. Wang[1], S. J. Wang[1], K. M. Uang[2], T. M. Chen[2], P. R. Wang[1], T. C. Wang[1] and R. M. Ko[1], [1]National Cheng Kung Univ. and [2]Wufeng Inst. of Tech. (Taiwan)
In this work, to increase PCE, we report a tandem structure with two different sensitizer dyes (hetrosensitizer) as well as ZnO-NWs by a simple hydrothermal growth method for DSSCs.

P-13-17
Synthesis of Co-Doped Fullerene Nanowhiskers and Cobalt-Encapsulated Carbon Nanocapsules
D. Matsuura[1], K. Miyazawa[2] and T. Kizuka[1], [1]Univ. of Tsukuba and [2]National Institute for Material Science (Japan)
It was found that (1) Co-doped FNWs can be synthesized by the liquid-liquid interfacial precipitation method, and (2) Co- and Co_2C-encapsulated CNCs can be synthesized by heating of Co-doped FNWs in a vacuum.

Area 14: Photovoltaics & Power Semiconductor Devices
(12 Papers)

P-14-1
Lateral High-Voltage 4H-SiC MOSFETs
W. S. Lee[1], C. W. Lin[1], M. S. Yang[1], C. F. Huang[1], J. Gong[2] and Z. Feng[3], [1]National Tsing Hua Univ., [2]TongHai Univ. and [3]University of South Carolina (Taiwan)
The characteristics of lateral high-voltage 4H-SiC MOSFETs built on the Si-face of a 4H-SiC semi-insulating substrate are reported. DIBL effect in these devices is also investigated.

P-14-2

First Principles Calculations on CSL Grain Boundary Impurities in Multicrystalline Silicon

A. Suvitha, N. S. Venkataramanan, R. Sahara, H. Mizuseki and Y. Kawazoe, Tohoku Univ. (Japan)

We have carried out DFT studies on the Sigma 5(210) and Sigma 9 (221) CSL GB of multicrystalline silicon. Energy calculation shows substitution site is the preferred for the transition metals in the GB region of Sigma 5 whereas, in the Sigma 9 GB plane except chromium other metal favors segregation at both the sites.

P-14-4

Material Research on High Quality Passivation Layers with Controlled Fixed Charge for Crystalline Silicon Solar Cells

T. Tachibana[1], T. Sameshima, Y. Iwashita[1,2], Y. Kiyota, T. Chikyow[2], H. Yoshida[3,4], K. Arafune, S. Satoh[3,4] and A. Ogura[1,4], [1]Meiji Univ., [2]NIMS, [3]Univ. of Hyogo and [4]CREST-JST (Japan)

In this study, we evaluated and controlled positive and negative fixed charge in the binary composition oxide thin layers fabricated by the combinatorial pulsed laser deposition

P-14-5

a-Si:H Solar Cell with Hexagonal Nano-Cylinder Array on Glass Substrate

W. C. Tu, Y. T. Chang, C. H. Yang, D. J. Yeh, C. I. Ho and S. C. Lee, National Taiwan Univ. (Taiwan)

A simple method of light trapping in a-Si:H solar cells was investigated. By nanosphere lithography, we patterned hexagonal nano-cylinder array on the glass substrate and reported 29% efficiency enhancement compared to the flat solar cell.

P-14-6

Application of sputtered $ZnO_{1-x}S_x$ buffer layer for $Cu(In, Ga)Se_2$ solar cells

A. Okamoto, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan)

We have applied the $ZnO_{1-x}S_x$ by co-sputtering of ZnO and ZnS, which should have high controllability of the compositional ratios of O and S for the buffer layers of $Cu(In,Ga)Se_2$ solar cells.

P-14-7

Surface morphology and device performance of $CuInS_2$ solar cells prepared by single and two step evaporation methods

S. Fukamizu, T. Kondo, Y. Oda, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan)

$CuInS_2$(CIS) films were fabricated by two-step evaporation methods that Cu-rich Cu-In-S deposited at 50 ^{o}C in the first step and In-S deposited in the second step to control good flatness and In-rich CIS films.

P-14-8

Improvement of Film Quality in CIS Thin Films Fabricated by Non-vacuum, Nanoparticles-based Approach

Y. Zhang[1,2], M. Ito[2], A. Yamada[1] and M. Konagai, [1]Tokyo Tech and [2]Toppan Printing Corp., Ltd. (Japan)

A new approach to fabricate a high quality CIS thin film has been developed.The fabrication was carried out through using copper selenide (Cu-Se) nanoparticles, indium selenide (In-Se) nanoparticles, with thiourea.

P-14-9

Interpretation of Crossover in J-V Characteristics of $Cu(In,Ga)Se_2$ Solar Cell Using Lift-off Process

Y. Abe, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan)

Although the photo J-V characteristics of the CIGS solar cell using a lift-off process were particular shape, this cause has not been interpreted yet. We investigated thebehavior of photocurrent of the CIGS solar cells.

P-14-10

Simulation of temperature characteristics of InGaP/InGaAs/Ge triple-junction solar cell under concentrated light.

Y. Sakurada, Y. Ota and K. Nishioka, Univ. of Miyazaki (Japan)

Temperature characteristics of InGaP/InGaAs/Ge triple-junction solar cell under concentrated light conditions were calculated using SPICE. We can accurately estimate the temperature characteristics of triple junction solar cells under concentrated light.

P-14-11

Shallow Carrier Trap Levels in GaAsN Investigated by Photoluminescence

M. Inagaki[1], H. Suzuki[2], A. Suzuki, K. Mutaguchi, A. Fukuyama, N. Kojima[1], Y. Ohshita and M. Yamaguchi, [1]Toyota Technological Inst. and [2]Univ. of Miyazaki (Japan)

The shallow carrier trap levels in GaAsN grown by chemical beam epitaxy were investigated by the temperature dependence of photoluminescence spectra. N-related trap level is ~17 meV below band edge with independently N composition.

P-14-12

Enhancement of the efficiency of GaAs-based solar cells by sol-gel-synthesized ZnO nanowire arrays as the antireflection layer

Y. K. Su, C. Y. Cheng, J. Y. Huang and Y. W. Lee, National Cheng Kung Univ. (Taiwan)

In recent decades, global-warming issues coupled with high oil prices, and photovoltaic is one of green energies which provide electricity without any pollution. We would like to develop high-efficiency and low-cost photovoltaics.

P-14-13

Fabrication of high quality TiO_2 thin films for high conversion efficiency dye-sensitized solar cells by multiple electrophoresis depositions

W. H. Chiu[1], K. M. Lee[2] and W. F. Hsieh[1,3], [1]National Chiao Tung Univ., [2]Indus. Tech. Res. Inst. and [3]National Cheng Kung Univ. (Taiwan)

A multiple electrophoretic deposition (EPD) for binder-free deposition has been successfully developed to improve the TiO2 photoanode quality, and the device gave a high efficiency up to 6.63% under AM 1.5G one sun irradiation.

Friday, September 24

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A-6: Organic Transistors and Device Physics Ⅰ (Area 10)

(9:00-10:45)
Chairs: H. Maeda (DNP)
H. Kajii (Osaka Univ.)

9:00 A-6-1 (Invited)
Inkjet Printing of Organic Thin-Film Transistors
T. Kawase, S. Moriya, K. Nakamura, K. Inoue, K. Nakamura and T. Aoki, Seiko Epson Corp. (Japan)
The application of inkjet printing to the fabrication of organic TFT backplanes are reviewed. A hybrid approach in which inkjet printing is combined with photolithography is explained in detail. The phenomena happening in the inkjet printing of semiconductor are also discussed.

9:30 A-6-2
Organic CMOS Logic Papers with In-Field User Customizability
T. Sekitani[1], K. Ishida[1], N. Masunaga[1], R. Takahashi[1], S. Shino[2], U. Zschieschang[3], H. Klauk[3], M. Takamiya[1], T. Sakurai[1] and T. Someya[1], [1]Tokyo Univ. , [2]Mitsubishi Paper Mills Ltd. and [3]Max Planck Inst. for Solid State Research (Japan)
We report the manufacturing of user-customized logic paper—paper in which organic complementary logic cells are embedded. The logic paper provides on-demand in-field customizability to the users by making use of commercially available inkjet printing.

9:45 A-6-3
Effects of an Interface Dipole Monolayer on Pentacene Organic Field-Effect Transistors
W. Ou-Yang, K. Lee, W. Martin, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
Effect of an aligned dipole monolayer with opposite mole-cular orientation on pentacene OFET performance was investigated. We found the monolayer greatly shifted threshold voltage, mobility and on/off ratio and these changes depended on the molecular orientation.

10:00 A-6-4
Organic transistors and circuits with parylene gate dielectric manufactured using subfemtoliter inkjet
T. Yokota, Y. Noguchi, Y. Kato, T. Sekitani and T. Someya, Tokyo Univ. (Japan)
We fabricated organic TFTs and complementary ring oscillator circuits by subfemtoliter inkjet printing. The TFTs have a channel length smaller than 10 μm, a channel width 500 μm, and the 3 μm-linewidth Ag source/drain electrodes.

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B-6: Junction Technology (Area 1)

(9:00-10:45)
Chairs: B. Mizuno (UJT Lab. Inc.)
S. Migita (AIST)

9:00 B-6-1 (Invited)
Overview and Challenges in Source/Drain Formation Technology in High Performance Transistors.
K. Suguro, Toshiba Corp. (Japan)
Source and drain formation technologies which are required in next generation Si devices such as memory LSIs and system LSIs are overviewed and the new challenge for the future are discussed in this paper.

9:30 B-6-2
Raised S/D for Advanced Planar MOSFET devices: Challenges and Applications for the 20nm Node and Beyond
N. Loubet[1], P. Khare[1], S. Mehta[2], S. Ponoth[2], B. Haren[2], Q. Liu[1], K. Cheng[2], J. Kuss[2], T. Adam[2], B. Doris[2], V. Paruchuri[2], W. Kleemeier[1] and R. Sampson[1], [1]STMicroelectronics and [2]IBM (USA)
As transistor physical dimensions continue to scale, RSD epitaxy integration presents new challenges in term of loading effects, facet reproducibility and control. In this paper, the feasibility and integration of flat and faceted RSD silicon epitaxy are investigated.

9:50 B-6-3
Raman Spectroscopy Measurement of Silicidation Induced Stress in Si and its Impact on Performances of Metal Source/Drain MOSFETs
S. Migita, V. Poborchii, T. Tada, Y. Morita, W. Mizubayashi and H. Ota, AIST (Japan)
Silicidation induced stress is examined by Raman spectroscopy. It is found that silicidation induces tensile stress in Si channel, and brings opposite temperature dependences of N-type and P-type metal S/D MOSFETs.

10:10 B-6-4
Accurate Measurement of Silicide Specific Contact Resistivity by Cross Bridge Kelvin Resistor for 28 nm CMOS technology and Beyond
K. Ohuchi, N. Kusunoki and F. Matsuoka, Toshiba America Electronic Components, Inc. (USA)
It is confirmed that specific-contact-resistivity measurement resolution by using modified cross-bridge Kelvin resistor is extended to 10^{-9} Ω-cm^2, and experimentally found 28nm-CMOS-technology realizes $1.1x10^{-8}$ and $7.8x10^{-9}$ Ω-cm^2 for n+ and p+ source/drain, respectively.

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C-6: Advanced CMOS Technology (Area 3)

(9:00-10:45)
Chairs: T. Hase (Renesas Electronics Corp.)
B. Doris (IBM)

9:00 C-6-1 (Invited)
Extremely-Thin SOI for Mainstream CMOS:Challenges and Opportunities
A. Khakifirooz, K. Cheng, A. Kumar, P. Kulkarni, S. Ponoth, B. S. Haran, S. Mehta, J. Cai, A. Byrant, J. Kuss, L. F. Edge, H. Jagannathan, Z. Ren, A. Reznicek, T. Adam, H. He, A. Kimball, S. Kanakasabapathy, S. Schmiz, S. Holmes, A. Majumdar, B. Jagannathan, D. Yang, A. Upham, S. C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, Z. Zhu, L. H,. Vanamurth, J. Faltermeier, S. Fan, D. Horak, T. Hook, V. Narayanan, V. Paruchuri, H. Bu, D. K. Sadana, P. Kozlowsk, B. Doris, D. McHerron, W. Haensch, M. Khare, E. Leobondung, J. O'Neil and G. Shahidi, IBM Research (USA)
Extremely thin SOI (ETSOI) is a viable option for future CMOS scaling owing to superior short-channel control and immunity to random dopant fluctuation. However, challenges of ETSOI integration have so far hindered its adoption for mainstream CMOS. In this talk we review some of these challenges and possible solutions. We will also review some of the unique opportunities offered by ETSOI technology.

9:30 C-6-2
Variability in Variable-Body-Factor Silicon-on-Thin-Box MOSFETs (SOTB MOSFETs)
Y. Yang, G. Du, R. Han and X. Liu, Peking Univ. (China)
A side-gate is used in the variable-body-factor SOTB to adjust the body-factor, which will, however, disturbs the variability performance of the device. In this work, we systematically investigated the influences of LER (line-edge-roughness), WFV (work- function variation) and STV (silicon layer thickness variation) on 20-nm-gate variable-body-factor SOTB MOSFETs.

9:50 C-6-3
Universal Relationship between Settling Time of Floating-Body SOI MOSFETs and the Substrate Current in their Body-Tied Counterparts
A. Toda[1], K. Ohyama[1], N. Higashiguchi[1], D. Hori[1], M. Miyake[1], S. Amakawa[1], J. Ida[2] and M. Miura-Mattausch[1], [1]Hiroshima Univ. and [2]Kanazawa Inst. of Tech. (Japan)
A device-size-independent universal relationship between hysteretic response of floating-body SOI MOSFETs and the dc substrate current in their body-tied counterparts is demonstrated. It could play an important role in compact modeling of history effects.

10:10 C-6-4
Ion-Ioff performance analysis of FDSOI MOSFETs with low processing temperature
C. Xu[1], P. Batude[1], C. Rauer[1], C. Le Royer[1], L. Hutin[1], A. Pouydebasque[1], C. Tabone[1], B. Previtali[1], O. Faynot[1], M. Mouis[2] and M. Vinet[1], [1]CEA-LETI/MINATEC and [2]IMEP (France)
This work demonstrates that Fully-Depleted Silicon On Insulator (FDSOI) transistors processed at low temperature (overall process temperature kept below 600°C) exhibit no strong degradation of the off current as compared to their conventional Rapid Thermal Processing (RTP) counterparts.

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D-6: Photonic and Electronic Integration (Area 7)

(9:00-10:30)
Chairs: N. Iizuka (Toshiba Corp.)
H. Isshiki (The Univ. of Electro-Communications)

9:00 D-6-1 (Invited)
Membrane-Type Photonic Devices for Optical Circuits on SOI
S. Arai and N. Nishiyama, Tokyo Tech (Japan)
Recent research activities on membrane-type photonic devices, such as ultra-low power-consumption semiconductor lasers as well as passive optical devices based on high index-contrast waveguides, aiming at on-chip optical interconnection for next-generation LSIs will be presented.

9:30 D-6-2
Towards Optical Networks-on-Chip Using CMOS Compatible III-V/SOI Technology
L. Grenouillet[1], P. Philippe[1], J. Harduin[1], N. Olivier[1], P. Grosse[1], L. Liu[2,3], T. Spuesens[2], P. Régreny[1], F. Mandorlo[4], P. Rojo-Romeo[4], R. Orobtchouk[4], D. Van Thourhout[2] and J. M. Fedeli[1], [1]CEA-LETI/MINATEC, [2]Ghent Univ., [3]Technical Univ of Denmark and [4]Institut des Nanotechnologies de Lyon INL (FRANCE)
Integrated components for optical networks-on-chip, including III-V microdisk lasers, photodetectors, and wavelength selective circuits, are all demonstrated using a complementary metal-oxide-semiconductor (CMOS) compatible III-V/silicon-on-insulator integration technology at 200mm wafer scale.

9:45 D-6-3
Design and Fabrication of Flip-Chip Micro-LED Arrays with PWM Driver for Heterogeneous Optoelectronic Integrated Circuit Device
S. B. Shin[1], J. Chiba[1], H. Okada[1], S. Iwayama[2] and A. Wakahara[1], [1]Univ. of Toyohashi of Tech. and [2]Stanley Electric Co. Ltd. (Japan)
We designed and fabricated of micro-LED arrays with pulse width modulation(PWM) driver by flip-chip bonding method for research of heterogeneous optoelectronic integrated circuit.

10:00 D-6-4
Monolithic One-bit Counter Circuit with Light Emitting Diode Indicators Fabricated in Si/III-V-N/Si Heterostructure
S. Tanaka, K. Noguchi, K. Yamane, Y. Deguchi, Y. Furukawa, H. Okada, A. Wakahara and H. Yonezu, Toyohashi Univ. of Tech. (Japan)
A monolithic one-bit counter circuit with LED indicators was fabricated, and was successfully operated. The fundamental properties of the circuits as well as the device characteristics were investigated.

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E-6: FeRAM (Area 4)

(9:00-10:35)
Chairs: T. Eshita (Fujitsu Semiconductor Ltd.)
K. Ishihara (Sharp Corp.)

9:00 E-6-1 (Invited)
Current Status and Future Challenge of Fe-NAND/SRAM Cell Technology
K. Takeuchi, Univ. of Tokyo (Japan)
This paper overviews Ferroelectric NAND flash memory and Ferroelectric 6T-SRAM. Fe-NAND enhances SSD performance to 9.5GByte/sec. A 100Million write/erase endurance is realized. A 0.5V ferroelectric 6T-SRAM is proposed which decreases the active power by 32%.

9:30 E-6-2 (Invited)
Current Development Status and Future Challenges of FeRAM
Y. Fujimori, H. Kimura, Y. Ichida, J. Iida, K. Ashikaga, H. Ito, T. Ozawa, T. Kanaya, N. Kinouchi, T. Suzuki, T. Date, D. Notsu, T. Fuchikami, Z. Zhiyong M. Kojima, M. Moriwake and H. Takasu, ROHM Co., Ltd. (Japan)
FeRAM technology on 130nm logic platform is successfully developed. We introduce non-volatile logic for new application. The non-volatile register has wide signal margin and high endurance cycles.

10:00 E-6-3
Synthesis of pure phase BiFeO3 films grown on Iridium electrode by MOCVD for ferroelectric memories
Y. Kumura[1,2], S. Y. Yang[2], P. Yu[2], J. X. Zhang[2], J. Seidel[2], A. I. Khan[2] and R. Ramesh[2], [1]Toshiba Corp. and [2]Univ. of California Berkeley (Japan)
We have successfully demonstrated the feasible synthesis of the pure phase BFO films without voids grown on the submicron-sized Ir electrode by MOCVD using double-layered deposition method for the first time.

10:20 E-6-4 (Late News)
Ferroelectric-Gate Thin-Film Transistor Fabricated by Total Solution Deposition Process
T. Miyasako[1], B. N. Q. Trinh[1], T. Kaneda[1], M. Onoue[1], P. T. Tue[1], E. Tokumitsu[1,2] and T. Shimoda[1,3], [1]JST, [2]Tokyo Tech and [3]JAIST (Japan)
We have fabricated ferroelectric-gate thin film transistors (FGTs) by totally using chemical solution deposition (CSD) process. The fabricated FGT exhibited a typical n-channel memory transistor operation. This is the first demonstration of inorganic thin film transistors (TFTs) fabricated by totally using CSD process for all layers.

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F-6: Spintronics (Ⅰ) - Spin-related Phenomena and Applications (Area 12)-

(9:30-10:45)
Chairs: K. Ito (Hitachi, Ltd.)
H. Saito (AIST)

9:30 F-6-1
Semiconductor / Ferromagnetic Metal Hybrid Optical Isolators using Nonreciprocal Polarization Rotation
H. Shimizu, S. Goto and T. Mori, Tokyo Univ. of Agri. and Tech. (Japan)
We report Fe - InGaAlAs / InP semiconductor - ferromagnetic metal hybrid optical isolators using nonreciprocal polarization rotation. We demonstrated optical isolation of as large as 18.3 dB in 0.85 mm-long waveguide devices.

9:45 F-6-2
Fabrication of MgO-based Magnetic Tunnel Junctions for Magnetic Field Sensor
K. Fujiwara[1], M. Oogane[1], F. Kou[2], H. Naganuma[1] and Y. Ando[1], [1]Tohoku Univ. and [2]RICOH COMPANY,LTD. (Japan)
Magnetic tunnel junctions sensor with an MgO barrier layer were fabricated. The effect of the shape and thickness of the free layer on the magnetic field sensor characteristics was systematically investigated. We achieved a large TMR/2H_k value of 4.8 %/Oe.

10:00 F-6-3
First-Principles Calculations of Quantum Transport Properties of Fe/Fe_2VAl/Fe Trilayers
S. Yabuuchi, I. Kitagawa and T. Hamada, Hitachi, Ltd. (Japan)
We investigated the electronic structure and the quantum transport properties of Fe/Fe_2VAl/Fe trilayer using first-principles calculations. The semimetallic Fe2VAl made it possible to achieve a low resistance area, which is difficult to achieve using a conventional insulator or metal.

10:15 F-6-4
Highly spin-polarized tunneling in Heusler-alloy-based magnetic tunnel junctions with a Co_2MnSi upper electrode and a MgO barrier
H-x Liu, T. Taira, Y. Honda, K. Matsuda, T. Uemura and M. Yamamoto, Hokkaido Univ. (Japan)
High tunnel magnetoresistance ratios of 1049% at 4.2 K and 335% at room temperature were demonstrated for Heusler-alloy-based magnetic tunnel junctions with a Co_2MnSi upper electrode and a MgO barrier. The key factors influencing the spin-dependent tunneling characteristics are discussed.

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G-6: Image Sensors and Interface Circuits (Area 5 & 11)

(9:00-10:45)
Chairs: S. Sugawa (Tohoku Univ.)
J. Akita (Kanazawa Univ.)

9:00 G-6-1 (Invited)
CMOS High–Speed Image Sensors –Pixel Devices, Circuits and Architectures–
S. Kawahito, Shizuoka Univ. (Japan)
CMOS high-speed image sensors are reviewed from the viewpoints of pixel devices and circuit techniques. Possible column-parallel ADC architectures for power-efficient high-speed high-quality imaging and global shutter pixels for low noise are discussed.

9:30 G-6-2
A Column Parallel Cyclic ADC with an Embedded Programmable Gain Amplifier for CMOS Image Sensors
T. Iida, M. A. Mustafa, L. Zhuo, K. Yasutomi, S. Itoh and S. Kawahito, Shizuoka Univ. (Japan)
This paper proposes a column parallel cyclic ADC with an embedded programmable gain amplifier. The measurement results of a prototype chip show the effectiveness of the embedded PGA for the reduction of ADC non-linearity and random noise.

9:50 G-6-3
A CMOS Image Sensor with an Automatic Pixel-Sensitivity Adjustment Function
G. Ramos[1], Y. Hirata[2] and Y. Arima[1], [1]Kyushu Inst. of Tech. and [2]Fukuoka Indus., Sci. and Tech. Foundation (Japan)
We developed an image sensor LSI that automatically adjusts the exposition time for each pixel according to the brightness of its surrounding pixels. The developed sensor LSI uses a 0.35µm CMOS 1-poly 3-metal process and has a die size of 3.75mm × 3.72mm. The power consumption is 267mW.

10:10 G-6-4
A Subnanowatt Vibration-sensing Circuit for Dust-size Battery-less Sensor Nodes
T. Shimamura, H. Morimura, M. Ugajin and S. Mutoh, NTT Microsystem Integration Laboratories (Japan)
The sensing circuit should be ultra-small power on the dust-size sensor node. We propose a vibration-sensing circuit based on mechanical charge transfer. The test chip detects the vibration of sub-hectohertz with subnanowatt power.

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H-6: Cu Reliability (Area 2)

(9:10-10:50)
Chairs: S. Ogawa (AIST)
K. Ito (Kyoto Univ.)

9:10 H-6-1 (Invited)
Cu Alloys and Noble Metal Liner Materials to Extend Damascene Cu Schemes
T. Nogami, IBM (USA)
CVD-Co films characterized (barrier properties and O/C incorporation). PVD-TaN/CVD-Co/PVD-Cu applied to Cu/ULK BEOL to produce reduced post-CMP defectivity and improved EM. However, EM advantage lost when divots due to corrosion formed at trench entrance.

9:40 H-6-2
Migration of Copper through Tungsten-Filled Via on Single Damascene Copper Interconnect
B. M. Kim, J. J. Kim, B. M. Seo, J. S. Oh, J. Y. Cho, J. Lee, K. Hong, B. H. Choi and S. Park, Hynix Semiconductor Inc. (Korea)
A phenomenon of copper migration through tungsten-filled vias, which land on single damascene copper underlayers, was examined. Successful mitigation of this problem was demonstrated through the enhancement of barrier metal or the change of soaking gas from silane to diborane in CVD W deposition process.

10:00 H-6-3 (Invited)
The Effects of Pre-existing Voids on Electromigration Lifetime Scaling
C.V. Thompson, MIT (USA)
Pre-existing voids are common in Cu interconnects. They are also mobile and their dynamics affect reliability scaling in a critical way. Experimental observations and modeling will be reviewed.

10:30 H-6-4
Structure Analyses of Ti-Based Self-Formed Barrier Layers
K. Kohama[1], K. Ito[1], Y. Sonobayashi[1], K. Ohmori[2], K. Mori[2], K. Maekawa[2], Y. Shirai[1] and M. Murakami[3], [1]Kyoto Univ., [2]Renesas Electronics Corp. and [3]The Ritsumeikan Trust (Japan)
Ti-based self-formed barrier layer has enough barrier properties against Cu diffusion into dielectrics. However, the structure and amorphous phases in the barrier layer were not directly identified. We employed an XPS technique with simultaneous Ar etching, to investigate the origin of such high performance of the barrier layer.

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I-6: GaN Power Transistors (Area 6)

(9:00-10:45)
Chairs: E. Y. Chang (National Chiao Tung Univ.)
T. Tanaka (Panasonic Corp.)

9:00 I-6-1 (Invited)
GaN on Si Based Power Devices:A New Era in Power Electronics
M. A. Briere, ACOO Enterprises LLC under contract for International Rectifier (USA)
The commercial introduction of GaN based power devices has opened new possibilities in power electronics. The current status and future prospects for GaN on Si power devices is reviewed, including long term reliability and device stability. Revolutionary advances made possible by these devices in several power electronic applications are discussed.

9:30 I-6-2
Thermally Stable Isolation of AlGaN/GaN Transistors by Using Fe Ion Implantation
H. Umeda, T. Takizawa, Y. Anda, T. Ueda and T. Tanaka, Panasonic Corp. (Japan)
Thermally stable isolation for AlGaN/GaN transistors by Fe ion-implantation is demonstrated. The Fe ions form deep levels after high temperature annealing. This technique enables high breakdown voltages and promising for monolithic integration of GaN devices.

10:00 I-6-4
Reduction of current collapse in AlGaN/GaN HEMTs using thick GaN cap layer
H. Chonan[1], Y. Sakamura[2], G. Piao[2], T. Ide[2], M. Shimizu[2], Y. Yano[3] and H. Nakanishi[1], [1]Tokyo Univ. of Sci., [2]AIST and [3]Taiyo Nippon Sanso Corp. (Japan)
Current collapse suppression using thick GaN cap layer in AlGaN/GaN HEMTs was proposed. Numerical simulations and experimental results show that thick GaN cap layer have effect in reducing carrier trapping in the device semiconductor surface.

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J-6: Nanowire Transistors (Area 13)

(9:00-10:45)
Chairs: S. Uno (Nagoya Univ.)
K. Nishiguchi (NTT Basic Res. Labs.)

9:00 J-6-1 (Invited)
Circuit Implementation of InAs Nanowire FET
W. Prost, K. Blekker, O. Benner and F. J. Tegude, University of Duisburg-Essen (Germany)
We report on the fabrication of InAs nanowire metal-insulator field-effect transistor and their implementation in basic circuits. The position controlled deposition of the InAs nanowires within the pre-patterned circuits on the host substrate is done by the field-assisted fluid self-assembly method.

9:30 J-6-2
Transport Physics of Quasi-Ballistic Nanowire MOSFETs
K. Natori, Tokyo Tech (Japan)
Transport physics of nanoscale MOSFETs is discussed based on characteristics of nanowire MOSFETs. The compact model discloses various new effects.

9:45 J-6-3
Body-biased steep-subthreshold-swing MOS (BS-MOS) with small hysteresis, off current, and drain voltage
K. Nishiguchi and A. Fujiwara, NTT Corp. (Japan)
We demonstrate 30-nm-gate-length nanowire MOSFETs. A parasitic bipolar transistor formed in an SOI channel reduces subthreshold swing below 60 mV/dec at room temperature. Additionally, triple-gate operation allows current characteristics with small hysteresis, high on/off ratio, and low drain voltage.

10:00 J-6-4
Impacts of Diameter-Dependent Annealing in Silicon Nanowire MOSFETs
R. Wang, T. Yu, W. Ding and R. Hung, Peking Univ. (China)
The diameter-dependent annealing effect in silicon nanowire MOSFETs is investigated. The implanted dopants diffuse faster in thin nanowires than those in thick nanowires during annealing process, which results in underestimating the nanowire S/D extension length.

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K-6: Quantum Dots (Area 8)

(9:00-10:45)
Chairs: A. Yamada (Tokyo Tech)
T. Yamaguchi (Ritsumeikan Univ.)

9:00 K-6-1 (Invited)
Quantum Dot Superlattice for High Efficiency Intermediate Band Solar Cell
Y. Okada, Univ. of Tokyo (Japan)
Effciency enhancements exceeding Shockley-Queisser limit of single junction solar cells are possible in an intermediate band solar cell, which incorporates a 3-dimensional quantum dot superlattice in the active region of a p-i-n junction structure. Recent experimental progress on multi-stacked quantum dot solar cells will be reviewed.

9:30 K-6-2
Energy transfer in multi-stacked InAs quantum dots
K. Akahane[1], N. Yamamoto[1], M. Naruse[1,2], T. Kawazoe[2], T. Yatsui[2] and M. Ohtsu[2], [1]Natl. Inst. of Info. & Com. Tech. and [2]Univ. of Tokyo (Japan)
We fabricated a modulated stacked QD structure to investigate energy transfer among QDs. Energy transfer from small QDs to large QDs was clearly observed. Long-range energy transfer can be considered from the measurement of N dependence of PL intensity.

9:45 K-6-3
Enhanced Photoluminescence Properties from Self-Assembled InAs Surface Quantum Dots by Antimony Incorporation
C. H. Chiang, Y. H. Wu, M. C. Hsieh, C. H. Yang, J. F. Wang, Y. C. Chang, L. Chang and J. F. Chen, National Chiao Tung Univ. (Taiwan)
We present a study of surfactant effect from self-assembled InAs surface quantum dots grown on GaAs substrate by incorporating antimony (Sb) into the QD layers with various Sb beam equivalent pressure.

10:00 K-6-4
Structure changes caused by quenching of InAs/GaAs(001) quantum dots
M. Takahasi, JAEA (Japan)
Structures of InAs/GaAs(001) free-standing quantum dots before and after quenching were studied by in situ synchrotron X-ray diffraction. It has been revealed that quenching results in significant structure changes. They take place quickly when the substrate goes through a temperature range in which dislocatd islands are preferably formed.

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Friday, September 24

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A-6: Organic Transistors and Device Physics Ⅰ (Area 10)

10:15 A-6-5
Effects of Gold Nanoparticles on Pentacene Organic Field-effect Transistors
K. Lee[1], W. Ou-Yang[1], M. Weis[2], D. Taguchi[1], T. Manaka[1] and M. Iwamoto[1], [1]Tokyo Tech and [2]Slovak Academy of Sciences (Japan)
By incorporating gold nanoparticles into PVA with different concentrations as nanocomposite gate insulator in pentacene OFET, the carrier behaviour of the devices was studied by considering the carrier injection and transport processes in terms of contact resistance and effective mobility.

10:30 A-6-6 (Late News)
Fabrication of Au electrodes with photopolymerization of triazine dithiol thin films
Y. Sato, R. Ye, K. Ohta and M. Baba, Iwate Univ. (Japan)
we fabricated electrodes of Au thin films on micropattern poly(DT) thin films photopolymerizated through a photomask. This process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.

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B-6: Junction Technology (Area 1)

10:30 B-6-5 (Late News)
Ge Self-Diffusion in Compressively strained Ge Grown on Relaxed $Si_{0.2}Ge_{0.8}$
Y. Kawamura[1], M. Uematsu[1], K Itoh[1], Y. Hoshi[2], K. Sawano[2], Y. Shiraki[2], E. Haller[3] and M. Myronov[4], [1]Keio Univ., [2]Tokyo City Univ., [3]Univ. of California Berkeley and [4]The Univ. of Warwick (Japan)
We present the first measurements of Ge self-diffusion under compressive biaxial strain using $Si_{0.2}Ge_{0.8}$/Ge isotope superlattice/$Si_{0.2}Ge_{0.8}$ heterostructures. Furthermore, we found that Ge self-diffusivities in compressively strained Ge are larger compared to those in relaxed Ge.

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C-6: Advanced CMOS Technology (Area 3)

10:30 C-6-5 (Late News)
Cost Efficient Novel High Performance Analog Devices Integrated with Advanced HKMG Scheme for 28nm CMOS Technology and Beyond
J.-P. Han[1], T. Shimizu[2], L. H. Pan[3], M. Voelker[1], C. Bernicot[4], F. Arnaud[4], A. C. Mocuta[3], K. Stahrenberg[1], A. Azuma[5], G. Yang[5], M. Eller[1], D. Jaeger[1], H. Zhuang[1], K. Miyashita[1], K. Stein[1], D. R. Nair[2], J. H. Park[2], M. Hamaguchi[2], S. Kohler[2], D. Chanemougame[4], W. Li[1], K. Kim[1], N. Kim[6], C. Wiedholz[1], S. Miyake[2], G. Tsutsui[2], H. van Meer[6], J. Liang[6], M. Ostermayr[1], J. Lian[1], M. Celik[1], R. Donaton[3], K. Barla[4], M. H. Na[3], Y. Goto[2], M. Sherony[3], F. Johnson[6], R.Wachnik[3], J. Sudijono[6], E. Kaste[3], R. Sampson[6], J.-H. Ku[1], A. Steegen[3] and W. Neumueller[1], [1]Infineon Technologise, [2]Renesas, [3]IBM Microelectronics, [4]STMicroelectronics, [5]Toshiba America, [6]GLOBALFOUNDRIES and [7]Samsung Electronics (USA)
A comprehensive study of high performance analog (HPA) devices integrated with high-k metal gate has shown that analog properties such as output voltage gain, Gm, Gds, Gm/Id, mismatch behavior, flicker noise, linearity, DC performance (e.g. Ion-Ioff, Ioff-Vtsat, DIBL, Cjswg) as well as reliability of HPA are superior to conventional analog devices

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D-6: Photonic and Electronic Integration (Area 7)

10:15 D-6-5
Monolithic Integration of Ga(NAsP) laser on Si (001) Substrate
S. Liebich[1], M. Zimprich[1], P. Ludewig[1], A. Beyer[1], B. Kunert[2], N. Hossain[3], S. Jin[3], S. J. Sweeney[3], K. Volz[1] and W. Stolz[1], [1]Philipps-Univ. Marburg, [2]NAsP III/V GmbH and [3]Univ. of Surrey (Germany)
Laser structures containing the dilute nitride material Ga(NAsP) can be grown lattice matched on silicon substrates with high crystalline quality and low defect density. Lasing operation from broad area lasers up to 120K is verified.

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E-6: FeRAM (Area 4)

4F 242

F-6: Spintronics (Ⅰ) - Spin-related Phenomena and Applications (Area 12)-

10:30 F-6-5
Temperature Dependence of Magnetic Damping in Heusler Alloy Thin Films
M. Oogane, S. Mizukami, Y. Kota, T. Kubota, H. Naganuma, A. Sakuma and Y. Ando, Tohoku Univ. (Japan)
The magnetic damping constants and their temperature dependence for the epitaxitially grown $Co_2MnAl_xSi_{1-x}$ and $Co_2Fe_xMn_{1-x}Si$ Heusler alloy films were systematically investigated.

Coffee Break (2F Forum)

1F 211

A-7: Organic Transistors and Device Physics Ⅱ (Area 10)

(11:15-12:15)
Chairs: H. Kajii (Osaka Univ.)
K. Fujita (Kyushu Univ.)

11:15 A-7-1
A Proposal of High Performance and Highly Fabricable Complementary Organic Thin Film Transistor Structure
A. Sugawara, Y. Wada, Y. Ishikawa and T. Toyabe, Toyo Univ. (Japan)
A Complementary Organic Thin Film Transistor (COTFT) structure is proposed, which would make it possible to realize high performance and highly fabricable organic integrated circuits, by using our original OTFT devices simulator, TOTAS.

11:30 A-7-2
Charge modulated reflectance measurement for probing carrier distribution in the pentacene field effect transistor
T. Manaka, S. Kawashima, Y. Tanaka and M. Iwamoto, Tokyo Tech (Japan)
In this presentation, microscopic charge modulated reflectance spectroscopy was conducted to study the injected carrier distribution (n) in pentacene FET. Signal distribution along channel is clearly good agreement with the carrier distribution calculated on the basis of a simple carrier transport model. In combination with the EFISHG mentioned above, each parameters in J=enuE is discriminately evaluated.

1F 212

B-7: Dopant Characterization (Area 1)

(11:15-12:25)
Chairs: Y. Hayami (Fujitsu semiconductor Ltd.)
B. Mizuno (UJT Lab. Inc.)

11:15 B-7-1 (Invited)
Dopant/carrier profiling in nanostructures.
W. Vandervorst[1,2], P. Eyben[1], A. Schulze[1,2], J. Mody[1,2], S. Koelling[1,2], A. Kambham[1,2] and M. Gilbert[1], [1]IMEC and [2]Instituut voor Kern- en Stralingsfysica (Belgium)
Compositional and electrical analysis of nanostructures involves extreme requirements ranging from “simple” 1D-depth resolution problems to metrology with high 2D-spatial resolution to the need to probe in an extremely small confined volume and 3D-devices. In this presentation we present an overview of the recent evolution in 1D, 2D, and 3D analysis.

11:45 B-7-2
Hole generation in B-implanted Ge without annealing: Formation of B_{12} cluster acting as a double acceptor
M. Koike and Y. Kamimuta, MIRAI-Toshiba (Japan)
We present hole generation (max: 8x10^20 cm^-3) in B-implanted Ge without annealing. The activation ratio in the wide range of impurity concentrations ($10^{16\text{-}22}$ cm^{-3}) is almost the same value of 1/6. These results can be explained by assuming B12 cluster formation as a double acceptor in the as-implanted Ge.

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C-7: FinFET Devices (Area 3)

(11:15-12:35)
Chairs: S. Hayashi (Panasonic Corp.)
K. Okano (Toshiba Corp.)

11:15 C-7-1
Experimental Study of PVD-TiN Gate with Poly-Si Capping and Its Application to 20 nm FinFET Fabrication
T. Kamei[1], Y. X. Liu[2], K. Endo[2], S. O'uchi[2], J. Tsukada[2], H. Yamauchi[2], Y. Ishikawa[2], T. Hayashida[1], T. Matsukawa[2], K. Sakamoto[2], A. Ogura[1] and M. Masahara[2], [1]Meiji Univ. and [2]AIST (Japan)
We have investigated threshold voltage (Vth) variability and mobility of n+-poly-Si and PVD-TiN gate FinFETs. Thin PDV-TiN with n+-poly-Si capping is very effective to set a symmetrical Vth for FinFETs without mobility degradations.

11:35 C-7-2
High-k Metal Gate FinFET SRAM Cell Optimization Considering Variability due to NBTI/PBTI and Surface Orientation
V. P. H. Hu, M. L. Fan, C. Y. Hsieh, P. Su and C. T. Chuang, National Chiao Tung Univ. (Taiwan)
This paper analyzes the impact of intrinsic process variation and NBTI/PBTI induced time-dependent variations on the stability/variability of 6T high-k metal gate FinFET SRAM cells with various surface orientations. Variability comparisons for FinFET SRAM cells with different gate stacks (SiO2 and SiO2/HfO2) are also examined.

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D-7: Nano Photonics (Area 7)

(11:15-12:00)
Chairs: M. Tokushima (AIST)
S. Saito (Hitachi, Ltd.)

11:15 D-7-1
InGaAs Nano-Photodiode enhanced by Polarization-Insensitive Surface-Plasmon Antenna
D. Okamoto, J. Fujikata and K. Ohashi, NEC Corp. (Japan)
We developed an InGaAs nano-photodiode incorporated with a polarization-insensitive ring-type surface-plasmon antenna consisting of gold-based concentric-ring gratings. The antenna enables high quantum efficiency of 80% for any polarization of incident light and wider wavelength bandwidth.

11:30 D-7-2
Metallic Nano-Slit Array Lens for Spatial Resolution Improvement of In-vivo CMOS image sensor
K. Sasagawa[1,2], T. Noda, T. Tokuda, M. S. Islam[3] and J. Ohta[1,2], [1]NAIST, [2]JST-CREST and [3]Univ. of California at Davis (Japan)
We proposed a metallic nano-slit array lens for implantable in-vivo CMOS image sensor. And the electromagnetic fields were simulated by FDTD method. The results show that the incident angle is limited and the spatial resolution is improved by the structure.

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E-7: MRAM (Area 4)

(11:15-12:05)
Chairs: S. Miura (NEC Corp.)
T. Eshita (Fujitsu Semiconductor Ltd.)

11:15 E-7-1 (Invited)
Current Status and Future Challenge of Embedded High-speed MRAM
S. Fukami, T. Suzuki, K. Nagahara, N. Ohshima, S. Saitoh, R. Nebashi, N. Sakimura, H. Honjo, K. Mori, E. Kariyada, Y. Kato, K. Suemitsu, H. Tanigawa, K. Kinoshita, S. Miura, N. Ishiwata and T. Sugibayashi, NEC Corp. (Japan)
The DW-motion MRAM with 2T1MTJ cell structure has been developed. We confirmed its potential to replace conventional embedded memories. Our technology will enable zero standby power consumption SoCs.

11:45 E-7-2
Phenomenological model for stress and relaxation processes of resistance drift in magnetic tunnel junctions
Y. Kamakura, S. Nakano and K. Taniguchi, Osaka Univ. (Japan)
A phenomenological model for stress and relaxation processes of resistance drift in AlOx based MTJs is proposed. By using the rheological approach, the model can well reproduce the characteristics observed in various pulsed stress experiments.

4F 242

F-7: Spintronics (Ⅱ) - New Applications - (Area 12)

(11:15-12:30)
Chairs: Y. Ohno (Tohoku Univ.)
K. Ito (Hitachi, Ltd.)

11:15 F-7-1 (Invited)
Three-Terminal Spin-Momentum-Transfer Magnetic Memory Element
M. Gaidis, J. Sun, E. O'Sullivan, G. Hu, J. DeBrosse, J. Nowak, D. Abraham and P. Trouilloud, IBM (USA)
SMT MRAM has potential as a nonvolatile memory with speed, density, endurance, and scaling. One can improve performance by separating the reading and writing functions of the device, adding a third terminal to the standard two-terminal device. We present the design and fabrication of the device, and high speed test results showing 1ns switching.

11:45 F-7-2 (Invited)
Spin dice: Random Number Generator using Current-induced Magnetization Switching in MgO-MTJs
A. Fukushima, T. Seki, K. Yakushiji, H. Kubota, S. Yuasa and K. Ando, AIST (Japan)
We propose a new type of physical random number generator based on the current induced magnetization switchings in MgO-MTJs, named spin dice. Random numbers are generated by the probabilistic characteristic of the switchings. We fabricate spin dice in a circuit board style, and generate the random numbers at 500 kbit/sec.

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4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-6: Image Sensors and Interface Circuits (Area 5 & 11)	**H-6: Cu Reliability (Area 2)**	**I-6: GaN Power Transistors (Area 6)**	**J-6: Nanowire Transistors (Area 13)**	**K-6: Quantum Dots (Area 8).)**	
10:30 G-6-5 (Late News) **A SPICE-based Multi-physics Seamless Simulation Platform for CMOS-MEMS** *T. Konishi[1], S. Maruyama[2], T. Matsushima[1], M. Mita[3], K. Machida[1,4], N. Ishihara[4], K. Masu[4], H. Fujita[2] and H. Toshiyoshi[2], [1]NTT Advanced Technology Corp., [2]Univ. of Tokyo, [3]JAXA and [4]Tokyo Tech (Japan)* We report a SPICE version of such multi-physics solver that is capable of microelectromechanical transient analysis, AC harmonic analysis, and electro-mechanical mixed-signal simulation that can be performed seamlessly with the LSI simulation.		**10:15 I-6-5** **Reduced contact resistance and Improved surface morphology for Ohmic Contacts on AlGaN/GaN based Semiconductors employing KrF Laser Irradiation** *G. H. Wang[1], T. Sudhiranjan[1], X. Wang[2], H. Y. Zheng[2], T. K. Chan[3], T. Osipowicz[3] and Y. L. Foo[1], [1]Inst. of Materials Res. And Eng., [2]Singapore Inst. Of Manufacturing Tech. and [3]National Univ. of Singapore (Singapore)* We employ excimer laser annealing for ohmic contact formation to n or p type GaN. Laser annealing achieved reduced sheet resistance in the contact formed, essential for high performance GaN light emitting diodes (LEDs) and heterostructure field-effect transistors applications. Forward current in LEDs increased due to the reduced contact resistance.	**10:15 J-6-5** **Single-electron transport through a Germanium-Nanowire Quantum Dot** *S. K. Shin[1,2], S. Huang[1], N. Fukata[3] and K. Ishibashi[1,2], [1]RIKEN, [2]Tokyo Inst. of Tech. and [3]National Inst. for Materials Sci. (Japan)* Single-electron transistors using an n-type GeNW were fabricated. Pronounced Coulomb peaks with the equidistant spacing in Vg were observed. While the Coulomb peak heights were varied very much, the dimensions of Coulomb diamonds were identical.	**10:15 K-6-5** **High-temperature phosphorous passivation of Si surface for improved heteroepitaxial growth of InAs as an initial step of III-As MOVPE on Si** *M. Deura, Y. Kondo, M. Takenaka, S. Takagi, Y. Shimogaki, Y. Nakano and M. Sugiyama, Univ. of Tokyo (Japan)* We investigated the annealing effect on InAs growth, annealed in group-V gas ambient at much higher temperature than that during growth and the protection effect of group-V atoms during annealing in terms of surface contamination.	
		10:30 I-6-6 **Nonequilibrium Carrier Transport Observed in Pnp AlGaN/GaN HBTs** *K. Kumakura and T. Makimoto, NTT Corp. (Japan)* We found nonequilibrium carrier transports in the nitride-based HBTs. They were ascribed to the high energy carrier injection into the base, and also to the carrier drift motion induced by the electric field inside the base.	**10:30 J-6-6** **A Theoretical Study of Electron Wave Function Penetration Effects on Electron-Modulated-Acoustic-Phonon Interactions in Silicon Nanowire MOSFETs** *J. Hattori[1,3], S. Uno[1,3], N. Mori[2,3] and K. Nakazato[1], [1]Nagoya Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)* We have theoretically studied the interaction between electrons and modulated acoustic phonons in gate biased silicon nanowires with taking into account electron wave function penetration into the oxide layer.	**10:30 K-6-6** **Growth of InAs Quantum Dots with Various Charged States on a Wafer Utilizing Concentric Distribution** *N. Kumagai[1], S. Ohkouchi[1], M. Shirane[1,2], Y. Igarashi[1,2], M. Nomura[1], Y. Ota[1], S. Yorozu[1,2], S. Iwamoto[1] and Y. Arakawa[1], [1]Univ. of Tokyo and [2]NEC Corp. (Japan)* Using concentric distribution of QD density on a wafer, we obtain a series of QDs with charged excitonic states from positive to negative via neutral states at a time. As a result, we succeed in growth of InAs QDs with selectively charged states on a same wafer by only Si doping.	

Coffee Break (2F Forum)

G-7: Data Converter Circuits (Area 5) (11:15-12:30) Chairs: M. Horiguchi (Renesas Electronics. Corp.) T. Koide (Hiroshima Univ.)	**H-7: 3D Interconnect (Area 2)** (11:15-12:25) Chairs: J. Gambino (IBM) J. Kodate (NTT)	**I-7: Processing and Interface Technologies (Area 6)** (11:15-12:30) Chairs: K. S. Seo (Seoul National Univ.) K. Kumakura (NTT Corp.)	**J-7: Nanowire Growth and Applications (Area 13)** (11:15-12:30) Chairs: N. Aoki (Chiba Univ.) K. Tateno (NTT Corp.)	**K-7: Growth and Characterization of Nitrides (Area 8)** (11:15-12:30) Chairs: T. Iwai (Fujitsu Labs. Ltd.) M. Takahashi (JAEA)	
11:15 G-7-1 **Qpix v.1: A high speed 400-pixels readout LSI with 10-bit 10MSps pixel ADCs** *F. Li, V. M. Khoa, M. Miyahara and A. Matsuzawa, Tokyo Tech (Japan)* Qpix v.1 has been developed to realize large area applications and to increase the basic performance. It possesses 400 pixels and compact readout structure to guarantee that all stored data in the pixels can be read out in 2.6 µs in parallel mode and 54 µs in serial mode.	**11:15 H-7-1 (Invited)** **3D Integration Technology and 3D System-on- a Chip** *M. Koyanagi, Tohoku Univ. (Japan)* A 3D super-chip integration technology using the reconfigured wafer-to-wafer bonding and multichip-to-wafer bonding is presented. In addition, new 3D-SoCs such as a 3D microprocessor, 3D-stacked image processor and 3D dependable SoC are discussed.	**11:15 I-7-1** **Deep level characterization of MOVPE-grown AlGaN with high Al compositions** *S. Okuzaki[1], K. Sugawara[1], H. Taketomi[2], H. Miyake[2], K. Hiramatsu[2] and T. Hashizume[1], [1]Hokkaido Univ. and [2]Mie Univ. (Japan)* We investigate Schottky interface properties and deep levels of $Al_xGa_{1-x}N$ with a wide range of Al composition ($0.25<x<0.60$) by using X-ray photoelectron spectroscopy (XPS), I-V, C-V, and deep level transient spectroscopy (DLTS).	**11:15 J-7-1** **Al-doped Zinc Oxide Field Emitter Array Controlled by High-Voltage Poly-Si Thin Film Transistor** *P. Y. Yang[1], J. L. Wang[2], W. C. Tsai[3], S. J. Wang[3], J. C. Lin[4], I. C. Lee[1], C. T. Chang[1] and H. C. Cheng[1], [1]National Chiao Tung Univ., [2]Ming Chi Univ. of Technology, [3]National Cheng Kung Univ. and [4]St. John's Univ. (Taiwan)* The hydrothermally grown Al-doped ZnO nanowires were controlled by high-voltage poly-Si thin film transistor to improve the anode current stability of field emitter.	**11:15 K-7-1 (Invited)** **Droplet elimination process by radical beam irradiation for the growth of InN-based III-nitrides and its application to device structure** *T. Yamaguchi and Y, Nanishi, [1]Ritsumeikan Univ. and [2]Seoul National Univ. (Japan)* A new method, named droplet elimination by radical beam irradiation (DERI), is proposed for the reproducible growth of high-quality InN. This method is also applied to the growth of Mg-doped InN and undoped InGaN toward the application to device structure.	
11:35 G-7-2 **A 0.5V 1.4mW 750MHz 10b CMOS Current Steering DAC** *N. Shimasaki, R. Ito, M. Miyahara and A. Matsuzawa, Tokyo Tech (Japan)* An ultra-low voltage and power of 0.5 V and 1.4 mW, yet high speed of 750 MHz CMOS 10 bit current DAC has been developed using digital feedback technique and forward body biasing.	**11:45 H-7-2** **Evaluation of Copper Diffusion in Thinned Wafer with Extrinsic Gettering for 3D-LSI by Capacitance-Time(C-t) measurement"** *J. C. Bea, K. W. Lee, M. Murugesan, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)* The effects of extrinsic gettering(EG) layers formed on p/p- wafers and p/p+ wafers by backside grinding and the following chemical mechanical polishing(CMP), dry polishing(DP) and ultra-poligrind(UPG) methods against metallic contamination induced has been investigated.	**11:30 I-7-2** **Direct Liquid Cooling Technology for Power Semiconductor Devices** *N. Otsuka, S. Nagai, M. Yanagihara, Y. Uemoto and D. Ueda, Panasonic Corp. (Japan)* We first demonstrate the reduction of junction temperatures in direct liquid cooling (DLC) of GaN power devices for high power and high voltage switching applications. In the DLC structure, junction temperature reductions of up to 55K or 100% higher power levels were demonstrated, and the thermal resistance was reduced as much as 32%.	**11:30 J-7-2** **Nanoarchitecture Light Emitting Diode Microarrays Using Position-Controlled GaN/ZnO Coaxial Nanotube Heterostructures** *C. H. Lee[1,2], J. Yoo[1,2], Y. J. Hong[1,2], J. Cho[1], Y. J. Kim[1,2], S. R. Jeon[3], J. H. Baek[3] and G. C. Yi[1], [1]Seoul National Univ., [2]POSTECH and [3]Korea Photonics Tech. Inst. (Korea)* We studied the fabrication and electroluminescent characteristics of GaN-based nanoarchitecture light emitting diode (LED) microarrays consisting of position-controlled GaN/ZnO coaxial nanotube heterostructures. The nanoarchitecture LEDs exhibited strong green and blue emission from the GaN/GaN/$In_{1-x}Ga_xN$ multi-quantum wells at room temperature.	**11:45 K-7-2** **Reduction of S-parameter by the Introduction of Nitrogen in GaNAs: Positron Annihilation and Its Comparative Study with Photoluminescence Spectroscopy** *H. Nakamoto[1], F. Ishikawa[1], M. Kondow[1], Y. Ohshima[1], A. Yabuchi[1], M. Mizuno[1], H. Araki[1] and Y. Shirai[2], [1]Osaka Univ. and [2]Kyoto Univ. (Japan)* The introduction of nitrogen into GaNAs reduces S-parameter compared to GaAs and that was further lowered by annealing. That suggests the possibility of correlation between carrier localization and the positron annihilation process.	

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A-7: Organic Transistors and Device Physics Ⅱ (Area 10)

11:45 A-7-3
Bias-temperature-instability and thermal anneal effects of organic thin-film transistors
P. H. Chen[1], P. Y. Lo[1,2], T. S. Hu[2] and P. W. Li[1], [1]National Central Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
Top-gate organic thin film transistors were fabricated and characterized in a temperature range of 300-370 K. In addition to thermally activated charge trapping and ion drift mechanisms, the trap numbers elimination at the P3HT/PVP and the dopant deactivation or bipolaron formation in P3HT are also possible origin for OTFTs instability.

12:00 A-7-4
Transport Mechanism at the First-layered Pentacene Grains and Grain Boundaries
Y. Hu[1,2], L. Wang[1], Q. Qi[1] and C. Jiang[1], [1]National Center for Nanoscience and Tech. and [2]Chinese Academy of Sci. (China)
We have performed both experimental and theoretical researches of transport mechanism in first layer grains and grain boundaries of the pentacene films and found that the grain boundary model is valid both in grain size dependent and temperature dependent mobility experiments.

1F 212

B-7: Dopant Characterization (Area 1)

12:05 B-7-3
Contribution of Carbon to Growth of Boron-Containing Cluster in Heavily B-doped Silicon
H. Itokawa[1,2], A. Ohta[2], M. Ikeda[2], I. Mizushima[1] and S. Miyazaki[2], [1]Toshiba Corp. and [2]Hiroshima Univ. (Japan)
It is well-known that substitutional C atoms can capture excess self-interstitial Si atoms and suppress the diffusion of ion-implanted intersitial-type dopants such as B in Si. In the case of B concentration as much as ~1 x 10^{21} cm^{-3}, the B activation ratio in Si is decreased with C incorporation.

1F 213

C-7: FinFET Devices (Area 3)

11:55 C-7-3
Advantage of Plasma Doping for Source/Drain Extension in Bulk-FinFET
T. Izumida, K. Okano, T. Kanemura, M. Kondo, S. Inaba, S. Itoh, N. Aoki and Y. Toyoshima, Toshiba Corp. (Japan)
We demonstrate the efficiency of plasma doping on the fabrication of a bulk-FinFET, showing detailed boron distributions in a narrow fin region analyzed by atom-probe tomography and SIMS, and device characteristics calculated by 3D simulations.

12:15 C-7-4
FinFETs Junctions Optimization by Conventional Ion Implantation for (Sub-)22nm Technology Nodes Circuit Applications
A. Veloso, A. De Keersgieter, S. Brus, N. Horiguchi, P. P. Absil and T. Hoffmann, IMEC (Belgium)
This work demonstrates a junctions formation methodology for aggressively scaled FinFET devices, using conventional ion implantation, and compatible with dense pitches applications, without penalty in RSD nor device performance, and yielding higher SRAM SNM values.

2F 221

D-7: Nano Photonics (Area 7)

11:45 D-7-3
Enhanced Sensitivity of SOI Photodiode by Au Nanoparticles
Y. Matsuo, A. Ono, H. Satoh and H. Inokawa, Shizuoka Univ. (Japan)
We demonstrated the enhancement of the quantum efficiency of SOI photodiode with Au nanparticles. The en-hancement mechanism is explained by the increment of the effective path in SOI due to the scattering and the multiple reflections.

4F 241

E-7: MRAM (Area 4)

4F 242

F-7: Spintronics (Ⅱ) - New Applications - (Area 12)

12:15 F-7-3
High-speed MRAM Random Number Generator using Error-Correcting Code
T. Tetsufumi, N. Shimomura, S. Ikegawa, M. Matsumoto, S. Fujita and H. Yoda, Toshiba Corp. (Japan)
A high speed random number generator (RNG) circuits based on magnetoresistive-random-access-memory (MRAM) using error-correcting coding (ECC) post-processing circuits is presented. It is shown that this post-processing block can be shared with conventional memory ECC block and powerfully improves the quality of randomness with minimum overhead.

12:30-13:30 Lunch

1F 211

A-8: Organic Transistors and Device Fabrication Ⅰ (Area 10)

(13:30-15:00)
Chairs: H. Usui (Tokyo Univ. of Agri. & Tech.)
M. Yoshida (AIST)

13:30 A-8-1 (Invited)
Materials and Processes for Air-Stable n-Channel Organic Transistors
J. H. Oh[1,2] and Z. Bao[1], [1]Stanford Univ. and [2]UNIST (USA)
Recently, there has been a remarkable progress in the molecular design, device performance and stability for n-channel OTFTs. Herein we report recent progress in materials design and processes for high-performance air-stable n-channel OTFTs, mainly focusing on the development of most-commonly used n-channel semiconductors, i.e., perylene diimide (PDI) and naphthalene diimide (NDI) derivatives.

1F 213

C-8: Gate-Insulator Reliability (Area 1) & (Area 3)

(13:30-15:10)
Chairs: B. Doris (IBM)
B. H. Lee (GIST)

13:30 C-8-1
Using Power Transform to Study DC and AC CHC Effects on nMOSFETs in 65 nm Technology
S. Y. Chen[1], C. H. Tu[1], M. X. Wu[1], H. S. Huang[1], Z. W. Jhou[2], S. Chou[2] and J. Ko[2], [1]National Taipei Univ. of Tech. and [2]United Microelectronics Corp. (Taiwan)
For the first time, this article is to use power transform to describe nMOSFET degradation due to DC and AC CHC stress. The power transform model is a function of voltage (V_d, V_g-V_t), current (I_d, I_g), and temperature (T). All the results show that the power transform model can well fit the experimental data of DC and AC CHC stress.

2F 221

D-8: Si Photonics (1) (Area 7)

(13:30-15:15)
Chairs: H. Isshiki (The Univ. of Electro-Communications)
N. Iizuka (Toshiba Corp.)

13:30 D-8-1 (Invited)
Nanophotonic On-Chip Interconnection Networks for Energy-Performance Optimized Computing
A. Biberman and K. Bergman, Columbia Univ. (USA)
Much recent progress in silicon nanophotonic technology has enabled the prospect of high-performance nanophotonic networks-on-chip (NoCs), which have become very attractive solutions to the growing bandwidth and power consumption challenges of future high-performance chip multiprocessors.

4F 241

E-8: PRAM/ReRAM (Area 4)

(13:30-15:15)
Chairs: Y. C. Chen (Macronix International Co., Ltd.)
M. Moniwa (Renesas Electronics Corp.)

13:30 E-8-1 (Invited)
A Survey of Cross Point Phase Change Memory Technologies
D. Kau, Intel Corp. (USA)
Among the recent advances in phase change memory and the integrated selector, stackable thin-film cross point memory delivers the densest array, therefore the most compact die size. Combining its attributes in cost, performance and reliability, cross point phase change technologies stimulate potential opportunities in computing memory hierarchy.

4F 242

F-8: Spintronics (Ⅲ) - Semiconductors - (Area 12)

(13:30-15:00)
Chairs: M. Yamamoto (Hokkaido Univ.)
S. Kuroda (Univ. of Tsukuba)

13:30 F-8-1 (Invited)
Magnetic anisotropy of GaMnAs and its application for multi-valued memory device
S. Lee[1], T. Yoo[1], S. Khym[1], H. Lee[1], S. Lee[1], S. Kim[1], J. Shin[1], X. Liu[2] and J. K. Furdyna[2], [1]Korea Univ. and [2]Univ. of Notre Dame (Korea)
We present interesting magnetic anisotropy properties and realization of four resistance states in single layer of GaMnAs film. We demonstrate such four resistance sates can be used for a quaternary memory device.

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G-7: Data Converter Circuits (Area 5)

11:55 G-7-3
Low-Complexity Time-Domain Winner-Take-All Circuit with High Time-Difference Resolution Limited only by With-In-Die Variation
M. Yasuda, T. Ansari, W. Imafuku, A. Kawabata, T. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
The time-domain Winner-Take-All (WTA) circuit detects the first arriving signal and determines the winner. In this paper, a time-domain WTA circuit with high time-difference resolution limited only by with-in-die variation is developed.

12:15 G-7-4 (Late News)
3.6-Times Higher Acceptable Raw Bit Error Rate, 97% Lower-Power, NV-RAM & NAND-Integrated Solid-State Drives (SSDs) with Adaptive Codeword ECC
M. Fukuda, K. Higuchi, S. Tanakamaru and K. Takeuchi, Univ. of Tokyo (Japan)
An adaptive codeword ECC is proposed for NV-RAM/NAND integrated SSDs. The acceptable raw bit error rate before ECC of NV-RAM and NAND increases by 3.6-times. The 10Gbps high-speed write is achieved with 97% power reduction.

4F 244

H-7: 3D Interconnect (Area 2)

12:05 H-7-3
Through Silicon Photonic Via with Si core for Low loss and High Density Vertical Optical Interconnection in 3D-LSI
A. Noriki, K. W. Lee, J. Bea, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We proposed through-Si photonic via with Si core (TSPV) for low-loss and high-density vertical optical interconnection in 3D-LSI. We confirmed light confinement of the TSPV and showed feasibility of very fine TSPV by 2D-FDTD simulation.

4F 245

I-7: Processing and Interface Technologies (Area 6)

11:45 I-7-3
Impact of Interface States and Bulk Carrier Lifetime on Photocapacitance of Metal/Insulator/GaN Structure
P. Bidzinski[1], M. Miczek[1], B. Admowicz[1], C. Mizue[2] and T. Hashizume[2], [1]Silesian Univ. of Tech. and [2]Hokkaido Univ. (Poland)
The capacitance of a metal/insulator/GaN ultraviolet detector has been calculated versus the light excitation intensity and the gate voltage. The influence of the interface states and bulk carrier lifetime on the photodetector characteristics has been discussed and the calculation results have been compared with experimental data.

12:15 I-7-5
New Stacked MIM Capacitors with a Side-contact Formation Technology
T. Tsutsumi, S. Sugitani, K. Nishimura and M. Ida, NTT Corp. (Japan)
We proposed new stacked MIM capacitors with electrical side-contacts, which enable to be fabricated with very few masks and a short turn-around time. We successfully fabricated five-layer stacked MIM capacitor and increase capacitance density from 0.30 fF/μmm^2 to 1.51 fF/μmm^2.

4F 246

J-7: Nanowire Growth and Applications (Area 13)

11:45 J-7-3
Electrical Characterization of InGaAs nanowire MISFETs Fabricated by Dielectric-first Process
Y. Kohashi[1], T. Sato[1], K. Tomioka[1,2], S. Hara[1], T. Fukui[1] and J. Motohisa[1], [1]Hokkaido Univ. and [2]JST-PRESTO (Japan)
We attempted gate-dielectric-first process to fabricate MISFETs using single InGaAs nanowires formed by selective-area MOVPE. We obtained improved maximum drain current as compared to our previous nanowire FETs.

12:00 J-7-4
Lateral GaAs nanowires with triangular and trapezoidal cross-sections grown on (311)B and (001) substrates
G. Zhang, K. Tateno, H. Gotoh and T. Sogawa, NTT Corp. (Japan)
The cross-sectional shape of lateral nanowires can be varied by using substrates with different orientations. Lateral nanowires with triangular and trapezoidal cross-sections were grown on (311)B and (001) substrates.

12:15 J-7-5
C-V Characteristics and Analysis of Undoped Gate-All-Around Nanowire FET Array
R. H. Baek[1], C. K. Baek[2], S. H. Lee[1], S. D. Suk[3], M. Li[3], Y. Y. Yeoh[3], K. H. Yeo[3], D. W. Kim[3], J. S. Lee[1,4], D. M. Kim[2] and Y. H. Jeong[1,4], [1]POSTECH, [2]Korea Institute for Advanced Study (KIAS), [3]Samsung Electronics Company and [4]National Center for Nanomaterials and Technology (NCNT) (Korea)
We analyzed the effect of undoped and floating channel on the nanowire C-V curves and extracted accurate inversion charge and mobility. The measured data were compared extensively with conventional planar MOS capacitor data.

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K-7: Growth and Characterization of Nitrides (Area 8)

12:00 K-7-3
Nucleus and Spiral Growth of GaN Studied by Selective-Area Metalorganic Vapor Phase Epitaxy
T. Akasaka, Y. Kobayashi and M. Kasu, NTT Corp. (Japan)
We have fabricated step-free GaN surfaces with a diameter up to 50 microns by selective-area metalorganic vapor phase epitaxy. We also discuss the mechanism of both nucleus and spiral growth of GaN in detail.

12:15 K-7-4
Enhanced optical characteristics of light-emitting-diode by localized surface plasmon of Ag/SiO_2 nanoparticles
L. W. Jang[1], T. Sahoo[1], D. S. Jo[1], J. W. Yoo[1], J. W. Jeon[1], S. M. Li[2], Y. H. Cho[2] and I. H. Lee[1], [1]Chonbuk National Univ. and [2]KAIST (Korea)
We investigated the localized surface plasmon coupling behavior in LED by Ag/SiO2 nanoparticles. The PL intensity of Ag/SiO2 coated sample was enhanced by 50 % due to the energy coupling between MQW-SP of Ag/SiO2.

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12:30-13:30 Lunch

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G-8: Bio Nanofusion Technologies (Area 11)

(13:30-15:00)
Chairs: J. Ohta (NAIST)
M. Sasaki (Toyota Technological Inst.)

13:30 G-8-1 (Invited)
Novel Quantum Effect Devices realized by Fusion of Bio-template and Defect-Free Neutral Beam Etching
S. Samukawa[1,2], [1]Tohoku Univ. and [2]JST (Japan)
A 2D Si ND array with a high-density and well-ordered arrangement could be fabricated by using bio-template and damage-free Cl neutral beam etching. In this structure, the controllable band gap energy (from 2.2eV to 1.4eV) and high photon absorption coefficient (>105 cm^{-1}) could be obtained at RT by controlling the Si-ND structure.

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H-8: 3D Integration (Area 2)

(13:30-14:55)
Chairs: T. Fukushima (Tohoku Univ.)
G. Beyer (IMEC)

13:30 H-8-1 (Invited)
Low temperature bonding for 3D integration
T. Suga, Univ. of Tokyo (Japan)
The surface activated boding (SAB) is a highly potential method providing a low temperature interconnect process inevitable for 3D integration. The applications of SAB are demonstrated on Cu direct bonding, and hetero-semiconductor wafer bonding, and the future outlook of the method will be discussed.

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I-8: Crystulline and Thin Film Silicon Solar Cell (Ⅰ) (Area 14)

(13:30-15:15)
Chairs: G. Coletti (ECW Solar Energy)
A. Masuda (AIST)

13:30 I-8-1 (Invited)
Crystalline Silicon Solar Cells, Thinner the Better
Y. Hayashi[1,2], [1]AIST and [2]Univ. of Tsukuba (Japan)
Historical trajectory of research and development of the very and ultra thin cSi solar cell/module was reviewed. According to theoretical and experimental reports, more than 20% efficiency with about 10 micro-meter thick cell is one of future targets.

2F 222

K-8: Si and Ge-based Materials and Devices (Area 8)

(13:30-15:00)
Chairs: H. Hibino (NTT Basic Res. Labs.)
A. Yamada (Tokyo Tech)

13:30 K-8-1
Very high mobility 2D holes in strained Ge quantum well epilayers grown by Reduced Pressure Chemical Vapor Deposition
M. Myronov[1], K. Sawano[2], D. R. Leadley[1] and Y. Shiraki[2], [1]Univ. of Warwick and [2]Tokyo City Univ. (UK)
For the first time, we report a very high 2DHG mobility obtained in compressive strained Ge QW epilayers grown on SiGe/Si(100) virtual substrate by an industrial type RP-CVD technique.

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A-8: Organic Transistors and Device Fabrication Ⅰ (Area 10)

14:00 A-8-2
3 V-driven flexible organic transistors with mobility exceeding 2 cm^2/Vs
K. Fukuda[1], N. Uchiyama[1], T. Sekitani[1], U. Zschieschang[2], H. Klauk[2], T. Yamamoto[3], K. Takimiya[3] and T. Someya[1], [1]Tokyo Univ., [2]Max Planck Inst. and [3]Hiroshima Univ. (Japan)
We fabricated organic TFTs using DNTT as p-type semiconductors and phosphonic acid self-assembled monolayers (SAMs) as gate insulators, and optimized the transistor characteristics by changing the alkyl chain length of the SAMs.

14:15 A-8-3
Different interfacial carrier behaviors between α-NPD and pentacene double-layer device with a polyimide blocking-layer by time-resolved optical second harmonic generation
L. Zhang, D. Taguchi, J. Li, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
The paper reports totally different carrier behaviors in α-NPD and pentacene layer in a double-layer structure by using time-resolved second harmonic generation techniques.

14:30 A-8-4
Megahertz Operation of Rectifier Circuits using Pentacene Thin-Film Transistors
M. Kitamura and Y. Arakawa, Tokyo Univ. (Japan)
We report on rectification properties of pentacene transistor diodes. The transistor diodes successfully rectify an AC voltage at a frequency above 1 MHz into a DC voltage without decrease in the output voltage.

14:45 A-8-5
Realization of Pentacene-based Thin Film Transistor Arrays for Large-area Organic Electronics Being Compatible with the Roll-to-Roll Manufacturing Technique
L. Wang[1,2], D. Li[1] and C. Jiang[1], [1]National Center for Nanoscience and Tech. and [2]Chinese Academy of Sci. (China)
In this work a vacuum thermal evaporation (VTE) is extended to a VTE-roller method that may be compatible with a roll-to-roll manufacturing technique. We show that the technique combines high uniformity with excellent performance of the deposited arrays of OTFTs on large areas.

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1F 213

C-8: Gate-Insulator Reliability (Area 1) & (Area 3)

13:50 C-8-2
Effect of Hot-Carrier Stress on the Recoverable and Permanent Components of Negative-Bias Temperature Instability
T. J. J. Ho[1], D. S. Ang[1] and C. M. Ng[2], [1]Nanyang Tech. Univ. and [2]GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)
Channel hot-hole stressing is found to reduce the apparent recoverable component of NBTI under 0-V recovery. Results show that this is a consequence of an increase in the density of deep-level hole traps.

14:10 C-8-3
Effect of Positive Gate Stressing on the Recoverable Component of Negative-Bias Temperature Instability
A. A. Boo[1], D. S. Ang[1], Z. Q. Teo[1] and C. M. Ng[2], [1]Nanyang Tech. Univ. and [2]GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)
Positive gate stressing of the p-MOSFET is found to reduce the recoverable component (R) of NBTI. This finding contradicts a current viewpoint which ascribes R to preexisting and/or high-field induced oxide trap generation.

14:30 C-8-4
Investigation of Recovery Effects on Degraded pMOSFETs of 65 nm Technology with Different Annealing Temperatures
S. Y. Chen[1], C. H. Tu[1], Y. F. Chen[1], H. S. Huang[1], Z. W. Jhou[1], S. Chou[2] and J. Ko[2], [1]National Taipei Univ. of Tech. and [2]United Microelectronics Corp. (Taiwan)
This study shows that CHC and NBTI-induced Nit can be largely recovered after annealing. It is considered that only reaction mode occurs during the degradation and recovery phases, minor or no diffusion mode has occurred.

14:50 C-8-5
Gate Leakage Current Reduction in Two-Step Processed High-k Dielectrics for Low Power Applications
G. Bersuker[1], D. Heh[1], J. Huang[1], C.S. Park[1], A. Padovani[2], L. Larcher[2], P. D. Kirsch[1] and R. Jammy[1], [1]SEMATECH and [2]Università di Modena e Reggio Emilia (USA)
Reduction of the gate leakage current in nMOS high-k devices is demonstrated by an engineered two-step deposited Hf-based high-k dielectric film. The electrical characteristics and reliability of the devices fabricated using the proposed two-step and conventional one-step high-k gate stacks are shown to be comparable.

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D-8: Si Photonics (1) (Area 7)

14:00 D-8-2
Loss Measurement of Multiple Layer a-Si Waveguides toward 3D Si-Optical Circuits
J. H. Kang, K. Inoue, Y. Atsumi, N. Nishiyama and S. Arai, Tokyo Tech (Japan)
The relationship between the propagation loss and surface roughness in multilayered a-Si waveguides has been investigated. The propagation loss was significantly affected by the top-surface roughness rather than the material absorption of a-Si.

14:15 D-8-3
Analysis of Vertically Stacked Structures of 2D PC Cavity and Amorphous-Silicon-Wire Waveguide with Low-Refractive-Index Material Cladding
T. Yamada[1,2], M. Okano[2], Y. Sakakibara[2], T. Kamei[2], J. Sugisaka[1,2], N. Yamamoto[2], M. Itoh[1], T. Sugaya[2], K. Komori[2] and M. Mori[2], [1]Univ. of Tsukuba and [2]AIST (Japan)
We proposed and theoretically investigated a highly-efficient light-extraction means from a 2D PC cavity to a silicon-wire waveguide with low-refractive-index material cladding. The high light-extraction efficiency over 90% is achieved.

14:30 D-8-4
Polarization-independent 5.4-ns Group Delay for Entire C-band by Integrated Delay Line of Si Rib Waveguide
M. Tokushima, T. Chu, A. Kamei and T. Horikawa, AIST (Japan)
We report, to the best of our knowledge, the longest polarization-independent group delay of 5.4 ns measured with a Si rib waveguide for the entire C-band of photonic telecommunication wavelengths so far. It is suggested that the rib waveguide has a great potential for integrated delay lines applicable to photonic telecommunication subsystems.

14:45 D-8-5
Bandgap Control Using Strained Beam Structures for Si-Based Photonic Devices
K. Yoshimoto, R. Suzuki, Y. Ishikawa and K. Wada, Univ. of Tokyo (Japan)
We propose method to control bandgap using Si micro-beam structure, and got significant bandgap change (~0.2eV) by inducing mechanical stress on it. This amount of strain (~1.5%) cannot be achieved by previous methods.

15:00 D-8-6
Strained SiGe-on-Si beam for tunable near-infrared light emission
R. Suzuki[1], K. Yoshimoto, L. Décosterd[1,2], Y. Ishikawa[1] and K. Wada, [1]Univ. of Tokyo and [2]Ecole Polytechnique Fédérale de Lausanne (Japan)
We propose a method to control the wavelength of near-infrared light emission from a beam-shaped germanium-rich SiGe by applying mechanical stress. Photoluminescence spectra show a bandgap narrowing under external stress, indicating a tunability of emission wavelength by applying a mechanical stress.

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E-8: PRAM/ReRAM (Area 4)

14:00 E-8-2
A SiO_2 Nano-thermal Unipolar 0T-1R ReRAM Device with Built-in Diode Isolation
K. P.Chang, H. T. Lue, K. Y. Hsieh and C. Y. Lu, Macronix Int'l Co., Ltd. (Taiwan)
Unipolar ReRAM devices using SiO2 as the storage node and an in-situ formed diode as the isolation device are studied. The extremely simple process promises potential for very low cost high-density storage.

14:20 E-8-3
Resistive Switching Device for Neuromorphic Device Application
K. Seo, I. Kim, S. Park, S. Jung, M. Siddik, J. Park, J. Kong, K. Lee, B. Lee and H. Hwang, GIST (Korea)
We mimicked various Spike Timing Dependence Plasticity (STDP) synaptic rules via resistive switching device. We showed potentiating, depressing and uniformity as well as frequency and weight dependency of the device for future neuromorphic application.

14:40 E-8-4
"A Novel Ni/WO_X /W ReRAM with Excellent Retention and Low Switching Current"
W.C. Chien[1], Y.C. Chen[1], F.M. Lee[1], Y.Y. Lin[1], E.K. Lai[1], Y.D. Yao[2], J. Gong[3], S.F. Horng[3], C.W. Yeh[1], S.C. Tsai[1], C.H. Lee[1], Y.K. Huang[1], C.F. Chen[1], H.F. Kao[1], Y.H. Shih[1], K.Y. Hsieh[1] and C. Y. Lu[1], [1]Macronix Int'l Co., Ltd., [2]Fu Jen Univ. and [3]National Tsing Hua Univ. (Taiwan)
The top electrode (TE) material plays an important role in WOX ReRAM characteristics. A novel Ni TE WOX ReRAM shows superior performances such as a switching current density < 8x105A/cm2, > 100X resistance ratio window, and extremely good data retention of > 300 years at 85 °C.

15:00 E-8-5 (Late News)
Microstructural Characterization in Reliability Measurement of PRAM
J. Bae, K. Hwang, K. Park, S. Jeon, D. H. Kang, S. Park, J. Ahn, S. Kim, G. Jeong and C. Chung, Samsung Electronics Co., Ltd. (Korea)
The cell failures after cycling endurance in PRAM have been classified into 3 groups (Stuck set, Stuck reset, tails from reset distribution), which have been analyzed by TEM.

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F-8: Spintronics (Ⅲ) - Semiconductors - (Area 12)

14:00 F-8-2 (Invited)
Electrical detection of Spin Transport in Si using High-quality Schottky Contacts
K. Hamaya[1,2], Y. Ando[1] and M. Miyao[1], [1]Kyushu Univ. and [2]PRESTO, JST (Japan)
We show high-quality formation of ferromagnetic Schottky source and drain contacts for spin-transistor applications, and demonstrate electrical spin injection and detection in Si using these contacts.

14:30 F-8-3
Spin injection into GaAs from Fe/GaO_x Tunnel Injector
H. Saito[1], J. C. Le Breton[2], V. Zayets[1], Y. Mineno[1,3], S. Yuasa[1] and K. Ando[1], [1]National Inst. of Adv. Indus. Sci. and Tech, [2]Univ. of Twente and [3]Toho Univ. (Japan)
We examined the electrical injection of spin-polarized electrons into a GaAs-based light-emitting diode structure from a Fe/GaO_x tunnel injector whose electron-charge injection efficiency was comparable to that of a conventional Fe/n$^+$AlGaAs ohmic injector.

14:45 F-8-4
Large magnetoresistance of $Ge_{1-x}Mn_x$ single films and heterostructures with magnetic nanocolumns
S. Yada, R. Okazaki and M. Tanaka, Univ. of Tokyo (Japan)
We observed large positive magnetoresistance in single films and heterostructures of $Ge_{1-x}Mn_x$ with amorphous $Ge_{1-y}Mn_y$ nanocolumns. Hysteretic behavior of magnetoresistance was also observed in the heterostructure, which might be caused by magnetization of $Ge_{1-x}Mn_x$.

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G-8: Bio Nanofusion Technologies (Area 11)

14:00 G-8-2
Planer Multi Electrode Array Coupled CMOS Image Sensor for in vitro Electrophysiology
A. Nakajima[1], T. Noda[1,2], K. Sasagawa[1,2], T. Tokuda[1,2], Y. Ishikawa[1,2], S. Shiosaka[1,2] and J. Ohta[1,2], [1]NAIST and [2]JST-CREST (Japan)
Multi-electrode Array Coupled CMOS image (MARC) sensor was designed for *in vitro* electrophysiology. We report design of MARC sensor, fabrication of Pt black microelectrode and a preliminary result from functional validations by imaging mouse brain slice.

14:15 G-8-3
Atmospheric Pressure Micro Inductively Coupled Plasma Light Source towards Portable Spectrometry System
S. Kumagai[1], H. Matsuyama[1], M. Hori[2] and M. Sasaki[1], [1]Toyota Technological Inst. and [2]Nagoya Univ. (Japan)
Atmospheric pressure inductively coupled plasma device is developed from glass epoxy substrate for portable light source. Plasma generation at 35W RF power is confirmed. Emission spectra with sharp peaks and the device durability are demonstrated.

14:30 G-8-4
Controlled Thermal Emission of Narrow-band IR Waves for Downsizing Sensor Module
K. Masuno, S. Kumagai and M. Sasaki, Toyota Technological Inst. (Japan)
New narrow-band wavelength selective IR emitter suitable for downsizing is proposed. Radiance peak at λ=1.67μm, which corresponds to Wood's anomaly of grating, and higher power efficiency are confirmed.

14:45 G-8-5
Fabrication and Location of 3-nm Pt Wires onto Silicon Surfaces
M. Kobayashi[1,2], K. Onodera[2], Y. Watanabe[3], K. Shiba[1] and I. Yamashita[2,4], [1]Japanese Foundation for Cancer Res., [2]NAIST, [3]Univ. of Tokyo and [4]Panasonic Corp. (Japan)
Fabrication and location of high aspect ratio 3-nm Pt wires onto silicon surfaces was achieved using a tube-shaped tobacco mosaic virus, which could not be achieved using conventional lithography.

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H-8: 3D Integration (Area 2)

14:00 H-8-2
Self-Assembly with Metal Microbump-to-Microbump Bonding for Advanced Chip-to-Wafer 3D Integration
E. Iwata, Y. Ohara, K. W. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We demonstrate highly productive microbump-to-microbump bonding method for the chip-to-wafer 3D integration. We aligned chips onto Si wafer using self-assembly method and established conduction of daisy chains having 5-, 10-um-size microbumps.

14:20 H-8-3
Metal Micro-Bump Induced Stress in 3D-LSIs _ a micro-Raman Study
M. Murugesan, Y. Ohara, J. C. Bea, K. W. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
In the flip-chip bonded 3D-LSI die/wafer via metal micro bump, the metallic micro-joint exerted a large compressive stress for the region underneath the micro-bump, and it is extended up to more than 10 μm. Since this value is pretty close to the depletion region thickness, and for extremely thin LSI die/wafer it would have an adverse impact on the device characteristics.

14:40 H-8-4 (Late News)
High Density and Power Efficient SiP with SCS Technology
E. Hosomi[1], Y. Matsubara[1], Y. Fujimoto[1], M. Oida[2], H. Ezawa[1], M. Fukuda[1], K. Numata[1] and K. Miyamoto[1], [1]Toshiba Corp. and [2]J-Devices Corp. (Japan)
SiP with SCS (stacked chip SoC) enables high bandwidth connection between logic and memory devices. SCS technology has advantage against eDRAM in reliability and cost. SCS offers low power solution compared to the conventional SiP structure with wire bonding.

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I-8: Crystulline and Thin Film Silicon Solar Cell (Ⅰ) (Area 14)

14:00 I-8-2
Enhanced Power Conversion Efficiency for Silicon Solar Cells Utilizing a Uniformly Distributed Indium-Tin-Oxide Nano-Whiskers
C. H. Chang[1], M. H. Hsu, W. L. Chang[2], W. C. Sun and P. Yu[1], [1]National Chiao Tung Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
Distinctive ITO nano-whiskers, grown by electron-beam evaporation, have been employed as a cost-effective ARC for Si solar cells. The nanostructure exhibits excellent anti-reflection for the wavelength range of 450nm~1050nm. The ITO-whiskers cell achieves 17.1% efficiency.

14:15 I-8-3
Microstructures of polycrystalline silicon films formed through explosive crystallization induced by flash lamp annealing
K. Ohdaira[1,2], S. Ishii[1], N. Tomura[1] and H. Matsumura[1], [1]JAIST and [2]JST (Japan)
Flash lamp annealing (FLA) induces explosive crystallization, lateral crystallization driven by the liberated latent heat, and TEM observations have clarified the microstructures of the flash-lamp-crystallized poly-Si films having periodic two characteristic regions formed spontaneously during the explosive crystallization.

14:30 I-8-4
Stacked Solar Cells using Transparent and Conductive Adhesive
J. Takenezawa[1], M. Hasumi[1], T. Sameshima[1], T. Koida[2], T. Kaneko[2], M. Karasawa[2] and M. Kondo[2], [1]Tokyo Univ. of Agri. And Tech. and [2]AIST (Japan)
We demonstrate multi-junction solar cells by stacking top a-Si:H p-i-n cell on bottom HIT silicon cell using polyimide transparent adhesive dispersed with ITO conductive particles. The Voc increased to 1.34V under illumination of AM 1.5.

14:45 I-8-5
In-situ observation of polycrystalline Si thin films grown using Al-doped ZnO on glass substrate by the aluminum-induced crystallization
M. Jung[1], A. Okada[2], T. Saito, T. Suemasu[2] and N. Usami[1], [1]Tohoku Univ. and [2]Univ. of Tsukuba (Japan)
Recently, the poly-Si thin film grown on glass substrate is attracting for large area electronic and solar cell applications [1,2]. As a common approach of crystallizing amorphous Si (a-Si), there are solid phase crystallization [3], excimer laser annealing [4], and metal-induced crystallization (MIC) [5-7]. Among them, the MIC process using metals such as Ni, Ag, Al, and Au is promising to obtain large-grained high quality material with low thermal budget.

15:00 I-8-6
Photothermal Spectroscopy by Atomic Force Microscopy on Crystalline Silicon Solar Cell Materials
K. Hara and T. Takahashi, Univ. of Tokyo (Japan)
We have performed the PT spectroscopy by AFM on single crystalline Si solar cell materials and discussed the influences of the surface recombination as well as the minority carrier diffusion length on the PT signals.

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K-8: Si and Ge-based Materials and Devices (Area 8)

13:45 K-8-2
Formation of Pyramidal-shaped Etch Pits on Germanium Surfaces Using Catalytic Reactions with Metallic Nanoparticles in Water
T. Kawase, K. Nishitani, K. Dei, J. Uchikoshi, M. Morita and K. Arima, Osaka Univ. (Japan)
We present an environmentally friendly formation of pyramidal-shaped etch pits on a Ge(100) surface with metallic nanoparticles in water. We also discuss a possible mechanism by electronic energy relationships.

14:00 K-8-3
Fabrication of defect-free and relaxed Ge-rich SGOI-wire structures for CMOS applications
M. Oda, Y. Moriyama, K. Ideda, Y. Kamimuta and T. Tezuka, MIRAI-TOSHIBA (Japan)
Strain-relaxed and defect-free SGOI wire structures were demonstrated by the proposed condensation-melting-recrystallization process. This technique will enable us to fabricate non-planar Ge-rich SGOI CMOS devices with additional stressor techniques for high-performance or low-power consumption applications.

14:15 K-8-4
Fabrication of Poly-Si TFT on Polycarbonate Substrate at Temperatures below 135°C
G. Nakagawa[1], N. Kawamoto[2], T. Imamura[3], Y. Tomizawa[3], T. Miyoshi[2], K. Tadatomo[2] and T. Asano[1], [1]Kyushu Univ., [2]Yamaguchi Univ. and [3]TEIJIN Ltd. (Japan)
We demonstrate the fabrication of poly-Si TFTs on polycarbonate substrate at temperatures below 135°C, i.e. well below the glass transition temperature of polycarbonate. TFTs whose electron mobility is over 10 cm^2/Vs can be fabricated.

14:30 K-8-5
Strain-Induced Back Channel Electron Mobility Enhancement in Poly-Si TFTs Formed by Continuous-Wave Laser Lateral Crystallization
S. Fujii, S. I. Kuroki, K. Kotani and T. Ito, Tohoku Univ. (Japan)
The back interface of the CLC poly-Si films had larger tensile strain than the surface. As a result, back channel electron mobility was 1.2 times larger than front channel electron mobility.

14:45 K-8-6
Epitaxial $NiSi_2$ Buffer Technique for Fluoride Resonant Tunneling Devices on Si
K. Takahashi, Y. Yoshizumi, Y. Fukuoka, N. Saito and K. Tsutsui, Tokyo Tech (Japan)
To fabricate CaF2/CdF2/CaF2 RTDs on Si, we propose the introduction of NiSi2 buffer layers to control the chemical reaction between Si and CdF2. We investigated the growth condition of NiSi2 on Si.

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Coffee Break (2F Forum)

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A-9: Organic Transistors and Device Fabrication Ⅱ (Area 10)
(15:30-17:15)
Chairs: S. Aratani (Hitachi, Ltd.)
M. Nakamura (Chiba Univ.)

15:30 A-9-1
Excellent interface properties of pentacene based metal-oxide-semiconductor diodes utilizing HfON higk-κ gate insulator
M. Liao, Y. U. Song, J. Ishikawa, T. Sano, J. Gao, H. Ishiwara and S. Ohmi, Tokyo Tech (Japan)
Pentacene based MOS diodes using SiO_2, HfO_2 and HfON as gate insulators were investigated. It was found that pentacene based MOS diodes with HfON gate insulators show a small flat-band voltage shift and a negligible frequency dispersion in C-V characteristics.

15:45 A-9-2
Oxygen Plasma Process of Self-assembled Monolayer Gate Dielectric for 2-V Operation High-mobility Organic TFT
K. Kuribara[1], T. Nakagawa[1], K. Fukuda[1], T. Yokota[1], T. Sekitani[1], U. Zschieschang[2], H. Klauk[2], T. Someya[1], T. Yamamoto[3] and K. Takimiya[3], [1]Univ. of Tokyo, [2]Max Planck Inst for Solid State Res. and [3]Hiroshima Univ. (Japan)
We optimized parameters of oxgen plasma process of self-assembled monolayer gate dielectric for organic TFTs. Short exposure time of plasma process (200 W, 30 sec.) products good transistors with high mobility of 0.97 cm^2/Vs and small hysteresis.

16:00 A-9-3
Direct observation of carrier behavior leading to electroluminescence in tetracene field-effect transistor
Y. Ohshima, H. Satou, T. Manaka, H. Kohn, N. Hirako and M. Iwamoto, Tokyo Tech (Japan)
We probed the carrier behavior leading to the electroluminescence under AC electric field in tetracene field-effect transistor using optical second harmonic generation technique, and clarified the space charge field effect on carrier injection.

16:15 A-9-4
Diffuser micropump structured with extremely flexible diaphragm of 2 micron-thick polyimide film
Y. Liu, H. Komatsuzaki, Z. Duan and Y. Nishioka, Nihon Univ. (Japan)
The simple structured air-actuated valveless micropump with the 2.1 micron-thick polyimide membrane was designed, fabricated and measured. The micropump was fabricated on the 60 micron-thick thin Si wafer using surface micromachining techniques.

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B-9: Interface and Strain Characterization (Area 1)
(15:30-17:10)
Chairs: O. Nakatsuka (Nagoya Univ.)
S. Migita (AIST)

15:30 B-9-1
Measurements of Electrostatic Potential Across p-n Junctions on Oxidized Si Surfaces by Scanning Multi-Mode Tunneling Spectroscopy
L. Bolotov, T. Tada, M. Iitake, M. Nishizawa and T. Kanayama, AIST (Japan)
High-resolution measurements of the surface potential was demonstrated on oxidized Si surfaces by scanning multi-mode tunneling spectroscopy at optimized tunneling gap. The potential maps agree with build-in potential for p-n junctions, while nanometer-scale fluctuations were caused by structural and charge variations.

15:50 B-9-2
Interfacial atomic structure between Pt-added NiSi and Si (001)
N. Ikarashi, M. Narihiro and T. Hase, Renesas Electronics Corp. (Japan)
HAADF-STEM revealed that Pt segregates at lattice-matched areas of the interface and occupied the Ni sites at the first interfacial atomic layer of NiSi. This finding shows that Pt segregates to lower the interfacial strain, reducing the interface energy. Thus, we infer that the interface-energy lowering results in the NiSi layer being stabilized.

16:10 B-9-3
TO- and LO-mode analyses in asymmetric stretching vibrations in ultra thin thermally grown GeO_2 on Ge substrate
M. Yoshida[1], T. Nishimura[1,2], C. H. Lee[1], K. Kita[1,2], K. Nagashio[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
A IR investigation of thin GeO_2 was performed for the first time, with a conscious of both TO and LO modes. Local bond feature such as the bridging bond angle is governed by the oxidation temperature just like that in SiO_2, while macroscopic one such as void defect seems to be determined by both temperature and pO_2.

16:30 B-9-4
Quantitative Analysis of Stress Relaxation in TEM specimen fabrication by Raman Spectroscopy with High-NA Oil-Immersion Lens
D. Kosemura[1,2] and A. Ogura[1], [1]Meiji Univ. and [2]JSPS (Japan)
The stress relaxation in the TEM specimens of SSOI was evaluated by Raman spectroscopy with high-NA oil-immersion lens. It was confirmed that the values of the relaxation was 75% at the thickness of 240 nm.

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C-9: Emerging Device Technology (Area 3)
(15:30-17:15)
Chairs: D. Hisamoto (Hitachi, Ltd.)
S. Hayashi (Panasonic Corp.)

15:30 C-9-1 (Invited)
CVD Graphene for High Speed Electronics
B. C. Huang, C. Q. Miao, Y. Wang, Y. H. Xie and J. C. S. Woo, UCLA (USA)
Few-layer graphene film was deposited on Ni film and Ni dots using CVD method. Under low temperature growth condition, the uniformity of graphene was remarkably improved. Top-gated graphene transistors are made by transferring the graphene film onto a SiO2 substrate. Ambipolar conduction is clearly observed from I_{DS}-V_{GS} curve

16:00 C-9-2
High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization
J. Mitard[1], B. De Jaeger[1], G. Eneman[2,3], A. Dobbie[4], M. Myronov[4], M. Kobayashi[5], J. Geypen[1], H. Bender[1], B. Vincent[1], R. Krom[2], J. Franco[2], G. Winderickx[1], E. Vrancken[1], W. Vanherle[1], W. E. Wang[1], J. Tseng[6], R. Loo[1], K. De Meyer[2], M. Caymax[1], L. Pantisano[1], D. R. Leadley[4], M. Meuris[1], P. P. Absil[1], S. Biesemans[1] and T. Hoffmann[1], [1]IMEC, [2]K.U Leuven, [3]FWO, [4]Univ. of Warwick, [5]Stanford Univ. and [6]TSMC (Belgium)
High hole-mobility 65nm biaxially-strained Ge-pFETs, with reduced EOT while maintaining minimized SCE, have been fabricated and electrically characterized in-depth for the low and high field transport. We demonstrate a 35%-I_{ON} gain for nano-scaled s-Ge pFETs.

16:40 C-9-4
Analysis of the Junctionless Transistor Architecture
J. P. Colinge[1], J. P. Raskin[2], A. Kranti[1], I. Ferain[1], C. W. Lee[1], N. Dehdashti Akhavan[1], P. Razavi[1], R. Yan[1] and R. Yu[1], [1]Univ. College Cork. and [2]Université catholique de Louvain (Ireland)
Strain is used to improve mobility in junctionless transistors. A bulk silicon version of the device is studied by simulation, and performance similar to that of the SOI version of the device are obtained.

2F 221

D-9: Si Photonics (2) (Area 7)
(15:30-17:15)
Chairs: H. Yamada (Tohoku Univ.)
M. Tokushima (AIST)

15:30 D-9-1
Real-time synchrotron radiation X-ray diffraction and abnormal temperature dependence of photoluminescence from erbium silicates on SiO_2/Si substrates
H. Omi[1], T. Tawara[1], M. Tateishi[1], H. Komatsu[1], S. Takeda[2], Y. Tsusaka[3], Y. Kagoshima[3] and J. Matsui[2], [1]NTT Basic Res. Labs., [2]Univ. of Hyogo and [3]CAST (Japan)
We characterized the formation of erbium silicates on silicon oxide films in real time using synchrotron radiation grazing incidence X-ray diffraction (GIXD). We also characterized light emission from the erbium silicates by photoluminescence measurements.

15:45 D-9-2
Evaluation of optical absorption and light propagation loss in $Er_xY_{2-x}SiO_5$ crystal waveguides
K. Homma, T. Nakajima, T. Kimura and H. Isshiki, Univ. of Electro-Communications (Japan)
We demonstrate introduction of ErxY2-xSiO5 to the waveguide, resulting in suppression of CUC in this system. And optical absorption cross section of Er ions and light propagation loss in the ErxY2-xSiO5 crystal waveguide are evaluated.

16:00 D-9-3
Design and Simulation of Silicon Ring Optical Modulator with p/n Junctions along Circumference
Y. Amemiya, H. Ding and S. Yokoyama, Hiroshima Univ. (Japan)
Silicon ring optical modulator with p/n junctions along circumference is proposed. Its performance at 1 V is simulated. The modulation > 95% is obtained at $1x10^{17}$-$5x10^{17}$ cm^{-3} carrier concentration and propagation loss < 5 dB/cm.

16:15 D-9-4
Design of Broadband Optical Switch Based on Mach-Zehnder Interferometer with Si wire Waveguides
K. Kintaka, Y. Shoji, S. Suda, H. Kawashima, T. Hasama and H. Ishikawa, AIST (Japan)
2x2 optical switches based on Mach-Zehnder interferometer (MZI) with Si wire waveguides are designed for broadband operation. Wavelength dependences of MZI switches using directional couplers, multimode interference couplers, and wavelength-insensitive couplers are calculated numerically.

4F 241

E-9: ReRAM (Area 4:)
(15:30-17:15)
Chairs: K. Ishihara (Sharp Corp.)
K. Hamada (Elpida Memory, Inc.)

15:30 E-9-1 (Invited)
Overview and Future Challenges of Hafnium Oxide ReRAM
Y. S. Chen[1,2], H. Y. Lee[1,2], P. S. Chen[3], P. Y. Gu[1], Y. Y. Hsu[1], W. H, Liu[1], C. H. Tsai[1], S. M. Wang[1], S. S. Sheu[1], P. C. Chiang[1], W. P. Lin[1], W. S. Chen[1], F. T. Chen[1], C. H. Lien[2] and M. J. Tsai[1], [1]ITRI, [2]National Tsing Hua Univ. and [3]Mingshin Univ. of Sci. and Tech. (Taiwan)
A highly reliable Hafnium Oxide ReRAM with high speed, low power operation, and excellent reliabilities including nonvolatility and endurance is demonstrated. A 1 Kb array with robust cycling endurance can be achieved by effective verifications. Some challenges must be overcome to realize this memory as a promising nonvolatile memory.

16:00 E-9-2
A New Tunneling Barrier Width Model of the Switching Mechanism in Hafnium Oxide-Based Resistive Random Access Memory
Y. H. Tseng[1], S. S. Chung[1,2], S. Shin[2], S. S. M. Kang[2], H. Y. Lee[3] and M. J. Tsai[3], [1]National Chiao Tung Univ., [2]Univ. of California, Merced and [3]ITRI (Taiwan)
In this paper, the switching characteristics of Ti/HfO2/TiN resistive random access memory (RRAM) have been examined. A novel tunneling barrier width model based on WKB approximation is proposed to explain the pertinent current-voltage characteristic and the origin of the resistance changing in RRAM.

16:20 E-9-3
High OFF/ON-resistive NiO ReRAM using Post-Plasma-Oxidation (PPO) process
K. Okamoto, M. Tada, K. Ito, Y. Saito, S. Ishida and H. Hada, NEC Corp. (Japan)
NiO resistive change cells with a high OFF/ON resistance ratio of 10^5 are realized using low temperature, post-plasma-oxidation (PPO) while reducing cell-to-cell variation of forming voltages.

16:40 E-9-4
Effects of Reactive Ti Creating Oxygen Vacancy Inside TiO_2 on Resistive Switching Characteristics in Resistive Random Access Memory Device
S. J. Kim, M. G. Sung, W. G. Kim, J. Y. Kim, J. H. Yoo, J. N. Kim, B. G. Gyun, J. Y. Byun, M. S. Joo, J. S. Roh and S. K. Park, Hynix Semiconductor Inc. (Korea)
The effects of reactive Ti layer on the resistive switching characteristics of TiO2-based ReRAM are investigated. Ti acts as a good oxygen gettering layer which makes the TiO2 to have a higher concentration of oxygen vacancy.

4F 242

F-9: Spintronics (Ⅳ) - Device and Circuits - (Area 12)
(15:30-17:00)
Chairs: K. Ando (AIST)
M. Yamamoto (Hokkaido Univ.)

15:30 F-9-1 (Invited)
Spin transfer torque effects in nanopillar devices with perpendicular anisotropy
S. Mangin, IJL – Nancy Université (France)
Spin-polarized current is used to reverse magnetization orientation in nanomagnets with strong perpendicular anisotropy. We will discuss the efficiency of such geometry, dynamic behaviours as well as domain nucleation and propagation while a field is applied and a current is injected in the nanopillar

16:00 F-9-2
High Speed Spin-Transfer Switching in GMR Nanopillars with Perpendicular Anisotropy
H. Tomita[1], T. Nozaki[1], T. Seki[1], T. Nagase[2], E. Kitagawa[2], M. Yoshikawa[2], T. Daibou[2], M. Nagamine[2], S. Ikegawa[2], N. Shimomura[2], H. Yoda[2] and Y. Suzuki[1], [1]Osaka Univ. and [2]Toshiba R & D center (Japan)
We investigated high-speed (sub-nano second) spin-transfer switching property in giant magnetoresistance (GMR) nanopillar systems with perpendicular magnetic anisotropy.

16:15 F-9-3
Hierarchical Nonvolatile Memory with Perpendicular Magnetic Tunnel Junctions for Normally-Off Computing
K. Abe, K. Nomura, S. Ikegawa, T. Kishi, H. Yoda and S. Fujita, Toshiba Corp. (Japan)
Hierarchical nonvolatile-memory composed of embedded-MRAM for L3 cache and nonvolatile-SRAM with MTJs for L2 cache is proposed. The average power of microprocessor with the hierarchical nonvolatile-memory is reduced by 65% in long standby time.

16:30 F-9-4
Design of a Process-Variation-Aware Nonvolatile MTJ-Based Lookup-Table Circuit
D. Suzuki, M. Natsui, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)
This paper presents a process-variation-aware nonvolatile lookup table circuit for nonvolatile field-programmable gate array with ultra-low power and immediate wakeup capability using MOS/MTJ hybrid structure.

Friday, September 24

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G-9: Nanomaterial Applications (Area 11) (15:30-16:30) Chairs: I. Yamashita (NAIST) K. Sawada (Toyohashi Univ. of Tech.)	**H-9: Image Sensor (Area 2)** (15:30-16:25) Chairs: M. Kodera (Toshiba Corp.) M. Matsuura (Renesas Electronics Corp.)	**I-9: Crystulline and Thin Film Silicon Solar Cell (Ⅱ) (Area 14)** (15:30-16:45) Chairs: Y. Hayashi (AIST) N. Usami (Tohoku Univ.)			
15:30 G-9-1 **Free-Standing Lipid Bilayers Based on Nanoporous Alumina Films** *A. Hirano-Iwata[1,2], T. Taira[1], A. Oshima[1], Y. Kimura[1] and M. Niwano[1], [1]Tohoku Univ. and [2]PRESTO, JST (Japan)* Mechanical stability of free-standing bilayer lipid membranes (BLMs) was improved by suspending the BLMs in nanoporous alumina films. The membrane stability was investigated in terms of lifetime and breakdown voltage.	**15:30 H-9-1** **Characterization of LTO coating on microlens of CMOS image sensor** *J. Gambino, B. Leidy, C. Musante, K. Ackerson, B. Guthrie, J. Twombly, E. Cooney, P. Pokrinchak, D. Meatyard, J. Adkisson, R. J. Rassel and M. Jaffe, IBM (USA)* CMOS image sensors with an LTO coating on the microlens have been characterized for dark current, quantum efficiency, and reliability.	**15:30 I-9-1 (Invited)** **Impact of Metal Contamination in Silicon Solar Cells** *G. Coletti, ECN Solar Energy (the Netherlands)* Impact of transition metals on the conversion efficiency of silicon solar cells is presented. Fe, Cr and Ti reduce the internal quantum efficiency (IQE) at long wavelength reducing the carrier diffusion length. Ni reduces the IQE at short wavelength increasing recombination in the solar cell emitter region. Cu reduces the IQE at both short and long wavelength. A physical model is presented explaining the data.			
15:45 G-9-2 **Fabrication of CMOS-compatible Poly-Si Nanowire FET Sensor** *H. Y. Chen[1,2], C. Y. Lin[2], M. C. Chen[2], H. C. Chen[2], C. C. Huang[2] and C. H. Chien[1,2], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)* A low-cost, superior uniformity Poly-Si nanowire FET sensor fabrication method features entire CMOS processing is presented. A self-aligned nanowire fabrication in bulk-Si technology is also disclosed for the first time for highly integrated sensor system design.	**15:50 H-9-2** **Near-Infrared Image Sensor Fabricated Using Compliant Bump** *N. Watanabe[1,3], F. Hoashi[1], Y. Nagai[2], H. Inada[2], Y. Iguchi[2] and T. Asano[1], [1]Kyushu Univ. , [2]Sumitomo Electric Industries, Ltd. and [3]Fukuoka Industry Sci. and Tech. Foundation (Japan)* We demonstrated a near-infrared image sensor in which an InGaAs/InP photodiode chip was electrically connected to a CMOS read-out circuit chip through compliant bumps.	**16:00 I-9-2** **Optimum design of a-Si:H/μc-Si:H tandem thin film solar cells with a low-refractive-index AZO transparent conducting oxide** *J. W. Leem and J. S. Yu, Kyung Hee Univ. (Korea)* Aluminum-doped zinc oxide (AZO) thin films with low-refractive-index (low-n) as a transparent conducting oxide (TCO) layer for Si solar cells are deposited on Si and glass substrates by rf magnetron sputter using an oblique angle deposition technique. To improve the efficiency, the a-Si:H/μc-Si:H tandem solar cells with a TCO layer of low-n AZO are designed using a Silvaco ATLAS simulation.			
16:00 G-9-3 (Late News) **Carbon nanotube-based sensor Device compatible with the CMOS process** *J. T. Huang, P. L. Hsu, T. H. Lin, W. T. Hsieh, K. Y. Lee, C. K. Chen and T. C. Tsai, National Taipei Univ. of Tech. (Taiwan)* This paper presents a low temperature fabrication method of Carbon Nanotubes(CNTs)-based sensors device on a CMOS integrated circuit chip made by TSMC 0.35μm CMOS process.	**16:10 H-9-3 (Late News)** **MEMS Resonance Test for Mechanical Characterization of Nano-Scale Thin Films** *H. Yamagiwa[1], D. Goto[1], T. Namazu[1], T. Takeuchi[2], K. Murakami[2], Y. Kawashimo[2], T. Takano[3], K. Yoshiki[1] and S. Inoue[1], [1]Univ. of Hyogo, [2]Shinko Seiki Co. Ltd. and [3]The New Industry Research Organization (Japan)* The purpose of this study is to develop a quantitative measurement method for the Young's modulus of nanometer-thick films. We developed the test technique using a MEMS resonator array and measured the Young's moduli of Al and plasma-polymerization films made from CH4 and CHF3 gases.	**16:15 I-9-3** **Efficiency enhancement of a-Si thin film solar cells by using different light trapping structures** *C. W. Kuo[1], W. P. Chu[1], J. S. Lin[2,3], T. C. Lin[4], Y. S. Tsai[1], F. S. Juang[1], M. H. Chung[5], T. E. Hsieh[5] and M. O. Liu[3], [1]National Formosa Univ., [2]Osaka Univ., [3]Industrial Tech. Res. Inst., [4]KunSan Univ. and [5]National Chiao Tung Univ. (Taiwan)* This study produced various light trapping structures in order to enhance efficiency for a-Si solar cells. When combining V-shape with a cross-like pattern, Jsc and efficiency were shown to increase to 12.35mA/cm2 and 6.29%, respectively.			
16:15 G-9-4 (Late News) **Light-Addressable Potentiometric Sensors for Sodium Ion Detection by Fluorinated-Atomic Layer Deposition Hafnium Oxide Membrane** *C. H. Chin[1], J. H. Yang[1], T. F. Lu[1], C. E. Lue[1], C. M. Yang[2] and C. S. Lai[1], [1]Chang Gung Univ. and [2]Inotera memories Inc. (Taiwan)* In this study, an inorganic method was investigated for Na+ detection based on LAPS. The sensing membrane, HfO2 layer, was deposited by ALD and treated by RTA and CF4 plasma. The pH sensitivity was decreased and pNa sensitivity was increased by CF4 plasma. Finally, the highest pNa sensitivity was 34.8 mV/pNa measured from pNa 1 to pNa 4.		**16:30 I-9-4** **Three-terminal a-Si solar Cells** *C. H. Tai, C. H. Lin, C. M. Wang and C. C. Lin, National Dong Hua Univ. (Taiwan)* A new back-to-back pin-nip structure increases the average electric field in a solar cell. The 0.28-m-thick three-terminal a-Si solar cell achieved an efficiency of 11.4 %.			

Friday, September 24

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A-9: Organic Transistors and Device Fabrication Ⅱ (Area 10)

16:30 A-9-5
Printed Electrode for All-Printed Polymer Diode
M. Yoshida, K. Suemori, S. Uemura, S. Hoshino, N. Takada, T. Kodzasa and T. Kamata, AIST (JAPAN)
We have developed a mechanical sintering technique for printed metal patterns. Using this technique, printed electrode with various work functions from 3.5eV to 5eV could be prepared on a plastic substrate. These printed alloys were effective to improve the performance of printed diode and transistors.

16:45 A-9-6
A Tunable Emission Prepared by Novel Photo-induced Color-Change Materials
W. T. Liu and W. Y. Huang, National Sun Yat-sen Univ. (Taiwan)
An organic phospher C-545T was used as a green light dopant in this study. After protonation the protonated C-545T could be transformed into an orange or red emitter depending on the degree of protonation. Accordingly, green, orange and red emitting layers were fabricated by doping C-545T in PAG containing resin with different light exposures. In conjunction with a blue-light pumping source, the above emitting layers could be easily integrated into a white light emission.

17:00 A-9-7 (Late News)
Fabrication of Sol-Gel Alumina Dielectric for Low-Voltage Operating Pentacene Transistor
K. K. Han[1] and S. Seo[2], [1]Seoul National Univ. and [2]Kyungwon Univ. (Korea)
A sol-gel alumina dielectric for pentacene transistor has been introduced. With this alumina dielectric, the low voltage pentacene thin film transistor is fabricated and it is free from the threshold voltage shift problems.

1F 212

B-9: Interface and Strain Characterization (Area 1)

16:50 B-9-5
Uniaxial and Biaxial Strain Distribution Mapping in SOI Micro-Structures by Polarized Raman Spectroscopy
M. Kurosawa[1,2], T. Sadoh[1] and M. Miyao[1], [1]Kyushu Univ. and [2]JSPS (Japan)
We have newly developed a polarized Raman spectroscopy technique, which uses special polarization configurations of the incident and scattered light. This enables the evaluation of strain axis distributions in SOI structures for the first time. This technique is a powerful tool to optimize the strained SOI micro-structures of the advanced LSIs.

1F 213

C-9: Emerging Device Technology (Area 3)

17:00 C-9-5 (Late News)
Short-Channel Junctionless Nanowire Transistors
C. W. Lee, I. Ferain, A. Kranti, N. Dehdashti Akhavan, P. Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, S. Gheorghe, R. Murphy and J. P. Colinge, Univ. College Cork (Ireland)
Junctionless silicon nanowire transistors with a gate length down to 50 nm have been demonstrated. The devices show very small short-channel effects: SS=60mV/dec, DIBL=7mV.

2F 221

D-9: Si Photonics (2) (Area 7)

16:30 D-9-5
Development of Accelerometer Using Mach-Zehnder Interferometer Type Optical Waveguide
M. Suzuki[1], K. Nishioka[1], T. Takahashi[1], S. Aoyagi[1], Y. Amemiya[2], M. Fukuyama[2] and S. Yokoyama[2], [1]Kansai Univ. and [2]Hiroshima Univ. (Japan)
A novel inertial force sensor which uses a Mach-Zehnder Interferometer (MZI) type optical waveguide made of crystal silicon is developed. In this sensor, one branched waveguide of the MZI have floating beam structure which is formed by removal of its underlying SiO2 layer.

16:45 D-9-6
10-GHz Operation of a PLZT Electro-Optic Modulator with a Ring Resonator Formed on a Silicon Substrate
T. Shimizu[1,2], M. Nakada[1], H. Tsuda[3], H. Miyazaki[1], J. Akedo[3] and K. Ohashi[1,2], [1]MIRAI-Selete, [2]NEC Corp. and [3]AIST (Japan)
We developed a PLZT electro-optic modulator with a ring resonator formed on silicon substrate by aerosol deposition. A 10-GHz optical output signal was produced by the modulator with a resonator size of 150x190 micron.

17:00 D-9-7
Crosstalk inprovement in Si-wire optical cross-bar switch
H. Kawashima, Y. Shoji, K. Kintaka, S. Suda, T. Hasama and H. Ishikawa, AIST (Japan)
Improvement of crosstalk by cascading Si-wire cross-bar switches is demonstrated. Achieved lowest crosstalk is -50 dB for the bar state and is -30 dB for the cross state. We discuss on the limiting factors.

4F 241

E-9: ReRAM (Area 4:)

17:00 E-9-5 (Late News)
Novel Low Power RRAM with a U-type Cell Structure for Improving Resistive Switching Characteristics
K. C. Ryoo[1,2], J. H. Oh[1,2], S. Jung[1], H. Jeong[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)
We propose a novel RRAM structure which makes it possible to reduce the reset current by controlling the number of the electrical path. Numerical simulation is also performed to investigate the optimal process condition.

4F 242

F-9: Spintronics (Ⅳ)- Device and Circuits - (Area 12)

16:45 F-9-5 (Late News)
Magnetic Field Dependence of Quadrupoar Splitting and Nuclear Spin Coherence in a (110) GaAs/AlGaAs Quantum Well
J. Ishihara, M. Ono, G. Sato, S. Matsuzaka, Y. Ohno and H. Ohno, Tohoku Univ. (Japan)
We investigated magnetic field dependences of quadrupoar splitting in the NMR spectrum, the nuclear decoherence time, and the dephasing time involving the inhomogeneous broadening in a (110) GaAs quantum well (QW).

Friday, September 24

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-9: Nanomaterial Applications (Area 11)	H-9: Image Sensor (Area 2)	I-9: Crystulline and Thin Film Silicon Solar Cell (Ⅱ) (Area 14)			

INSTRUCTION FOR SPEAKERS

Oral Presentation:

Time Schedule

	Total session time	Presentation time	Discussion time
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	10 min.	5 min.

BELL: First: Warning, Second: End of speech, Third: End of discussion.

Audio-Visual Equipment

The following equipments are ready at each conference meeting room during SSDM 2010:

* LCD projector
* PC (laptop computer), Windows XP, PowerPoint 2003-2007 and PDF
  The use of personal PCs for presentations is prohibited.
* Microphone
* Projection laser pointer

Uploading your Presentation

The single most important action of the authors is to upload your presentation file to the PC in each session room using your own USB thumb drive. It is the presenter's responsibility to **upload the slide file as soon as possible in each session room at any break** well in advance to the session of presentation. At a short break, the PC may be too crowded to upload the file. If the chairman cannot find your presentation file at the beginning of the session, your presentation will be withdrawn.

In the presentation PC, each presenter's file should be positioned in the folder that corresponds to the session of presentation. The file must be compatible with Microsoft PowerPoint 2007 or Adobe Acrobat 9 on Microsoft Windows. Compatibility can be checked at the Speakers' Room on the third level of Faculty of Engineering Bldg. 2, where the same PCs as in each session room are installed. Details will be informed on SSDM website at http://www.ssdm.jp

Poster Presentation:

Presenting Poster

Poster sessions will be held on Thursday, September 23 from 13:15 to 14:45 on the 5th floor of Takeda Bldg. Poster boards will be available with identifying labels. Authors are requested to prepare their posters between 9:00 and 12:00 on September 23 and remove them by 15:10 on September 23. Any posters remaining after 15:10 will be disposed by the SSDM Secretariat. Usable space on each poster board will be approximately 900 mm wide and 1,500 mm high. Pushpins will be available.

Each presentation will be assigned a board, labeled with the Abstract number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near by their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are required to make 3 minutes short oral presentation on September 23. The presentation time should be kept strictly to 3 minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations be held in a quick, successive sequence. While one speaker is giving his/her presentation, the next speakers should wait nearby in line for their turn in order to move on to the next presentation.

Please note that any absent speakers will be skipped and each presentation will be automatically stopped after 3 minutes have elapsed. Only a PC projector will be made available. You should send your short presentation file to the secretariat (ssdm2010-abs@intergroup.co.jp) by e-mail by before August 24, 2010. Please indicate your paper number and name in the title of your e-mail. The file must be in 3-page landscape PDF format, and the 1st page must indicate your paper title, name of authors and their affiliations only. Because of the limited presentation time, please describe clearly and tersely your research objective and results.

Short oral presentations will be held as follows:

1F Room 211	Area 10
1F Room 212	Area 1
1F Room 213	Area 3
2F Room 221	Area 7
4F Room 241	Area 4
4F Room 242	Area 9, 12
4F Room 243	Area 5
4F Room 244	Area 2, 8
4F Room 245	Area 6
4F Room 246	Area 13
2F Room 222	Area 14
2F Room 223	Area11

Confidentiality:

We will delete all electronic files from the SSDM computers after the presentations are completed. SSDM will not publish or distribute the presentation material.

Agreement not to pre-publish abstracts:

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

EXHIBITION

On the days of the conference SSDM 2010 Exhibition will be held at Forum on the 2nd floor of Faculty of Engineering, Bldg. 2. The show will feature the displays of the latest products of the following exhibitors. Complementary coffee service will be available at Forum during the intermissions of the technical sessions.

Exhibitors

Agilent Technologies International Japan
EIKO
Japanese Society of Applied Physics
JEOL
KEYENCE Japan
NTT Basic Research Laboratories
R-DEC
RSoft Design Group Japan
SILVACO Japan
TNS Systems LLC
(in alphabetical order)

Show dates and hours

Wednesday, September 22 : 9:00 – 15:30
Thursday, September 23 : 8:00 – 18:30
Friday, September 24 : 8:00 – 15:30

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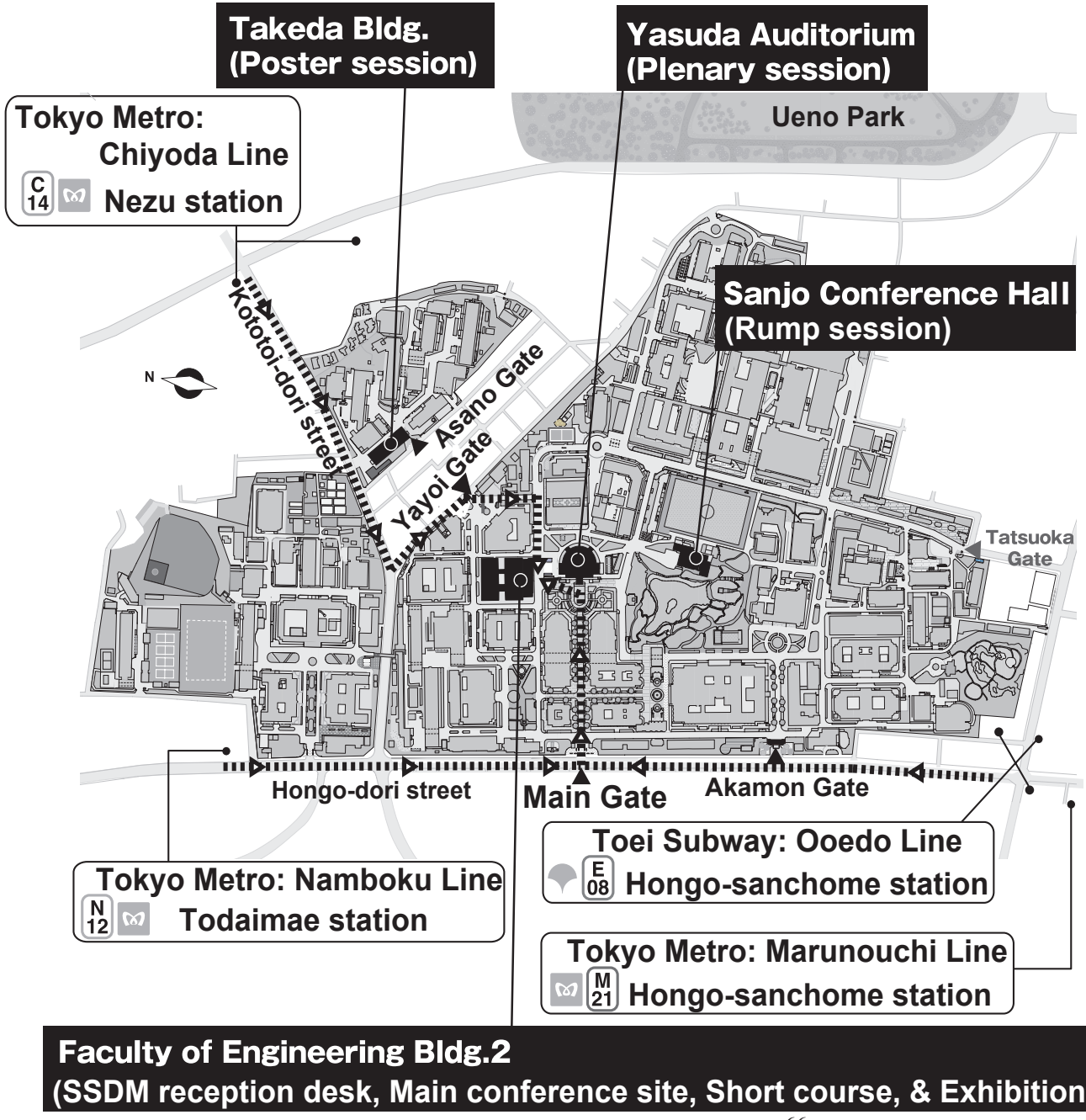
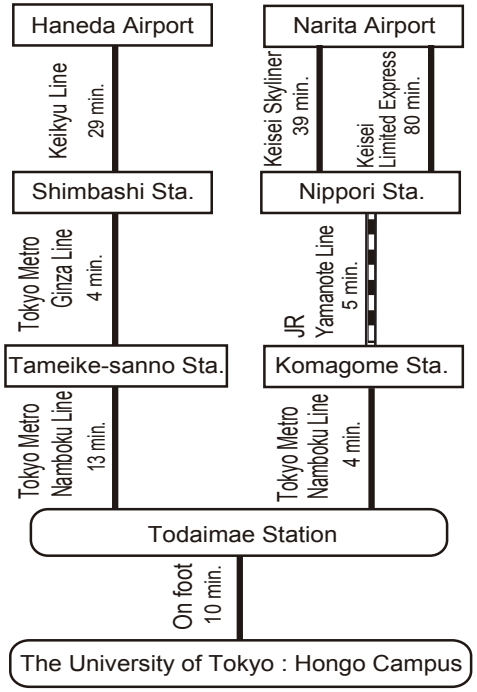


from Airport



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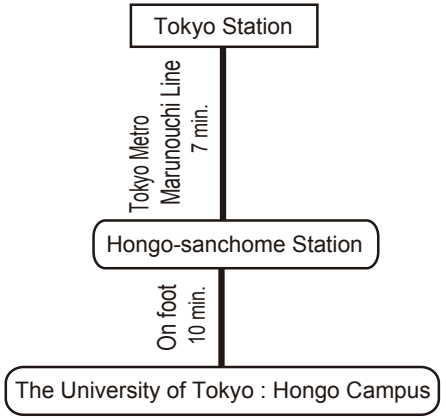
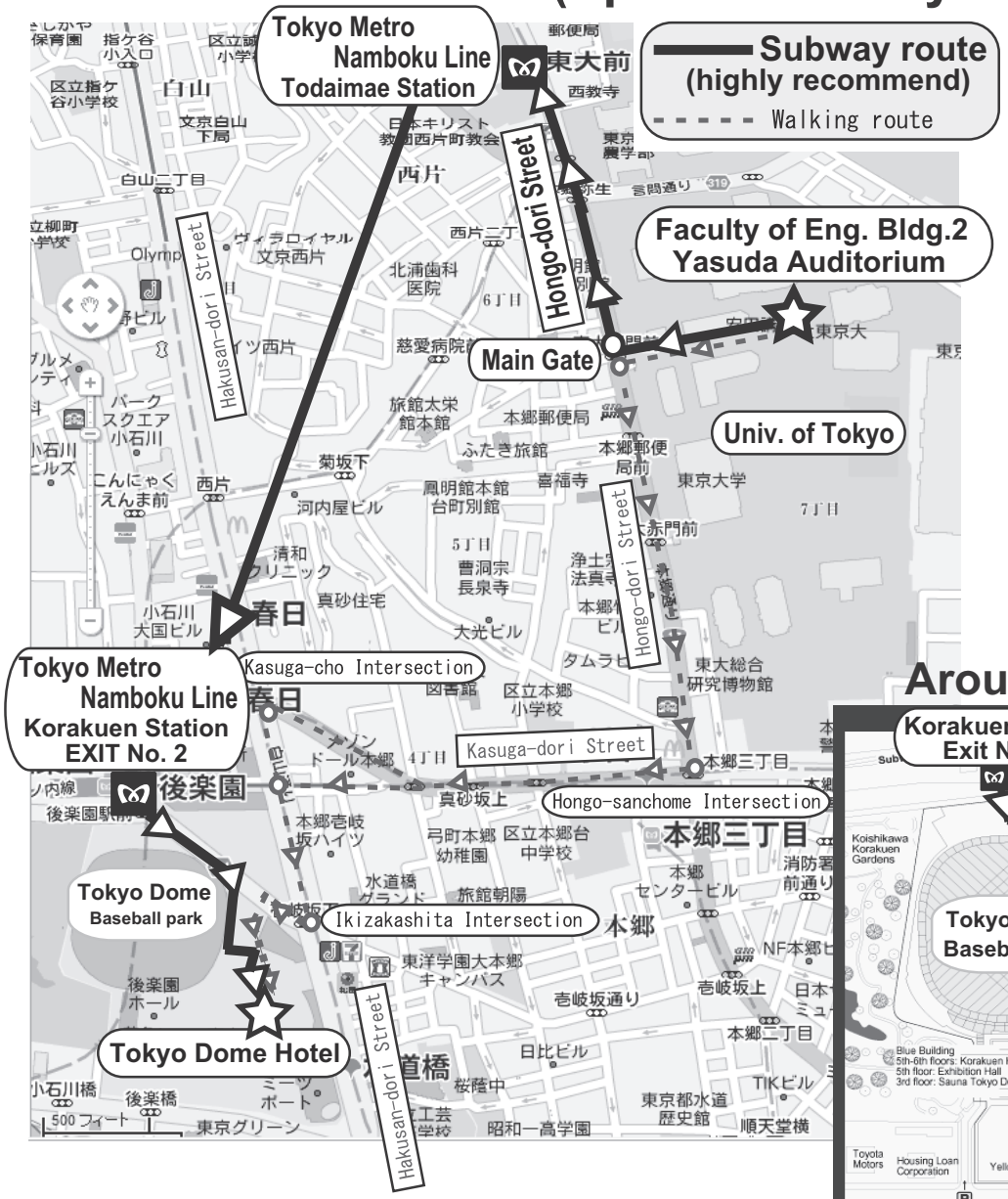
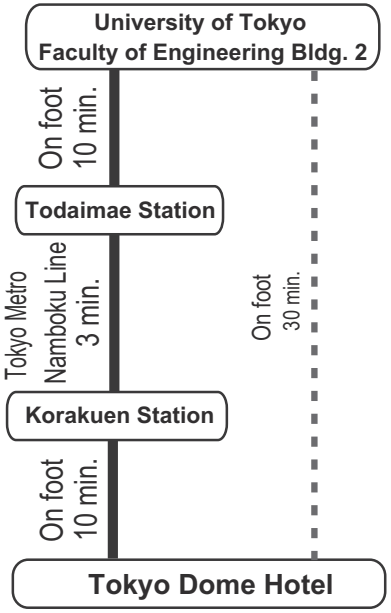


Access to Tokyo Dome Hotel

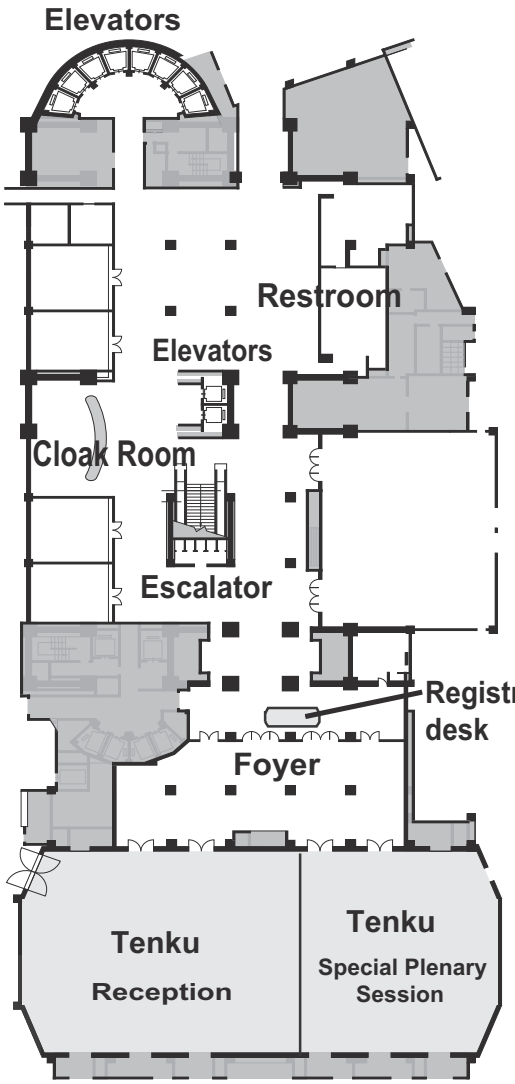
(Special Plenary Session & Reception)



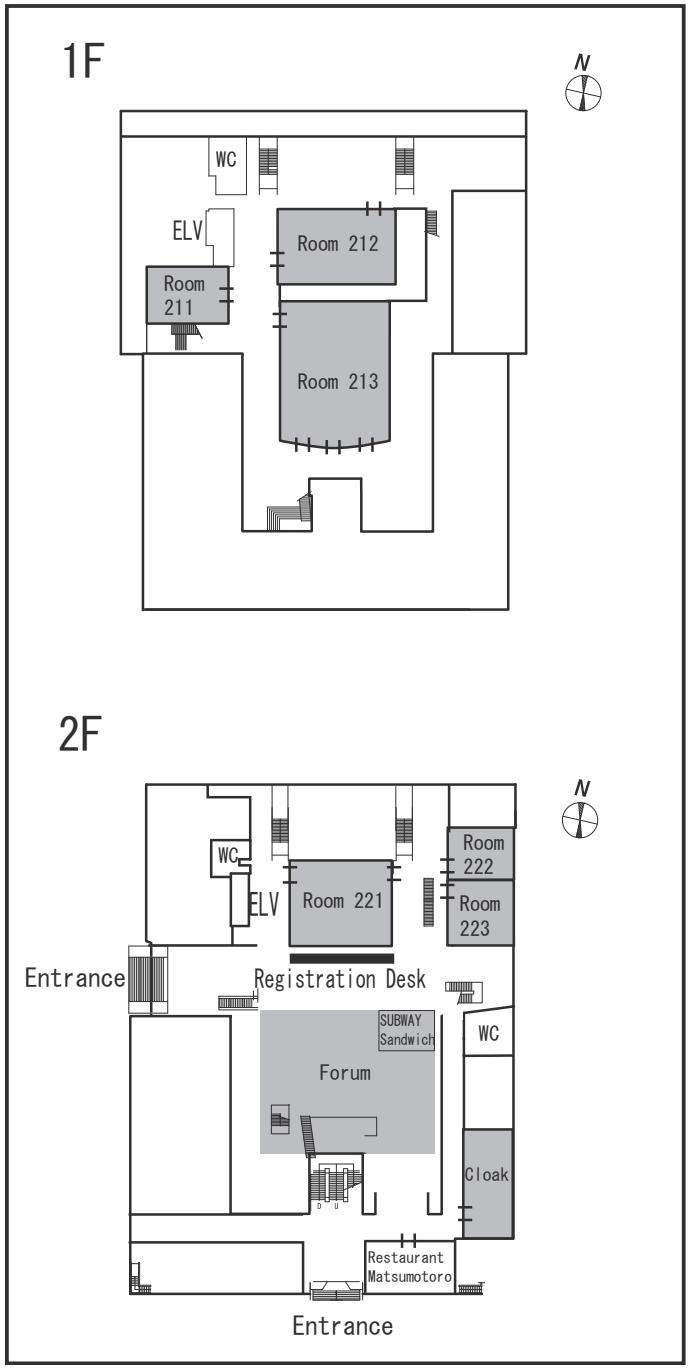


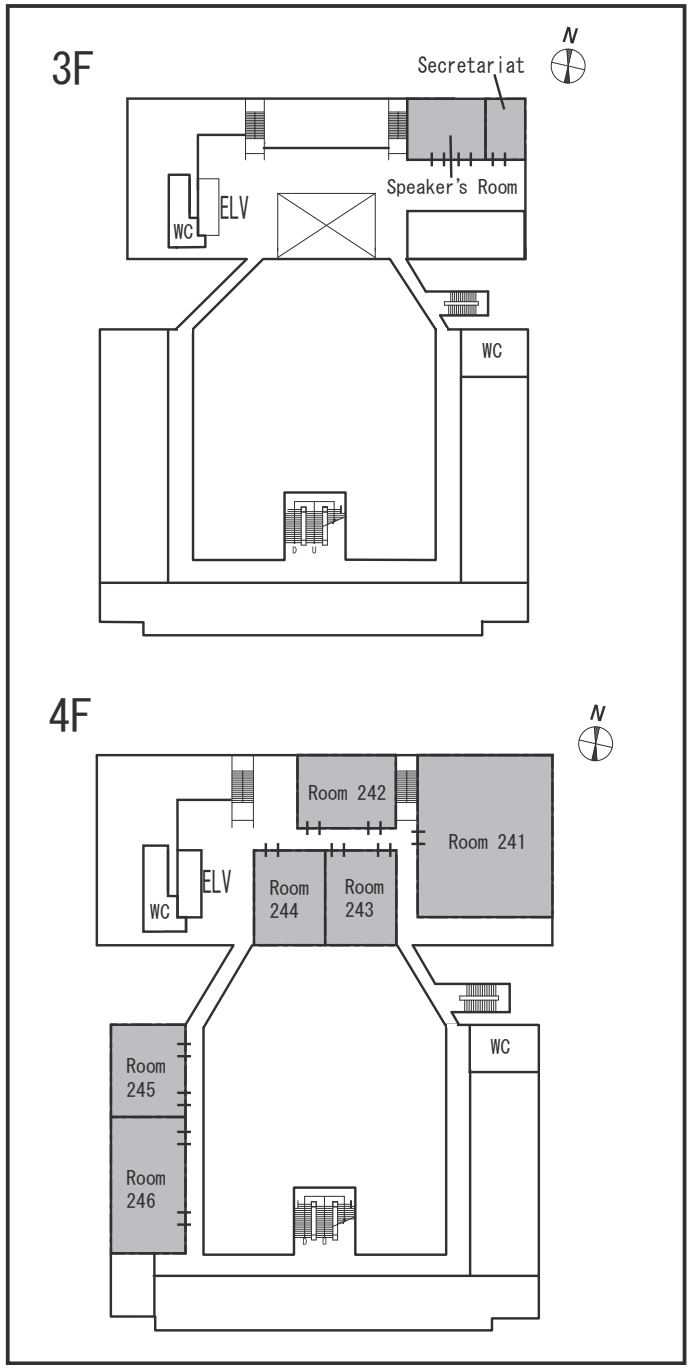
Around Tokyo Dome

B1F Floor



SSDM 2010 Floor Guide, The University of Tokyo, Faculty of Engineering Bldg.2





MEMO

PROGRAM TIME TABLE

Wednesday, September 22					
10:00-12:00 Opening & Plenary Sessions (Yasuda Auditorium)					
1F 211	**1F 212**	**1F 213**	**2F 221**	**4F 241**	**4F 242**
13:00-14:15 Area 10: A-1: Organic Device Physics	**13:00-14:10 Area 1:** B-1: Ge MOS Technology 1	**13:00-14:20 Area 3:** C-1: Low Frequency Noise	**13:00-14:15 Area 7:** D-1: Nonlinear Optics	**13:00-14:20 Area 4:** E-1: DRAM	**13:00-14:15 Area 9:** F-1: Graphene Structures and Transport
14:45-15:45 **Area 10:** A-2: Electric Characterization of Organic Semiconductors	**14:45-16:05** **Area 1:** B-2: Ge MOS Technology 2	**14:45-16:05** **Area 3:** C-2: Transport Physics	**14:45-15:45** **Area 7:** D-2: Advanced Design and Measurement	**14:45-16:05** **Area 4:** E-2: Flash Memory Ⅰ	**14:45-16:00** **Area 9:** F-2: Novel Structures
17:00-18:30 Special Plenary Session (Tokyo Dome Hotel)					
18:30-20:00 Reception (Tokyo Dome Hotel)					
Thursday, September 23					
1F 211	**1F 212**	**1F 213**	**2F 221**	**4F 241**	**4F 242**
9:00-10:30 Area 10: A-3: Organic Light Emitting Diodes	**9:00-10:30 Area 1:** B-3: High-k Gate Stack	**9:00-10:30 Area 3:** C-3: Tunnel & Schottky-S/D FETs	**9:00-10:45 Area 7:** D-3: GaN LED	**9:00-10:50 Area 4:** E-3: Flash Memory Ⅱ	**9:00-10:45 Area 9:** F-3: Spin Manipulation and Photon Detection
11:00-12:15 **Short Presentation** Area 10	**11:00-12:15** **Short Presentation** Area 1	**11:00-12:15** **Short Presentation** Area 3	**11:00-12:15** **Short Presentation** Area 7	**11:00-12:15** **Short Presentation** Area 4	**11:00-12:15** **Short Presentation** Area 9 and Area 12
13:15-14:45 Poster Session (Takeda Bldg.)					
1F 211	**1F 212**	**1F 213**	**2F 221**	**4F 241**	**4F 242**
15:10-16:25 Area 10: A-4: Organic Memory and Related Materials	**15:10-16:20 Area 1:** B-4: Process Integration	**15:10-16:25 Area 3:** C-4: Tr & SRAM Variabilities	**15:10-16:25 Area 7:** D-4: Photonic Crystal Devices	**15:10-16:10 Area 4:** E-4: Flash Memory Ⅲ	**15:10-16:25 Area 9:** F-4: Quantum Dots
16:50-18:05 Area 10: A-5: Organic Electronics and Device Physics	**16:50-18:10 Area 1:** B-5: Advanced Gate Dielectrics	**16:50-18:10 Area 3:** C-5: Si Nanowire Technology	**16:50-18:05 Area 7:** D-5: Quantum Dot	**16:50-17:30 Area 4:** E-5: Flash Memory Ⅳ	**16:50-18:05 Area 9:** F-5: New Functional MOS Structures
18:30-20:00 Rump Session (Sanjyo Conference Hall)					
Friday, September 24					
1F 211	**1F 212**	**1F 213**	**2F 221**	**2F 241**	**2F 242**
9:00-10:45 Area 10: A-6: Organic Transistors and Device Physics Ⅰ	**9:00-10:45 Area 1:** B-6: Junction Technology	**9:00-10:45 Area 3:** C-6: Advanced CMOS Technology	**9:00-10:30 Area 7:** D-6: Photonic and Electronic Integration	**9:00-10:35 Area 4:** E-6: FeRAM	**9:30-10:45 Area 12:** F-6: Spintronics (Ⅰ)- Spin-related Phenomena and Applications -
11:15-12:15 Area 10: A-7: Organic Transistors and Device Physics Ⅱ	**11:15-12:25 Area 1:** B-7: Dopant Characterization	**11:15-12:35 Area 3:** C-7: FinFET Devices	**11:15-12:00 Area 7:** D-7: Nano Photonics	**11:15-12:05 Area 4:** E-7: MRAM	**11:15-12:30 Area 12:** F-7: Spintronics (Ⅱ)- New Applications -
13:30-15:00 Area 10: A-8: Organic Transistors and Device Fabrication Ⅰ		**13:30-15:10 Area 1&3:** C-8: Gate-Insulator Reliability	**13:30-15:15 Area 7:** D-8: Si Photonics (1)	**13:30-15:15 Area 4:** E-8: PRAM/ReRAM	**13:30-15:00 Area 12:** F-8: Spintronics (Ⅲ)- Semiconductors -
15:30-17:15 Area 10: A-9: Organic Transistors and Device Fabrication Ⅱ	**15:30-17:10 Area 1:** B-9: Interface and Strain Characterization	**15:30-17:15 Area 3:** C-9: Emerging Device Technology	**15:30-17:15 Area 7:** D-9: Si Photonics (2)	**15:30-17:15 Area 4:** E-9: ReRAM	**15:30-17:00 Area 12:** F-9: Spintronics (Ⅳ) - Device and Circuits -

Area Scope

Area 1: Advanced Si Processing & Materials Science
Area 2: Advanced Interconnect /3-D Integration Science
Area 3: CMOS Devices / Device Physics
Area 4: Advanced Memory Technology
Area 5: Advanced Circuits and Systems
Area 6: Compound Semiconductor Electron Devices and Related Technologies
Area 7: Photonic Devices and Optoelectronic Integration
Area 8: Advanced Material Synthesis and Crystal Growth Technology
Area 9: Physics and Application of Novel Functional Devices and Materials

PROGRAM TIME TABLE

Wednesday, September 22

10:00-12:00 Opening & Plenary Sessions (Yasuda Auditorium)

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
13:00-14:10 Area 5: G-1: RF Circuits and Systems (1)	**13:00-14:15 Area 8:** H-1: New Functional Materials	**13:00-14:15 Area 6:** I-1: III-V High-Speed and High-Frequency Transistors	**13:00-14:15 Area 13:** J-1: Carbon Nanotube Devices	**13:30-14:00 Area 14:** K-1: Modeling of Power LDMOSFET	**13:00-14:15 Area 11:** L-1: Biosensors
14:45-16:05 Area 5: G-2: RF Circuits and Systems (2)	**14:45-16:00 Area 8:** H-2: Growth of Grapheme for Electronics Applications	**14:45-16:00 Area 6:** I-2: GaN HEMTs	**14:45-16:00 Area 13:** J-2: Carbon Nanotube Properties and Transport	**14:45-15:45 Area 14:** K-2: Power Module Technology	**14:45-16:00 Area 11:** L-2: Silicon Based Biomedical Devices

17:00-18:30 Special Plenary Session (Tokyo Dome Hotel)

18:30-20:00 Reception (Tokyo Dome Hotel)

Thursday, September 23

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
9:00-10:50 Area 5: G-3: Modeling, Variation and Reliability	**9:00-10:30 Area 8:** H-3: Oxides and Nanowires	**9:00-10:30 Area 6:** I-3: III-V Device Technologies	**9:00-10:30 Area 13:** J-3: Graphene Photonics and Electronics	**9:00-10:30 Area 14:** K-3: Compound Power Semiconductor Devices	**9:00-10:30 Area 11:** L-3: Nano Structures and Devices
11:00-12:15 Short Presentation Area 5	**11:00-12:15 Short Presentation** Area 2 and Area 8	**11:00-12:15 Short Presentation** Area 6	**11:00-12:15 Short Presentation** Area 13	**11:00-12:15 Short Presentation** Area 14	**11:00-12:15 Short Presentation** Area 11

13:15-14:45 Poster Session (Takeda Bldg.)

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
15:10-16:25 Area 5: G-4: Advanced Analog Circuits	**15:10-16:20 Area 2:** H-4: Carbon Interconnect	**15:10-16:25 Area 6:** I-4: Silicon Carbide Devices	**15:10-16:25 Area 13:** J-4: Graphene's Electrical Properties	**15:10-16:25 Area 14:** K-4: Next Generation Solar Cells	
16:50-18:05 Area 5&11: G-5: Integrated MEMS/Bio Sensors	**16:50-18:00 Area 2:** H-5: Cu/Low-k Integration	**16:50-17:50 Area 6:** I-5: Oxide Devices	**16:50-18:05 Area 13:** J-5: Graphene Devices	**16:50-18:05 Area 14:** K-5: Compound Semiconductor Solar Cells	

18:30-20:00 Rump Session (Sanjyo Conference Hall)

Friday, September 24

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
9:00-10:45 Area 5&11: G-6: Image Sensors and Interface Circuits	**9:10-10:50 Area 2:** H-6: Cu Reliability	**9:00-10:45 Area 6:** I-6: GaN Power Transistors	**9:00-10:45 Area 13:** J-6: Nanowire Transistors	**9:00-10:45 Area 8:** K-6: Quantum Dots	
11:15-12:30 Area 5: G-7: Data Converter Circuits	**11:15-12:25 Area 2:** H-7: 3D Interconnect	**11:15-12:30 Area 6:** I-7: Processing and Interface Technologies	**11:15-12:15 Area 13:** J-7: Nanowire Growth and Applications	**11:15-12:30 Area 8:** K-7: Growth and Characterization of Nitrides	
13:30-15:00 Area 11: G-8: Bio Nanofusion Technologies	**13:30-14:55 Area 2:** H-8: 3D Integration	**13:30-15:15 Area 14:** I-8: Crystulline and Thin Film Silicon Solar Cell (Ⅰ)		**13:30-15:00 Area 8:** K-8: Si and Ge-based Materials and Devices	
15:30-16:30 Area 11: G-9: Nanomaterial Applications	**15:30-16:25 Area 2:** H-9: Image Sensor	**15:30-16:45 Area 14:** I-9: Crystulline and Thin Film Silicon Solar Cell (Ⅱ)			

Area 10: Organic Materials Science, Device Physics, and Applications
Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)
Area 12: Spintronic Materials and Devices
Area 13: Application of Nanotubes, Nanowires, and Graphene
Area 14: Photovoltaics & Power Semiconductor Devices

2010 International Conference on Solid State Devices and Materials (SSDM 2010)

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