Friday, September 24

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A-6: Organic Transistors and Device Physics Ⅰ (Area 10)

(9:00-10:45)
Chairs: H. Maeda (DNP)
H. Kajii (Osaka Univ.)

9:00 A-6-1 (Invited)
Inkjet Printing of Organic Thin-Film Transistors
T. Kawase, S. Moriya, K. Nakamura, K. Inoue, K. Nakamura and T. Aoki, Seiko Epson Corp. (Japan)
The application of inkjet printing to the fabrication of organic TFT backplanes are reviewed. A hybrid approach in which inkjet printing is combined with photolithography is explained in detail. The phenomena happening in the inkjet printing of semiconductor are also discussed.

9:30 A-6-2
Organic CMOS Logic Papers with In-Field User Customizability
T. Sekitani[1], K. Ishida[1], N. Masunaga[1], R. Takahashi[1], S. Shino[2], U. Zschieschang[3], H. Klauk[3], M. Takamiya[1], T. Sakurai[1] and T. Someya[1], [1]Tokyo Univ. , [2]Mitsubishi Paper Mills Ltd. and [3]Max Planck Inst. for Solid State Research (Japan)
We report the manufacturing of user-customized logic paper—paper in which organic complementary logic cells are embedded. The logic paper provides on-demand in-field customizability to the users by making use of commercially available inkjet printing.

9:45 A-6-3
Effects of an Interface Dipole Monolayer on Pentacene Organic Field-Effect Transistors
W. Ou-Yang, K. Lee, W. Martin, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
Effect of an aligned dipole monolayer with opposite mole-cular orientation on pentacene OFET performance was investigated. We found the monolayer greatly shifted threshold voltage, mobility and on/off ratio and these changes depended on the molecular orientation.

10:00 A-6-4
Organic transistors and circuits with parylene gate dielectric manufactured using subfemtoliter inkjet
T. Yokota, Y. Noguchi, Y. Kato, T. Sekitani and T. Someya, Tokyo Univ. (Japan)
We fabricated organic TFTs and complementary ring oscillator circuits by subfemtoliter inkjet printing. The TFTs have a channel length smaller than 10 μm, a channel width 500 μm, and the 3 μm-linewidth Ag source/drain electrodes.

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B-6: Junction Technology (Area 1)

(9:00-10:45)
Chairs: B. Mizuno (UJT Lab. Inc.)
S. Migita (AIST)

9:00 B-6-1 (Invited)
Overview and Challenges in Source/Drain Formation Technology in High Performance Transistors.
K. Suguro, Toshiba Corp. (Japan)
Source and drain formation technologies which are required in next generation Si devices such as memory LSIs and system LSIs are overviewed and the new challenge for the future are discussed in this paper.

9:30 B-6-2
Raised S/D for Advanced Planar MOSFET devices: Challenges and Applications for the 20nm Node and Beyond
N. Loubet[1], P. Khare[1], S. Mehta[2], S. Ponoth[2], B. Haren[2], Q. Liu[1], K. Cheng[2], J. Kuss[2], T. Adam[2], B. Doris[2], V. Paruchuri[2], W. Kleemeier[1] and R. Sampson[1], [1]STMicroelectronics and [2]IBM (USA)
As transistor physical dimensions continue to scale, RSD epitaxy integration presents new challenges in term of loading effects, facet reproducibility and control. In this paper, the feasibility and integration of flat and faceted RSD silicon epitaxy are investigated.

9:50 B-6-3
Raman Spectroscopy Measurement of Silicidation Induced Stress in Si and its Impact on Performances of Metal Source/Drain MOSFETs
S. Migita, V. Poborchii, T. Tada, Y. Morita, W. Mizubayashi and H. Ota, AIST (Japan)
Silicidation induced stress is examined by Raman spectroscopy. It is found that silicidation induces tensile stress in Si channel, and brings opposite temperature dependences of N-type and P-type metal S/D MOSFETs.

10:10 B-6-4
Accurate Measurement of Silicide Specific Contact Resistivity by Cross Bridge Kelvin Resistor for 28 nm CMOS technology and Beyond
K. Ohuchi, N. Kusunoki and F. Matsuoka, Toshiba America Electronic Components, Inc. (USA)
It is confirmed that specific-contact-resistivity measurement resolution by using modified cross-bridge Kelvin resistor is extended to 10^{-9} Ω-cm^2, and experimentally found 28nm-CMOS-technology realizes $1.1x10^{-8}$ and $7.8x10^{-9}$ Ω-cm^2 for n+ and p+ source/drain, respectively.

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C-6: Advanced CMOS Technology (Area 3)

(9:00-10:45)
Chairs: T. Hase (Renesas Electronics Corp.)
B. Doris (IBM)

9:00 C-6-1 (Invited)
Extremely-Thin SOI for Mainstream CMOS:Challenges and Opportunities
A. Khakifirooz, K. Cheng, A. Kumar, P. Kulkarni, S. Ponoth, B. S. Haran, S. Mehta, J. Cai, A. Byrant, J. Kuss, L. F. Edge, H. Jagannathan, Z. Ren, A. Reznicek, T. Adam, H. He, A. Kimball, S. Kanakasabapathy, S. Schmiz, S. Holmes, A. Majumdar, B. Jagannathan, D. Yang, A. Upham, S. C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, Z. Zhu, L. H,. Vanamurth, J. Faltermeier, S. Fan, D. Horak, T. Hook, V. Narayanan, V. Paruchuri, H. Bu, D. K. Sadana, P. Kozlowsk, B. Doris, D. McHerron, W. Haensch, M. Khare, E. Leobondung, J. O'Neil and G. Shahidi, IBM Research (USA)
Extremely thin SOI (ETSOI) is a viable option for future CMOS scaling owing to superior short-channel control and immunity to random dopant fluctuation. However, challenges of ETSOI integration have so far hindered its adoption for mainstream CMOS. In this talk we review some of these challenges and possible solutions. We will also review some of the unique opportunities offered by ETSOI technology.

9:30 C-6-2
Variability in Variable-Body-Factor Silicon-on-Thin-Box MOSFETs (SOTB MOSFETs)
Y. Yang, G. Du, R. Han and X. Liu, Peking Univ. (China)
A side-gate is used in the variable-body-factor SOTB to adjust the body-factor, which will, however, disturbs the variability performance of the device. In this work, we systematically investigated the influences of LER (line-edge-roughness), WFV (work- function variation) and STV (silicon layer thickness variation) on 20-nm-gate variable-body-factor SOTB MOSFETs.

9:50 C-6-3
Universal Relationship between Settling Time of Floating-Body SOI MOSFETs and the Substrate Current in their Body-Tied Counterparts
A. Toda[1], K. Ohyama[1], N. Higashiguchi[1], D. Hori[1], M. Miyake[1], S. Amakawa[1], J. Ida[2] and M. Miura-Mattausch[1], [1]Hiroshima Univ. and [2]Kanazawa Inst. of Tech. (Japan)
A device-size-independent universal relationship between hysteretic response of floating-body SOI MOSFETs and the dc substrate current in their body-tied counterparts is demonstrated. It could play an important role in compact modeling of history effects.

10:10 C-6-4
Ion-Ioff performance analysis of FDSOI MOSFETs with low processing temperature
C. Xu[1], P. Batude[1], C. Rauer[1], C. Le Royer[1], L. Hutin[1], A. Pouydebasque[1], C. Tabone[1], B. Previtali[1], O. Faynot[1], M. Mouis[2] and M. Vinet[1], [1]CEA-LETI/MINATEC and [2]IMEP (France)
This work demonstrates that Fully-Depleted Silicon On Insulator (FDSOI) transistors processed at low temperature (overall process temperature kept below 600°C) exhibit no strong degradation of the off current as compared to their conventional Rapid Thermal Processing (RTP) counterparts.

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D-6: Photonic and Electronic Integration (Area 7)

(9:00-10:30)
Chairs: N. Iizuka (Toshiba Corp.)
H. Isshiki (The Univ. of Electro-Communications)

9:00 D-6-1 (Invited)
Membrane-Type Photonic Devices for Optical Circuits on SOI
S. Arai and N. Nishiyama, Tokyo Tech (Japan)
Recent research activities on membrane-type photonic devices, such as ultra-low power-consumption semiconductor lasers as well as passive optical devices based on high index-contrast waveguides, aiming at on-chip optical interconnection for next-generation LSIs will be presented.

9:30 D-6-2
Towards Optical Networks-on-Chip Using CMOS Compatible III-V/SOI Technology
L. Grenouillet[1], P. Philippe[1], J. Harduin[1], N. Olivier[1], P. Grosse[1], L. Liu[2,3], T. Spuesens[2], P. Régreny[1], F. Mandorlo[4], P. Rojo-Romeo[4], R. Orobtchouk[4], D. Van Thourhout[2] and J. M. Fedeli[1], [1]CEA-LETI/MINATEC, [2]Ghent Univ., [3]Technical Univ of Denmark and [4]Institut des Nanotechnologies de Lyon INL (FRANCE)
Integrated components for optical networks-on-chip, including III-V microdisk lasers, photodetectors, and wavelength selective circuits, are all demonstrated using a complementary metal-oxide-semiconductor (CMOS) compatible III-V/silicon-on-insulator integration technology at 200mm wafer scale.

9:45 D-6-3
Design and Fabrication of Flip-Chip Micro-LED Arrays with PWM Driver for Heterogeneous Optoelectronic Integrated Circuit Device
S. B. Shin[1], J. Chiba[1], H. Okada[1], S. Iwayama[2] and A. Wakahara[1], [1]Univ. of Toyohashi of Tech. and [2]Stanley Electric Co. Ltd. (Japan)
We designed and fabricated of micro-LED arrays with pulse width modulation(PWM) driver by flip-chip bonding method for research of heterogeneous optoelectronic integrated circuit.

10:00 D-6-4
Monolithic One-bit Counter Circuit with Light Emitting Diode Indicators Fabricated in Si/III-V-N/Si Heterostructure
S. Tanaka, K. Noguchi, K. Yamane, Y. Deguchi, Y. Furukawa, H. Okada, A. Wakahara and H. Yonezu, Toyohashi Univ. of Tech. (Japan)
A monolithic one-bit counter circuit with LED indicators was fabricated, and was successfully operated. The fundamental properties of the circuits as well as the device characteristics were investigated.

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E-6: FeRAM (Area 4)

(9:00-10:35)
Chairs: T. Eshita (Fujitsu Semiconductor Ltd.)
K. Ishihara (Sharp Corp.)

9:00 E-6-1 (Invited)
Current Status and Future Challenge of Fe-NAND/SRAM Cell Technology
K. Takeuchi, Univ. of Tokyo (Japan)
This paper overviews Ferroelectric NAND flash memory and Ferroelectric 6T-SRAM. Fe-NAND enhances SSD performance to 9.5GByte/sec. A 100Million write/erase endurance is realized. A 0.5V ferroelectric 6T-SRAM is proposed which decreases the active power by 32%.

9:30 E-6-2 (Invited)
Current Development Status and Future Challenges of FeRAM
Y. Fujimori, H. Kimura, Y. Ichida, J. Iida, K. Ashikaga, H. Ito, T. Ozawa, T. Kanaya, N. Kinouchi, T. Suzuki, T. Date, D. Notsu, T. Fuchikami, Z. Zhiyong M. Kojima, M. Moriwake and H. Takasu, ROHM Co., Ltd. (Japan)
FeRAM technology on 130nm logic platform is successfully developed. We introduce non-volatile logic for new application. The non-volatile register has wide signal margin and high endurance cycles.

10:00 E-6-3
Synthesis of pure phase BiFeO3 films grown on Iridium electrode by MOCVD for ferroelectric memories
Y. Kumura[1,2], S. Y. Yang[2], P. Yu[2], J. X. Zhang[2], J. Seidel[2], A. I. Khan[2] and R. Ramesh[2], [1]Toshiba Corp. and [2]Univ. of California Berkeley (Japan)
We have successfully demonstrated the feasible synthesis of the pure phase BFO films without voids grown on the submicron-sized Ir electrode by MOCVD using double-layered deposition method for the first time.

10:20 E-6-4 (Late News)
Ferroelectric-Gate Thin-Film Transistor Fabricated by Total Solution Deposition Process
T. Miyasako[1], B. N. Q. Trinh[1], T. Kaneda[1], M. Onoue[1], P. T. Tue[1], E. Tokumitsu[1,2] and T. Shimoda[1,3], [1]JST, [2]Tokyo Tech and [3]JAIST (Japan)
We have fabricated ferroelectric-gate thin film transistors (FGTs) by totally using chemical solution deposition (CSD) process. The fabricated FGT exhibited a typical n-channel memory transistor operation. This is the first demonstration of inorganic thin film transistors (TFTs) fabricated by totally using CSD process for all layers.

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F-6: Spintronics (Ⅰ) - Spin-related Phenomena and Applications (Area 12)-

(9:30-10:45)
Chairs: K. Ito (Hitachi, Ltd.)
H. Saito (AIST)

9:30 F-6-1
Semiconductor / Ferromagnetic Metal Hybrid Optical Isolators using Nonreciprocal Polarization Rotation
H. Shimizu, S. Goto and T. Mori, Tokyo Univ. of Agri. and Tech. (Japan)
We report Fe - InGaAlAs / InP semiconductor - ferromagnetic metal hybrid optical isolators using nonreciprocal polarization rotation. We demonstrated optical isolation of as large as 18.3 dB in 0.85 mm-long waveguide devices.

9:45 F-6-2
Fabrication of MgO-based Magnetic Tunnel Junctions for Magnetic Field Sensor
K. Fujiwara[1], M. Oogane[1], F. Kou[2], H. Naganuma[1] and Y. Ando[1], [1]Tohoku Univ. and [2]RICOH COMPANY,LTD. (Japan)
Magnetic tunnel junctions sensor with an MgO barrier layer were fabricated. The effect of the shape and thickness of the free layer on the magnetic field sensor characteristics was systematically investigated. We achieved a large TMR/2H_k value of 4.8 %/Oe.

10:00 F-6-3
First-Principles Calculations of Quantum Transport Properties of Fe/Fe_2VAl/Fe Trilayers
S. Yabuuchi, I. Kitagawa and T. Hamada, Hitachi, Ltd. (Japan)
We investigated the electronic structure and the quantum transport properties of Fe/Fe_2VAl/Fe trilayer using first-principles calculations. The semimetallic Fe2VAl made it possible to achieve a low resistance area, which is difficult to achieve using a conventional insulator or metal.

10:15 F-6-4
Highly spin-polarized tunneling in Heusler-alloy-based magnetic tunnel junctions with a Co_2MnSi upper electrode and a MgO barrier
H-x Liu, T. Taira, Y. Honda, K. Matsuda, T. Uemura and M. Yamamoto, Hokkaido Univ. (Japan)
High tunnel magnetoresistance ratios of 1049% at 4.2 K and 335% at room temperature were demonstrated for Heusler-alloy-based magnetic tunnel junctions with a Co_2MnSi upper electrode and a MgO barrier. The key factors influencing the spin-dependent tunneling characteristics are discussed.

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G-6: Image Sensors and Interface Circuits (Area 5 & 11)

(9:00-10:45)
Chairs: S. Sugawa (Tohoku Univ.)
J. Akita (Kanazawa Univ.)

9:00 G-6-1 (Invited)
CMOS High–Speed Image Sensors –Pixel Devices, Circuits and Architectures–
S. Kawahito, Shizuoka Univ. (Japan)
CMOS high-speed image sensors are reviewed from the viewpoints of pixel devices and circuit techniques. Possible column-parallel ADC architectures for power-efficient high-speed high-quality imaging and global shutter pixels for low noise are discussed.

9:30 G-6-2
A Column Parallel Cyclic ADC with an Embedded Programmable Gain Amplifier for CMOS Image Sensors
T. Iida, M. A. Mustafa, L. Zhuo, K. Yasutomi, S. Itoh and S. Kawahito, Shizuoka Univ. (Japan)
This paper proposes a column parallel cyclic ADC with an embedded programmable gain amplifier. The measurement results of a prototype chip show the effectiveness of the embedded PGA for the reduction of ADC non-linearity and random noise.

9:50 G-6-3
A CMOS Image Sensor with an Automatic Pixel-Sensitivity Adjustment Function
G. Ramos[1], Y. Hirata[2] and Y. Arima[1], [1]Kyushu Inst. of Tech. and [2]Fukuoka Indus., Sci. and Tech. Foundation (Japan)
We developed an image sensor LSI that automatically adjusts the exposition time for each pixel according to the brightness of its surrounding pixels. The developed sensor LSI uses a 0.35µm CMOS 1-poly 3-metal process and has a die size of 3.75mm × 3.72mm. The power consumption is 267mW.

10:10 G-6-4
A Subnanowatt Vibration-sensing Circuit for Dust-size Battery-less Sensor Nodes
T. Shimamura, H. Morimura, M. Ugajin and S. Mutoh, NTT Microsystem Integration Laboratories (Japan)
The sensing circuit should be ultra-small power on the dust-size sensor node. We propose a vibration-sensing circuit based on mechanical charge transfer. The test chip detects the vibration of sub-hectohertz with subnanowatt power.

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H-6: Cu Reliability (Area 2)

(9:10-10:50)
Chairs: S. Ogawa (AIST)
K. Ito (Kyoto Univ.)

9:10 H-6-1 (Invited)
Cu Alloys and Noble Metal Liner Materials to Extend Damascene Cu Schemes
T. Nogami, IBM (USA)
CVD-Co films characterized (barrier properties and O/C incorporation). PVD-TaN/CVD-Co/PVD-Cu applied to Cu/ULK BEOL to produce reduced post-CMP defectivity and improved EM. However, EM advantage lost when divots due to corrosion formed at trench entrance.

9:40 H-6-2
Migration of Copper through Tungsten-Filled Via on Single Damascene Copper Interconnect
B. M. Kim, J. J. Kim, B. M. Seo, J. S. Oh, J. Y. Cho, J. Lee, K. Hong, B. H. Choi and S. Park, Hynix Semiconductor Inc. (Korea)
A phenomenon of copper migration through tungsten-filled vias, which land on single damascene copper underlayers, was examined. Successful mitigation of this problem was demonstrated through the enhancement of barrier metal or the change of soaking gas from silane to diborane in CVD W deposition process.

10:00 H-6-3 (Invited)
The Effects of Pre-existing Voids on Electromigration Lifetime Scaling
C.V. Thompson, MIT (USA)
Pre-existing voids are common in Cu interconnects. They are also mobile and their dynamics affect reliability scaling in a critical way. Experimental observations and modeling will be reviewed.

10:30 H-6-4
Structure Analyses of Ti-Based Self-Formed Barrier Layers
K. Kohama[1], K. Ito[1], Y. Sonobayashi[1], K. Ohmori[2], K. Mori[2], K. Maekawa[2], Y. Shirai[1] and M. Murakami[3], [1]Kyoto Univ., [2]Renesas Electronics Corp. and [3]The Ritsumeikan Trust (Japan)
Ti-based self-formed barrier layer has enough barrier properties against Cu diffusion into dielectrics. However, the structure and amorphous phases in the barrier layer were not directly identified. We employed an XPS technique with simultaneous Ar etching, to investigate the origin of such high performance of the barrier layer.

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I-6: GaN Power Transistors (Area 6)

(9:00-10:45)
Chairs: E. Y. Chang (National Chiao Tung Univ.)
T. Tanaka (Panasonic Corp.)

9:00 I-6-1 (Invited)
GaN on Si Based Power Devices:A New Era in Power Electronics
M. A. Briere, ACOO Enterprises LLC under contract for International Rectifier (USA)
The commercial introduction of GaN based power devices has opened new possibilities in power electronics. The current status and future prospects for GaN on Si power devices is reviewed, including long term reliability and device stability. Revolutionary advances made possible by these devices in several power electronic applications are discussed.

9:30 I-6-2
Thermally Stable Isolation of AlGaN/GaN Transistors by Using Fe Ion Implantation
H. Umeda, T. Takizawa, Y. Anda, T. Ueda and T. Tanaka, Panasonic Corp. (Japan)
Thermally stable isolation for AlGaN/GaN transistors by Fe ion-implantation is demonstrated. The Fe ions form deep levels after high temperature annealing. This technique enables high breakdown voltages and promising for monolithic integration of GaN devices.

10:00 I-6-4
Reduction of current collapse in AlGaN/GaN HEMTs using thick GaN cap layer
H. Chonan[1], Y. Sakamura[2], G. Piao[2], T. Ide[2], M. Shimizu[2], Y. Yano[3] and H. Nakanishi[1], [1]Tokyo Univ. of Sci., [2]AIST and [3]Taiyo Nippon Sanso Corp. (Japan)
Current collapse suppression using thick GaN cap layer in AlGaN/GaN HEMTs was proposed. Numerical simulations and experimental results show that thick GaN cap layer have effect in reducing carrier trapping in the device semiconductor surface.

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J-6: Nanowire Transistors (Area 13)

(9:00-10:45)
Chairs: S. Uno (Nagoya Univ.)
K. Nishiguchi (NTT Basic Res. Labs.)

9:00 J-6-1 (Invited)
Circuit Implementation of InAs Nanowire FET
W. Prost, K. Blekker, O. Benner and F. J. Tegude, University of Duisburg-Essen (Germany)
We report on the fabrication of InAs nanowire metal-insulator field-effect transistor and their implementation in basic circuits. The position controlled deposition of the InAs nanowires within the pre-patterned circuits on the host substrate is done by the field-assisted fluid self-assembly method.

9:30 J-6-2
Transport Physics of Quasi-Ballistic Nanowire MOSFETs
K. Natori, Tokyo Tech (Japan)
Transport physics of nanoscale MOSFETs is discussed based on characteristics of nanowire MOSFETs. The compact model discloses various new effects.

9:45 J-6-3
Body-biased steep-subthreshold-swing MOS (BS-MOS) with small hysteresis, off current, and drain voltage
K. Nishiguchi and A. Fujiwara, NTT Corp. (Japan)
We demonstrate 30-nm-gate-length nanowire MOSFETs. A parasitic bipolar transistor formed in an SOI channel reduces subthreshold swing below 60 mV/dec at room temperature. Additionally, triple-gate operation allows current characteristics with small hysteresis, high on/off ratio, and low drain voltage.

10:00 J-6-4
Impacts of Diameter-Dependent Annealing in Silicon Nanowire MOSFETs
R. Wang, T. Yu, W. Ding and R. Hung, Peking Univ. (China)
The diameter-dependent annealing effect in silicon nanowire MOSFETs is investigated. The implanted dopants diffuse faster in thin nanowires than those in thick nanowires during annealing process, which results in underestimating the nanowire S/D extension length.

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K-6: Quantum Dots (Area 8)

(9:00-10:45)
Chairs: A. Yamada (Tokyo Tech)
T. Yamaguchi (Ritsumeikan Univ.)

9:00 K-6-1 (Invited)
Quantum Dot Superlattice for High Efficiency Intermediate Band Solar Cell
Y. Okada, Univ. of Tokyo (Japan)
Effciency enhancements exceeding Shockley-Queisser limit of single junction solar cells are possible in an intermediate band solar cell, which incorporates a 3-dimensional quantum dot superlattice in the active region of a p-i-n junction structure. Recent experimental progress on multi-stacked quantum dot solar cells will be reviewed.

9:30 K-6-2
Energy transfer in multi-stacked InAs quantum dots
K. Akahane[1], N. Yamamoto[1], M. Naruse[1,2], T. Kawazoe[2], T. Yatsui[2] and M. Ohtsu[2], [1]Natl. Inst. of Info. & Com. Tech. and [2]Univ. of Tokyo (Japan)
We fabricated a modulated stacked QD structure to investigate energy transfer among QDs. Energy transfer from small QDs to large QDs was clearly observed. Long-range energy transfer can be considered from the measurement of N dependence of PL intensity.

9:45 K-6-3
Enhanced Photoluminescence Properties from Self-Assembled InAs Surface Quantum Dots by Antimony Incorporation
C. H. Chiang, Y. H. Wu, M. C. Hsieh, C. H. Yang, J. F. Wang, Y. C. Chang, L. Chang and J. F. Chen, National Chiao Tung Univ. (Taiwan)
We present a study of surfactant effect from self-assembled InAs surface quantum dots grown on GaAs substrate by incorporating antimony (Sb) into the QD layers with various Sb beam equivalent pressure.

10:00 K-6-4
Structure changes caused by quenching of InAs/GaAs(001) quantum dots
M. Takahasi, JAEA (Japan)
Structures of InAs/GaAs(001) free-standing quantum dots before and after quenching were studied by in situ synchrotron X-ray diffraction. It has been revealed that quenching results in significant structure changes. They take place quickly when the substrate goes through a temperature range in which dislocatd islands are preferably formed.

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A-6: Organic Transistors and Device Physics Ⅰ (Area 10)

10:15 A-6-5
Effects of Gold Nanoparticles on Pentacene Organic Field-effect Transistors
K. Lee[1], W. Ou-Yang[1], M. Weis[2], D. Taguchi[1], T. Manaka[1] and M. Iwamoto[1], [1]Tokyo Tech and [2]Slovak Academy of Sciences (Japan)
By incorporating gold nanoparticles into PVA with different concentrations as nanocomposite gate insulator in pentacene OFET, the carrier behaviour of the devices was studied by considering the carrier injection and transport processes in terms of contact resistance and effective mobility.

10:30 A-6-6 (Late News)
Fabrication of Au electrodes with photopolymerization of triazine dithiol thin films
Y. Sato, R. Ye, K. Ohta and M. Baba, Iwate Univ. (Japan)
we fabricated electrodes of Au thin films on micropattern poly(DT) thin films photopolymerizated through a photomask. This process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.

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B-6: Junction Technology (Area 1)

10:30 B-6-5 (Late News)
Ge Self-Diffusion in Compressively strained Ge Grown on Relaxed $Si_{0.2}Ge_{0.8}$
Y. Kawamura[1], M. Uematsu[1], K Itoh[1], Y. Hoshi[2], K. Sawano[2], Y. Shiraki[2], E. Haller[3] and M. Myronov[4], [1]Keio Univ., [2]Tokyo City Univ., [3]Univ. of California Berkeley and [4]The Univ. of Warwick (Japan)
We present the first measurements of Ge self-diffusion under compressive biaxial strain using $Si_{0.2}Ge_{0.8}$/Ge isotope superlattice/$Si_{0.2}Ge_{0.8}$ heterostructures. Furthermore, we found that Ge self-diffusivities in compressively strained Ge are larger compared to those in relaxed Ge.

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C-6: Advanced CMOS Technology (Area 3)

10:30 C-6-5 (Late News)
Cost Efficient Novel High Performance Analog Devices Integrated with Advanced HKMG Scheme for 28nm CMOS Technology and Beyond
J.-P. Han[1], T. Shimizu[2], L. H. Pan[3], M. Voelker[1], C. Bernicot[4], F. Arnaud[4], A. C. Mocuta[3], K. Stahrenberg[1], A. Azuma[5], G. Yang[5], M. Eller[1], D. Jaeger[1], H. Zhuang[1], K. Miyashita[1], K. Stein[1], D. R. Nair[2], J. H. Park[2], M. Hamaguchi[2], S. Kohler[2], D. Chanemougame[4], W. Li[1], K. Kim[1], N. Kim[6], C. Wiedholz[1], S. Miyake[2], G. Tsutsui[2], H. van Meer[6], J. Liang[6], M. Ostermayr[1], J. Lian[1], M. Celik[1], R. Donaton[3], K. Barla[4], M. H. Na[3], Y. Goto[2], M. Sherony[3], F. Johnson[6], R.Wachnik[3], J. Sudijono[6], E. Kaste[3], R. Sampson[6], J.-H. Ku[1], A. Steegen[3] and W. Neumueller[1], [1]Infineon Technologise, [2]Renesas, [3]IBM Microelectronics, [4]STMicroelectronics, [5]Toshiba America, [6]GLOBALFOUNDRIES and [7]Samsung Electronics (USA)
A comprehensive study of high performance analog (HPA) devices integrated with high-k metal gate has shown that analog properties such as output voltage gain, Gm, Gds, Gm/Id, mismatch behavior, flicker noise, linearity, DC performance (e.g. Ion-Ioff, Ioff-Vtsat, DIBL, Cjswg) as well as reliability of HPA are superior to conventional analog devices

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D-6: Photonic and Electronic Integration (Area 7)

10:15 D-6-5
Monolithic Integration of Ga(NAsP) laser on Si (001) Substrate
S. Liebich[1], M. Zimprich[1], P. Ludewig[1], A. Beyer[1], B. Kunert[2], N. Hossain[3], S. Jin[3], S. J. Sweeney[3], K. Volz[1] and W. Stolz[1], [1]Philipps-Univ. Marburg, [2]NAsP III/V GmbH and [3]Univ. of Surrey (Germany)
Laser structures containing the dilute nitride material Ga(NAsP) can be grown lattice matched on silicon substrates with high crystalline quality and low defect density. Lasing operation from broad area lasers up to 120K is verified.

4F 241

E-6: FeRAM (Area 4)

4F 242

F-6: Spintronics (Ⅰ) - Spin-related Phenomena and Applications (Area 12)-

10:30 F-6-5
Temperature Dependence of Magnetic Damping in Heusler Alloy Thin Films
M. Oogane, S. Mizukami, Y. Kota, T. Kubota, H. Naganuma, A. Sakuma and Y. Ando, Tohoku Univ. (Japan)
The magnetic damping constants and their temperature dependence for the epitaxitially grown $Co_2MnAl_xSi_{1-x}$ and $Co_2Fe_xMn_{1-x}Si$ Heusler alloy films were systematically investigated.

Coffee Break (2F Forum)

1F 211

A-7: Organic Transistors and Device Physics Ⅱ (Area 10)

(11:15-12:15)
Chairs: H. Kajii (Osaka Univ.)
K. Fujita (Kyushu Univ.)

11:15 A-7-1
A Proposal of High Performance and Highly Fabricable Complementary Organic Thin Film Transistor Structure
A. Sugawara, Y. Wada, Y. Ishikawa and T. Toyabe, Toyo Univ. (Japan)
A Complementary Organic Thin Film Transistor (COTFT) structure is proposed, which would make it possible to realize high performance and highly fabricable organic integrated circuits, by using our original OTFT devices simulator, TOTAS.

11:30 A-7-2
Charge modulated reflectance measurement for probing carrier distribution in the pentacene field effect transistor
T. Manaka, S. Kawashima, Y. Tanaka and M. Iwamoto, Tokyo Tech (Japan)
In this presentation, microscopic charge modulated reflectance spectroscopy was conducted to study the injected carrier distribution (n) in pentacene FET. Signal distribution along channel is clearly good agreement with the carrier distribution calculated on the basis of a simple carrier transport model. In combination with the EFISHG mentioned above, each parameters in J=enuE is discriminately evaluated.

1F 212

B-7: Dopant Characterization (Area 1)

(11:15-12:25)
Chairs: Y. Hayami (Fujitsu semiconductor Ltd.)
B. Mizuno (UJT Lab. Inc.)

11:15 B-7-1 (Invited)
Dopant/carrier profiling in nanostructures.
W. Vandervorst[1,2], P. Eyben[1], A. Schulze[1,2], J. Mody[1,2], S. Koelling[1,2], A. Kambham[1,2] and M. Gilbert[1], [1]IMEC and [2]Instituut voor Kern- en Stralingsfysica (Belgium)
Compositional and electrical analysis of nanostructures involves extreme requirements ranging from “simple” 1D-depth resolution problems to metrology with high 2D-spatial resolution to the need to probe in an extremely small confined volume and 3D-devices. In this presentation we present an overview of the recent evolution in 1D, 2D, and 3D analysis.

11:45 B-7-2
Hole generation in B-implanted Ge without annealing: Formation of B_{12} cluster acting as a double acceptor
M. Koike and Y. Kamimuta, MIRAI-Toshiba (Japan)
We present hole generation (max: 8x10^20 cm^-3) in B-implanted Ge without annealing. The activation ratio in the wide range of impurity concentrations ($10^{16\text{-}22}$ cm^{-3}) is almost the same value of 1/6. These results can be explained by assuming B12 cluster formation as a double acceptor in the as-implanted Ge.

1F 213

C-7: FinFET Devices (Area 3)

(11:15-12:35)
Chairs: S. Hayashi (Panasonic Corp.)
K. Okano (Toshiba Corp.)

11:15 C-7-1
Experimental Study of PVD-TiN Gate with Poly-Si Capping and Its Application to 20 nm FinFET Fabrication
T. Kamei[1], Y. X. Liu[2], K. Endo[2], S. O'uchi[2], J. Tsukada[2], H. Yamauchi[2], Y. Ishikawa[2], T. Hayashida[1], T. Matsukawa[2], K. Sakamoto[2], A. Ogura[1] and M. Masahara[2], [1]Meiji Univ. and [2]AIST (Japan)
We have investigated threshold voltage (Vth) variability and mobility of n+-poly-Si and PVD-TiN gate FinFETs. Thin PDV-TiN with n+-poly-Si capping is very effective to set a symmetrical Vth for FinFETs without mobility degradations.

11:35 C-7-2
High-k Metal Gate FinFET SRAM Cell Optimization Considering Variability due to NBTI/PBTI and Surface Orientation
V. P. H. Hu, M. L. Fan, C. Y. Hsieh, P. Su and C. T. Chuang, National Chiao Tung Univ. (Taiwan)
This paper analyzes the impact of intrinsic process variation and NBTI/PBTI induced time-dependent variations on the stability/variability of 6T high-k metal gate FinFET SRAM cells with various surface orientations. Variability comparisons for FinFET SRAM cells with different gate stacks (SiO2 and SiO2/HfO2) are also examined.

2F 221

D-7: Nano Photonics (Area 7)

(11:15-12:00)
Chairs: M. Tokushima (AIST)
S. Saito (Hitachi, Ltd.)

11:15 D-7-1
InGaAs Nano-Photodiode enhanced by Polarization-Insensitive Surface-Plasmon Antenna
D. Okamoto, J. Fujikata and K. Ohashi, NEC Corp. (Japan)
We developed an InGaAs nano-photodiode incorporated with a polarization-insensitive ring-type surface-plasmon antenna consisting of gold-based concentric-ring gratings. The antenna enables high quantum efficiency of 80% for any polarization of incident light and wider wavelength bandwidth.

11:30 D-7-2
Metallic Nano-Slit Array Lens for Spatial Resolution Improvement of In-vivo CMOS image sensor
K. Sasagawa[1,2], T. Noda, T. Tokuda, M. S. Islam[3] and J. Ohta[1,2], [1]NAIST, [2]JST-CREST and [3]Univ. of California at Davis (Japan)
We proposed a metallic nano-slit array lens for implantable in-vivo CMOS image sensor. And the electromagnetic fields were simulated by FDTD method. The results show that the incident angle is limited and the spatial resolution is improved by the structure.

4F 241

E-7: MRAM (Area 4)

(11:15-12:05)
Chairs: S. Miura (NEC Corp.)
T. Eshita (Fujitsu Semiconductor Ltd.)

11:15 E-7-1 (Invited)
Current Status and Future Challenge of Embedded High-speed MRAM
S. Fukami, T. Suzuki, K. Nagahara, N. Ohshima, S. Saitoh, R. Nebashi, N. Sakimura, H. Honjo, K. Mori, E. Kariyada, Y. Kato, K. Suemitsu, H. Tanigawa, K. Kinoshita, S. Miura, N. Ishiwata and T. Sugibayashi, NEC Corp. (Japan)
The DW-motion MRAM with 2T1MTJ cell structure has been developed. We confirmed its potential to replace conventional embedded memories. Our technology will enable zero standby power consumption SoCs.

11:45 E-7-2
Phenomenological model for stress and relaxation processes of resistance drift in magnetic tunnel junctions
Y. Kamakura, S. Nakano and K. Taniguchi, Osaka Univ. (Japan)
A phenomenological model for stress and relaxation processes of resistance drift in AlOx based MTJs is proposed. By using the rheological approach, the model can well reproduce the characteristics observed in various pulsed stress experiments.

4F 242

F-7: Spintronics (Ⅱ) - New Applications - (Area 12)

(11:15-12:30)
Chairs: Y. Ohno (Tohoku Univ.)
K. Ito (Hitachi, Ltd.)

11:15 F-7-1 (Invited)
Three-Terminal Spin-Momentum-Transfer Magnetic Memory Element
M. Gaidis, J. Sun, E. O'Sullivan, G. Hu, J. DeBrosse, J. Nowak, D. Abraham and P. Trouilloud, IBM (USA)
SMT MRAM has potential as a nonvolatile memory with speed, density, endurance, and scaling. One can improve performance by separating the reading and writing functions of the device, adding a third terminal to the standard two-terminal device. We present the design and fabrication of the device, and high speed test results showing 1ns switching.

11:45 F-7-2 (Invited)
Spin dice: Random Number Generator using Current-induced Magnetization Switching in MgO-MTJs
A. Fukushima, T. Seki, K. Yakushiji, H. Kubota, S. Yuasa and K. Ando, AIST (Japan)
We propose a new type of physical random number generator based on the current induced magnetization switchings in MgO-MTJs, named spin dice. Random numbers are generated by the probabilistic characteristic of the switchings. We fabricate spin dice in a circuit board style, and generate the random numbers at 500 kbit/sec.

Friday, September 24

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-6: Image Sensors and Interface Circuits (Area 5 & 11)	**H-6: Cu Reliability (Area 2)**	**I-6: GaN Power Transistors (Area 6)**	**J-6: Nanowire Transistors (Area 13)**	**K-6: Quantum Dots (Area 8).)**	
10:30 G-6-5 (Late News) **A SPICE-based Multi-physics Seamless Simulation Platform for CMOS-MEMS** *T. Konishi[1], S. Maruyama[2], T. Matsushima[1], M. Mita[3], K. Machida[1,4], N. Ishihara[4], K. Masu[4], H. Fujita[2] and H. Toshiyoshi[2], [1]NTT Advanced Technology Corp., [2]Univ. of Tokyo, [3]JAXA and [4]Tokyo Tech (Japan)* We report a SPICE version of such multi-physics solver that is capable of microelectromechanical transient analysis, AC harmonic analysis, and electro-mechanical mixed-signal simulation that can be performed seamlessly with the LSI simulation.		**10:15 I-6-5** **Reduced contact resistance and Improved surface morphology for Ohmic Contacts on AlGaN/GaN based Semiconductors employing KrF Laser Irradiation** *G. H. Wang[1], T. Sudhiranjan[1], X. Wang[2], H. Y. Zheng[2], T. K. Chan[3], T. Osipowicz[3] and Y. L. Foo[1], [1]Inst. of Materials Res. And Eng., [2]Singapore Inst. Of Manufacturing Tech. and [3]National Univ. of Singapore (Singapore)* We employ excimer laser annealing for ohmic contact formation to n or p type GaN. Laser annealing achieved reduced sheet resistance in the contact formed, essential for high performance GaN light emitting diodes (LEDs) and heterostructure field-effect transistors applications. Forward current in LEDs increased due to the reduced contact resistance.	**10:15 J-6-5** **Single-electron transport through a Germanium-Nanowire Quantum Dot** *S. K. Shin[1,2], S. Huang[1], N. Fukata[3] and K. Ishibashi[1,2], [1]RIKEN, [2]Tokyo Inst. of Tech. and [3]National Inst. for Materials Sci. (Japan)* Single-electron transistors using an n-type GeNW were fabricated. Pronounced Coulomb peaks with the equidistant spacing in Vg were observed. While the Coulomb peak heights were varied very much, the dimensions of Coulomb diamonds were identical.	**10:15 K-6-5** **High-temperature phosphorous passivation of Si surface for improved heteroepitaxial growth of InAs as an initial step of III-As MOVPE on Si** *M. Deura, Y. Kondo, M. Takenaka, S. Takagi, Y. Shimogaki, Y. Nakano and M. Sugiyama, Univ. of Tokyo (Japan)* We investigated the annealing effect on InAs growth, annealed in group-V gas ambient at much higher temperature than that during growth and the protection effect of group-V atoms during annealing in terms of surface contamination.	
		10:30 I-6-6 **Nonequilibrium Carrier Transport Observed in Pnp AlGaN/GaN HBTs** *K. Kumakura and T. Makimoto, NTT Corp. (Japan)* We found nonequilibrium carrier transports in the nitride-based HBTs. They were ascribed to the high energy carrier injection into the base, and also to the carrier drift motion induced by the electric field inside the base.	**10:30 J-6-6** **A Theoretical Study of Electron Wave Function Penetration Effects on Electron-Modulated-Acoustic-Phonon Interactions in Silicon Nanowire MOSFETs** *J. Hattori[1,3], S. Uno[1,3], N. Mori[2,3] and K. Nakazato[1], [1]Nagoya Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)* We have theoretically studied the interaction between electrons and modulated acoustic phonons in gate biased silicon nanowires with taking into account electron wave function penetration into the oxide layer.	**10:30 K-6-6** **Growth of InAs Quantum Dots with Various Charged States on a Wafer Utilizing Concentric Distribution** *N. Kumagai[1], S. Ohkouchi[1], M. Shirane[1,2], Y. Igarashi[1,2], M. Nomura[1], Y. Ota[1], S. Yorozu[1,2], S. Iwamoto[1] and Y. Arakawa[1], [1]Univ. of Tokyo and [2]NEC Corp. (Japan)* Using concentric distribution of QD density on a wafer, we obtain a series of QDs with charged excitonic states from positive to negative via neutral states at a time. As a result, we succeed in growth of InAs QDs with selectively charged states on a same wafer by only Si doping.	

Coffee Break (2F Forum)

G-7: Data Converter Circuits (Area 5) (11:15-12:30) Chairs: M. Horiguchi (Renesas Electronics. Corp.) T. Koide (Hiroshima Univ.)	**H-7: 3D Interconnect (Area 2)** (11:15-12:25) Chairs: J. Gambino (IBM) J. Kodate (NTT)	**I-7: Processing and Interface Technologies (Area 6)** (11:15-12:30) Chairs: K. S. Seo (Seoul National Univ.) K. Kumakura (NTT Corp.)	**J-7: Nanowire Growth and Applications (Area 13)** (11:15-12:30) Chairs: N. Aoki (Chiba Univ.) K. Tateno (NTT Corp.)	**K-7: Growth and Characterization of Nitrides (Area 8)** (11:15-12:30) Chairs: T. Iwai (Fujitsu Labs. Ltd.) M. Takahashi (JAEA)	
11:15 G-7-1 **Qpix v.1: A high speed 400-pixels readout LSI with 10-bit 10MSps pixel ADCs** *F. Li, V. M. Khoa, M. Miyahara and A. Matsuzawa, Tokyo Tech (Japan)* Qpix v.1 has been developed to realize large area applications and to increase the basic performance. It possesses 400 pixels and compact readout structure to guarantee that all stored data in the pixels can be read out in 2.6 µs in parallel mode and 54 µs in serial mode.	**11:15 H-7-1 (Invited)** **3D Integration Technology and 3D System-on- a Chip** *M. Koyanagi, Tohoku Univ. (Japan)* A 3D super-chip integration technology using the reconfigured wafer-to-wafer bonding and multichip-to-wafer bonding is presented. In addition, new 3D-SoCs such as a 3D microprocessor, 3D-stacked image processor and 3D dependable SoC are discussed.	**11:15 I-7-1** **Deep level characterization of MOVPE-grown AlGaN with high Al compositions** *S. Okuzaki[1], K. Sugawara[1], H. Taketomi[2], H. Miyake[2], K. Hiramatsu[2] and T. Hashizume[1], [1]Hokkaido Univ. and [2]Mie Univ. (Japan)* We investigate Schottky interface properties and deep levels of $Al_xGa_{1-x}N$ with a wide range of Al composition ($0.25<x<0.60$) by using X-ray photoelectron spectroscopy (XPS), I-V, C-V, and deep level transient spectroscopy (DLTS).	**11:15 J-7-1** **Al-doped Zinc Oxide Field Emitter Array Controlled by High-Voltage Poly-Si Thin Film Transistor** *P. Y. Yang[1], J. L. Wang[2], W. C. Tsai[3], S. J. Wang[3], J. C. Lin[4], I. C. Lee[1], C. T. Chang[1] and H. C. Cheng[1], [1]National Chiao Tung Univ., [2]Ming Chi Univ. of Technology, [3]National Cheng Kung Univ. and [4]St. John's Univ. (Taiwan)* The hydrothermally grown Al-doped ZnO nanowires were controlled by high-voltage poly-Si thin film transistor to improve the anode current stability of field emitter.	**11:15 K-7-1 (Invited)** **Droplet elimination process by radical beam irradiation for the growth of InN-based III-nitrides and its application to device structure** *T. Yamaguchi and Y, Nanishi, [1]Ritsumeikan Univ. and [2]Seoul National Univ. (Japan)* A new method, named droplet elimination by radical beam irradiation (DERI), is proposed for the reproducible growth of high-quality InN. This method is also applied to the growth of Mg-doped InN and undoped InGaN toward the application to device structure.	
11:35 G-7-2 **A 0.5V 1.4mW 750MHz 10b CMOS Current Steering DAC** *N. Shimasaki, R. Ito, M. Miyahara and A. Matsuzawa, Tokyo Tech (Japan)* An ultra-low voltage and power of 0.5 V and 1.4 mW, yet high speed of 750 MHz CMOS 10 bit current DAC has been developed using digital feedback technique and forward body biasing.	**11:45 H-7-2** **Evaluation of Copper Diffusion in Thinned Wafer with Extrinsic Gettering for 3D-LSI by Capacitance-Time(C-t) measurement"** *J. C. Bea, K. W. Lee, M. Murugesan, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)* The effects of extrinsic gettering(EG) layers formed on p/p- wafers and p/p+ wafers by backside grinding and the following chemical mechanical polishing(CMP), dry polishing(DP) and ultra-poligrind(UPG) methods against metallic contamination induced has been investigated.	**11:30 I-7-2** **Direct Liquid Cooling Technology for Power Semiconductor Devices** *N. Otsuka, S. Nagai, M. Yanagihara, Y. Uemoto and D. Ueda, Panasonic Corp. (Japan)* We first demonstrate the reduction of junction temperatures in direct liquid cooling (DLC) of GaN power devices for high power and high voltage switching applications. In the DLC structure, junction temperature reductions of up to 55K or 100% higher power levels were demonstrated, and the thermal resistance was reduced as much as 32%.	**11:30 J-7-2** **Nanoarchitecture Light Emitting Diode Microarrays Using Position-Controlled GaN/ZnO Coaxial Nanotube Heterostructures** *C. H. Lee[1,2], J. Yoo[1,2], Y. J. Hong[1,2], J. Cho[1], Y. J. Kim[1,2], S. R. Jeon[3], J. H. Baek[3] and G. C. Yi[1], [1]Seoul National Univ., [2]POSTECH and [3]Korea Photonics Tech. Inst. (Korea)* We studied the fabrication and electroluminescent characteristics of GaN-based nanoarchitecture light emitting diode (LED) microarrays consisting of position-controlled GaN/ZnO coaxial nanotube heterostructures. The nanoarchitecture LEDs exhibited strong green and blue emission from the GaN/GaN/$In_{1-x}Ga_xN$ multi-quantum wells at room temperature.	**11:45 K-7-2** **Reduction of S-parameter by the Introduction of Nitrogen in GaNAs: Positron Annihilation and Its Comparative Study with Photoluminescence Spectroscopy** *H. Nakamoto[1], F. Ishikawa[1], M. Kondow[1], Y. Ohshima[1], A. Yabuchi[1], M. Mizuno[1], H. Araki[1] and Y. Shirai[2], [1]Osaka Univ. and [2]Kyoto Univ. (Japan)* The introduction of nitrogen into GaNAs reduces S-parameter compared to GaAs and that was further lowered by annealing. That suggests the possibility of correlation between carrier localization and the positron annihilation process.	

Friday, September 24

1F 211

A-7: Organic Transistors and Device Physics Ⅱ (Area 10)

11:45 A-7-3
Bias-temperature-instability and thermal anneal effects of organic thin-film transistors
P. H. Chen[1], P. Y. Lo[1,2], T. S. Hu[2] and P. W. Li[1], [1]National Central Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
Top-gate organic thin film transistors were fabricated and characterized in a temperature range of 300-370 K. In addition to thermally activated charge trapping and ion drift mechanisms, the trap numbers elimination at the P3HT/PVP and the dopant deactivation or bipolaron formation in P3HT are also possible origin for OTFTs instability.

12:00 A-7-4
Transport Mechanism at the First-layered Pentacene Grains and Grain Boundaries
Y. Hu[1,2], L. Wang[1], Q. Qi[1] and C. Jiang[1], [1]National Center for Nanoscience and Tech. and [2]Chinese Academy of Sci. (China)
We have performed both experimental and theoretical researches of transport mechanism in first layer grains and grain boundaries of the pentacene films and found that the grain boundary model is valid both in grain size dependent and temperature dependent mobility experiments.

1F 212

B-7: Dopant Characterization (Area 1)

12:05 B-7-3
Contribution of Carbon to Growth of Boron-Containing Cluster in Heavily B-doped Silicon
H. Itokawa[1,2], A. Ohta[2], M. Ikeda[2], I. Mizushima[1] and S. Miyazaki[2], [1]Toshiba Corp. and [2]Hiroshima Univ. (Japan)
It is well-known that substitutional C atoms can capture excess self-interstitial Si atoms and suppress the diffusion of ion-implanted intersitial-type dopants such as B in Si. In the case of B concentration as much as ~1 x 10^{21} cm^{-3}, the B activation ratio in Si is decreased with C incorporation.

1F 213

C-7: FinFET Devices (Area 3)

11:55 C-7-3
Advantage of Plasma Doping for Source/Drain Extension in Bulk-FinFET
T. Izumida, K. Okano, T. Kanemura, M. Kondo, S. Inaba, S. Itoh, N. Aoki and Y. Toyoshima, Toshiba Corp. (Japan)
We demonstrate the efficiency of plasma doping on the fabrication of a bulk-FinFET, showing detailed boron distributions in a narrow fin region analyzed by atom-probe tomography and SIMS, and device characteristics calculated by 3D simulations.

12:15 C-7-4
FinFETs Junctions Optimization by Conventional Ion Implantation for (Sub-)22nm Technology Nodes Circuit Applications
A. Veloso, A. De Keersgieter, S. Brus, N. Horiguchi, P. P. Absil and T. Hoffmann, IMEC (Belgium)
This work demonstrates a junctions formation methodology for aggressively scaled FinFET devices, using conventional ion implantation, and compatible with dense pitches applications, without penalty in RSD nor device performance, and yielding higher SRAM SNM values.

2F 221

D-7: Nano Photonics (Area 7)

11:45 D-7-3
Enhanced Sensitivity of SOI Photodiode by Au Nanoparticles
Y. Matsuo, A. Ono, H. Satoh and H. Inokawa, Shizuoka Univ. (Japan)
We demonstrated the enhancement of the quantum efficiency of SOI photodiode with Au nanparticles. The en-hancement mechanism is explained by the increment of the effective path in SOI due to the scattering and the multiple reflections.

4F 241

E-7: MRAM (Area 4)

4F 242

F-7: Spintronics (Ⅱ) - New Applications - (Area 12)

12:15 F-7-3
High-speed MRAM Random Number Generator using Error-Correcting Code
T. Tetsufumi, N. Shimomura, S. Ikegawa, M. Matsumoto, S. Fujita and H. Yoda, Toshiba Corp. (Japan)
A high speed random number generator (RNG) circuits based on magnetoresistive-random-access-memory (MRAM) using error-correcting coding (ECC) post-processing circuits is presented. It is shown that this post-processing block can be shared with conventional memory ECC block and powerfully improves the quality of randomness with minimum overhead.

12:30-13:30 Lunch

1F 211

A-8: Organic Transistors and Device Fabrication Ⅰ (Area 10)

(13:30-15:00)
Chairs: H. Usui (Tokyo Univ. of Agri. & Tech.)
M. Yoshida (AIST)

13:30 A-8-1 (Invited)
Materials and Processes for Air-Stable n-Channel Organic Transistors
J. H. Oh[1,2] and Z. Bao[1], [1]Stanford Univ. and [2]UNIST (USA)
Recently, there has been a remarkable progress in the molecular design, device performance and stability for n-channel OTFTs. Herein we report recent progress in materials design and processes for high-performance air-stable n-channel OTFTs, mainly focusing on the development of most-commonly used n-channel semiconductors, i.e., perylene diimide (PDI) and naphthalene diimide (NDI) derivatives.

1F 213

C-8: Gate-Insulator Reliability (Area 1) & (Area 3)

(13:30-15:10)
Chairs: B. Doris (IBM)
B. H. Lee (GIST)

13:30 C-8-1
Using Power Transform to Study DC and AC CHC Effects on nMOSFETs in 65 nm Technology
S. Y. Chen[1], C. H. Tu[1], M. X. Wu[1], H. S. Huang[1], Z. W. Jhou[2], S. Chou[2] and J. Ko[2], [1]National Taipei Univ. of Tech. and [2]United Microelectronics Corp. (Taiwan)
For the first time, this article is to use power transform to describe nMOSFET degradation due to DC and AC CHC stress. The power transform model is a function of voltage (V_d, V_g-V_t), current (I_d, I_g), and temperature (T). All the results show that the power transform model can well fit the experimental data of DC and AC CHC stress.

2F 221

D-8: Si Photonics (1) (Area 7)

(13:30-15:15)
Chairs: H. Isshiki (The Univ. of Electro-Communications)
N. Iizuka (Toshiba Corp.)

13:30 D-8-1 (Invited)
Nanophotonic On-Chip Interconnection Networks for Energy-Performance Optimized Computing
A. Biberman and K. Bergman, Columbia Univ. (USA)
Much recent progress in silicon nanophotonic technology has enabled the prospect of high-performance nanophotonic networks-on-chip (NoCs), which have become very attractive solutions to the growing bandwidth and power consumption challenges of future high-performance chip multiprocessors.

4F 241

E-8: PRAM/ReRAM (Area 4)

(13:30-15:15)
Chairs: Y. C. Chen (Macronix International Co., Ltd.)
M. Moniwa (Renesas Electronics Corp.)

13:30 E-8-1 (Invited)
A Survey of Cross Point Phase Change Memory Technologies
D. Kau, Intel Corp. (USA)
Among the recent advances in phase change memory and the integrated selector, stackable thin-film cross point memory delivers the densest array, therefore the most compact die size. Combining its attributes in cost, performance and reliability, cross point phase change technologies stimulate potential opportunities in computing memory hierarchy.

4F 242

F-8: Spintronics (Ⅲ) - Semiconductors - (Area 12)

(13:30-15:00)
Chairs: M. Yamamoto (Hokkaido Univ.)
S. Kuroda (Univ. of Tsukuba)

13:30 F-8-1 (Invited)
Magnetic anisotropy of GaMnAs and its application for multi-valued memory device
S. Lee[1], T. Yoo[1], S. Khym[1], H. Lee[1], S. Lee[1], S. Kim[1], J. Shin[1], X. Liu[2] and J. K. Furdyna[2], [1]Korea Univ. and [2]Univ. of Notre Dame (Korea)
We present interesting magnetic anisotropy properties and realization of four resistance states in single layer of GaMnAs film. We demonstrate such four resistance sates can be used for a quaternary memory device.

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G-7: Data Converter Circuits (Area 5)

11:55 G-7-3
Low-Complexity Time-Domain Winner-Take-All Circuit with High Time-Difference Resolution Limited only by With-In-Die Variation
M. Yasuda, T. Ansari, W. Imafuku, A. Kawabata, T. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
The time-domain Winner-Take-All (WTA) circuit detects the first arriving signal and determines the winner. In this paper, a time-domain WTA circuit with high time-difference resolution limited only by with-in-die variation is developed.

12:15 G-7-4 (Late News)
3.6-Times Higher Acceptable Raw Bit Error Rate, 97% Lower-Power, NV-RAM & NAND-Integrated Solid-State Drives (SSDs) with Adaptive Codeword ECC
M. Fukuda, K. Higuchi, S. Tanakamaru and K. Takeuchi, Univ. of Tokyo (Japan)
An adaptive codeword ECC is proposed for NV-RAM/NAND integrated SSDs. The acceptable raw bit error rate before ECC of NV-RAM and NAND increases by 3.6-times. The 10Gbps high-speed write is achieved with 97% power reduction.

4F 244

H-7: 3D Interconnect (Area 2)

12:05 H-7-3
Through Silicon Photonic Via with Si core for Low loss and High Density Vertical Optical Interconnection in 3D-LSI
A. Noriki, K. W. Lee, J. Bea, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We proposed through-Si photonic via with Si core (TSPV) for low-loss and high-density vertical optical interconnection in 3D-LSI. We confirmed light confinement of the TSPV and showed feasibility of very fine TSPV by 2D-FDTD simulation.

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I-7: Processing and Interface Technologies (Area 6)

11:45 I-7-3
Impact of Interface States and Bulk Carrier Lifetime on Photocapacitance of Metal/Insulator/GaN Structure
P. Bidzinski[1], M. Miczek[1], B. Admowicz[1], C. Mizue[2] and T. Hashizume[2], [1]Silesian Univ. of Tech. and [2]Hokkaido Univ. (Poland)
The capacitance of a metal/insulator/GaN ultraviolet detector has been calculated versus the light excitation intensity and the gate voltage. The influence of the interface states and bulk carrier lifetime on the photodetector characteristics has been discussed and the calculation results have been compared with experimental data.

12:15 I-7-5
New Stacked MIM Capacitors with a Side-contact Formation Technology
T. Tsutsumi, S. Sugitani, K. Nishimura and M. Ida, NTT Corp. (Japan)
We proposed new stacked MIM capacitors with electrical side-contacts, which enable to be fabricated with very few masks and a short turn-around time. We successfully fabricated five-layer stacked MIM capacitor and increase capacitance density from 0.30 fF/μmm^2 to 1.51 fF/μmm^2.

4F 246

J-7: Nanowire Growth and Applications (Area 13)

11:45 J-7-3
Electrical Characterization of InGaAs nanowire MISFETs Fabricated by Dielectric-first Process
Y. Kohashi[1], T. Sato[1], K. Tomioka[1,2], S. Hara[1], T. Fukui[1] and J. Motohisa[1], [1]Hokkaido Univ. and [2]JST-PRESTO (Japan)
We attempted gate-dielectric-first process to fabricate MISFETs using single InGaAs nanowires formed by selective-area MOVPE. We obtained improved maximum drain current as compared to our previous nanowire FETs.

12:00 J-7-4
Lateral GaAs nanowires with triangular and trapezoidal cross-sections grown on (311)B and (001) substrates
G. Zhang, K. Tateno, H. Gotoh and T. Sogawa, NTT Corp. (Japan)
The cross-sectional shape of lateral nanowires can be varied by using substrates with different orientations. Lateral nanowires with triangular and trapezoidal cross-sections were grown on (311)B and (001) substrates.

12:15 J-7-5
C-V Characteristics and Analysis of Undoped Gate-All-Around Nanowire FET Array
R. H. Baek[1], C. K. Baek[2], S. H. Lee[1], S. D. Suk[3], M. Li[3], Y. Y. Yeoh[3], K. H. Yeo[3], D. W. Kim[3], J. S. Lee[1,4], D. M. Kim[2] and Y. H. Jeong[1,4], [1]POSTECH, [2]Korea Institute for Advanced Study (KIAS), [3]Samsung Electronics Company and [4]National Center for Nanomaterials and Technology (NCNT) (Korea)
We analyzed the effect of undoped and floating channel on the nanowire C-V curves and extracted accurate inversion charge and mobility. The measured data were compared extensively with conventional planar MOS capacitor data.

2F 222

K-7: Growth and Characterization of Nitrides (Area 8)

12:00 K-7-3
Nucleus and Spiral Growth of GaN Studied by Selective-Area Metalorganic Vapor Phase Epitaxy
T. Akasaka, Y. Kobayashi and M. Kasu, NTT Corp. (Japan)
We have fabricated step-free GaN surfaces with a diameter up to 50 microns by selective-area metalorganic vapor phase epitaxy. We also discuss the mechanism of both nucleus and spiral growth of GaN in detail.

12:15 K-7-4
Enhanced optical characteristics of light-emitting-diode by localized surface plasmon of Ag/SiO_2 nanoparticles
L. W. Jang[1], T. Sahoo[1], D. S. Jo[1], J. W. Yoo[1], J. W. Jeon[1], S. M. Li[2], Y. H. Cho[2] and I. H. Lee[1], [1]Chonbuk National Univ. and [2]KAIST (Korea)
We investigated the localized surface plasmon coupling behavior in LED by Ag/SiO2 nanoparticles. The PL intensity of Ag/SiO2 coated sample was enhanced by 50 % due to the energy coupling between MQW-SP of Ag/SiO2.

2F 223

12:30-13:30 Lunch

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G-8: Bio Nanofusion Technologies (Area 11)

(13:30-15:00)
Chairs: J. Ohta (NAIST)
M. Sasaki (Toyota Technological Inst.)

13:30 G-8-1 (Invited)
Novel Quantum Effect Devices realized by Fusion of Bio-template and Defect-Free Neutral Beam Etching
S. Samukawa[1,2], [1]Tohoku Univ. and [2]JST (Japan)
A 2D Si ND array with a high-density and well-ordered arrangement could be fabricated by using bio-template and damage-free Cl neutral beam etching. In this structure, the controllable band gap energy (from 2.2eV to 1.4eV) and high photon absorption coefficient (>105 cm^{-1}) could be obtained at RT by controlling the Si-ND structure.

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H-8: 3D Integration (Area 2)

(13:30-14:55)
Chairs: T. Fukushima (Tohoku Univ.)
G. Beyer (IMEC)

13:30 H-8-1 (Invited)
Low temperature bonding for 3D integration
T. Suga, Univ. of Tokyo (Japan)
The surface activated boding (SAB) is a highly potential method providing a low temperature interconnect process inevitable for 3D integration. The applications of SAB are demonstrated on Cu direct bonding, and hetero-semiconductor wafer bonding, and the future outlook of the method will be discussed.

4F 245

I-8: Crystulline and Thin Film Silicon Solar Cell (Ⅰ) (Area 14)

(13:30-15:15)
Chairs: G. Coletti (ECW Solar Energy)
A. Masuda (AIST)

13:30 I-8-1 (Invited)
Crystalline Silicon Solar Cells, Thinner the Better
Y. Hayashi[1,2], [1]AIST and [2]Univ. of Tsukuba (Japan)
Historical trajectory of research and development of the very and ultra thin cSi solar cell/module was reviewed. According to theoretical and experimental reports, more than 20% efficiency with about 10 micro-meter thick cell is one of future targets.

2F 222

K-8: Si and Ge-based Materials and Devices (Area 8)

(13:30-15:00)
Chairs: H. Hibino (NTT Basic Res. Labs.)
A. Yamada (Tokyo Tech)

13:30 K-8-1
Very high mobility 2D holes in strained Ge quantum well epilayers grown by Reduced Pressure Chemical Vapor Deposition
M. Myronov[1], K. Sawano[2], D. R. Leadley[1] and Y. Shiraki[2], [1]Univ. of Warwick and [2]Tokyo City Univ. (UK)
For the first time, we report a very high 2DHG mobility obtained in compressive strained Ge QW epilayers grown on SiGe/Si(100) virtual substrate by an industrial type RP-CVD technique.

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A-8: Organic Transistors and Device Fabrication Ⅰ (Area 10)

14:00 A-8-2
3 V-driven flexible organic transistors with mobility exceeding 2 cm^2/Vs
K. Fukuda[1], N. Uchiyama[1], T. Sekitani[1], U. Zschieschang[2], H. Klauk[2], T. Yamamoto[3], K. Takimiya[3] and T. Someya[1], [1]Tokyo Univ., [2]Max Planck Inst. and [3]Hiroshima Univ. (Japan)
We fabricated organic TFTs using DNTT as p-type semiconductors and phosphonic acid self-assembled monolayers (SAMs) as gate insulators, and optimized the transistor characteristics by changing the alkyl chain length of the SAMs.

14:15 A-8-3
Different interfacial carrier behaviors between α-NPD and pentacene double-layer device with a polyimide blocking-layer by time-resolved optical second harmonic generation
L. Zhang, D. Taguchi, J. Li, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
The paper reports totally different carrier behaviors in α-NPD and pentacene layer in a double-layer structure by using time-resolved second harmonic generation techniques.

14:30 A-8-4
Megahertz Operation of Rectifier Circuits using Pentacene Thin-Film Transistors
M. Kitamura and Y. Arakawa, Tokyo Univ. (Japan)
We report on rectification properties of pentacene transistor diodes. The transistor diodes successfully rectify an AC voltage at a frequency above 1 MHz into a DC voltage without decrease in the output voltage.

14:45 A-8-5
Realization of Pentacene-based Thin Film Transistor Arrays for Large-area Organic Electronics Being Compatible with the Roll-to-Roll Manufacturing Technique
L. Wang[1,2], D. Li[1] and C. Jiang[1], [1]National Center for Nanoscience and Tech. and [2]Chinese Academy of Sci. (China)
In this work a vacuum thermal evaporation (VTE) is extended to a VTE-roller method that may be compatible with a roll-to-roll manufacturing technique. We show that the technique combines high uniformity with excellent performance of the deposited arrays of OTFTs on large areas.

1F 212

1F 213

C-8: Gate-Insulator Reliability (Area 1) & (Area 3)

13:50 C-8-2
Effect of Hot-Carrier Stress on the Recoverable and Permanent Components of Negative-Bias Temperature Instability
T. J. J. Ho[1], D. S. Ang[1] and C. M. Ng[2], [1]Nanyang Tech. Univ. and [2]GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)
Channel hot-hole stressing is found to reduce the apparent recoverable component of NBTI under 0-V recovery. Results show that this is a consequence of an increase in the density of deep-level hole traps.

14:10 C-8-3
Effect of Positive Gate Stressing on the Recoverable Component of Negative-Bias Temperature Instability
A. A. Boo[1], D. S. Ang[1], Z. Q. Teo[1] and C. M. Ng[2], [1]Nanyang Tech. Univ. and [2]GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)
Positive gate stressing of the p-MOSFET is found to reduce the recoverable component (R) of NBTI. This finding contradicts a current viewpoint which ascribes R to preexisting and/or high-field induced oxide trap generation.

14:30 C-8-4
Investigation of Recovery Effects on Degraded pMOSFETs of 65 nm Technology with Different Annealing Temperatures
S. Y. Chen[1], C. H. Tu[1], Y. F. Chen[1], H. S. Huang[1], Z. W. Jhou[1], S. Chou[2] and J. Ko[2], [1]National Taipei Univ. of Tech. and [2]United Microelectronics Corp. (Taiwan)
This study shows that CHC and NBTI-induced Nit can be largely recovered after annealing. It is considered that only reaction mode occurs during the degradation and recovery phases, minor or no diffusion mode has occurred.

14:50 C-8-5
Gate Leakage Current Reduction in Two-Step Processed High-k Dielectrics for Low Power Applications
G. Bersuker[1], D. Heh[1], J. Huang[1], C.S. Park[1], A. Padovani[2], L. Larcher[2], P. D. Kirsch[1] and R. Jammy[1], [1]SEMATECH and [2]Università di Modena e Reggio Emilia (USA)
Reduction of the gate leakage current in nMOS high-k devices is demonstrated by an engineered two-step deposited Hf-based high-k dielectric film. The electrical characteristics and reliability of the devices fabricated using the proposed two-step and conventional one-step high-k gate stacks are shown to be comparable.

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D-8: Si Photonics (1) (Area 7)

14:00 D-8-2
Loss Measurement of Multiple Layer a-Si Waveguides toward 3D Si-Optical Circuits
J. H. Kang, K. Inoue, Y. Atsumi, N. Nishiyama and S. Arai, Tokyo Tech (Japan)
The relationship between the propagation loss and surface roughness in multilayered a-Si waveguides has been investigated. The propagation loss was significantly affected by the top-surface roughness rather than the material absorption of a-Si.

14:15 D-8-3
Analysis of Vertically Stacked Structures of 2D PC Cavity and Amorphous-Silicon-Wire Waveguide with Low-Refractive-Index Material Cladding
T. Yamada[1,2], M. Okano[2], Y. Sakakibara[2], T. Kamei[2], J. Sugisaka[1,2], N. Yamamoto[2], M. Itoh[1], T. Sugaya[2], K. Komori[2] and M. Mori[2], [1]Univ. of Tsukuba and [2]AIST (Japan)
We proposed and theoretically investigated a highly-efficient light-extraction means from a 2D PC cavity to a silicon-wire waveguide with low-refractive-index material cladding. The high light-extraction efficiency over 90% is achieved.

14:30 D-8-4
Polarization-independent 5.4-ns Group Delay for Entire C-band by Integrated Delay Line of Si Rib Waveguide
M. Tokushima, T. Chu, A. Kamei and T. Horikawa, AIST (Japan)
We report, to the best of our knowledge, the longest polarization-independent group delay of 5.4 ns measured with a Si rib waveguide for the entire C-band of photonic telecommunication wavelengths so far. It is suggested that the rib waveguide has a great potential for integrated delay lines applicable to photonic telecommunication subsystems.

14:45 D-8-5
Bandgap Control Using Strained Beam Structures for Si-Based Photonic Devices
K. Yoshimoto, R. Suzuki, Y. Ishikawa and K. Wada, Univ. of Tokyo (Japan)
We propose method to control bandgap using Si micro-beam structure, and got significant bandgap change (~0.2eV) by inducing mechanical stress on it. This amount of strain (~1.5%) cannot be achieved by previous methods.

15:00 D-8-6
Strained SiGe-on-Si beam for tunable near-infrared light emission
R. Suzuki[1], K. Yoshimoto, L. Décosterd[1,2], Y. Ishikawa[1] and K. Wada, [1]Univ. of Tokyo and [2]Ecole Polytechnique Fédérale de Lausanne (Japan)
We propose a method to control the wavelength of near-infrared light emission from a beam-shaped germanium-rich SiGe by applying mechanical stress. Photoluminescence spectra show a bandgap narrowing under external stress, indicating a tunability of emission wavelength by applying a mechanical stress.

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E-8: PRAM/ReRAM (Area 4)

14:00 E-8-2
A SiO_2 Nano-thermal Unipolar 0T-1R ReRAM Device with Built-in Diode Isolation
K. P.Chang, H. T. Lue, K. Y. Hsieh and C. Y. Lu, Macronix Int'l Co., Ltd. (Taiwan)
Unipolar ReRAM devices using SiO2 as the storage node and an in-situ formed diode as the isolation device are studied. The extremely simple process promises potential for very low cost high-density storage.

14:20 E-8-3
Resistive Switching Device for Neuromorphic Device Application
K. Seo, I. Kim, S. Park, S. Jung, M. Siddik, J. Park, J. Kong, K. Lee, B. Lee and H. Hwang, GIST (Korea)
We mimicked various Spike Timing Dependence Plasticity (STDP) synaptic rules via resistive switching device. We showed potentiating, depressing and uniformity as well as frequency and weight dependency of the device for future neuromorphic application.

14:40 E-8-4
"A Novel Ni/WO_X /W ReRAM with Excellent Retention and Low Switching Current"
W.C. Chien[1], Y.C. Chen[1], F.M. Lee[1], Y.Y. Lin[1], E.K. Lai[1], Y.D. Yao[2], J. Gong[3], S.F. Horng[3], C.W. Yeh[1], S.C. Tsai[1], C.H. Lee[1], Y.K. Huang[1], C.F. Chen[1], H.F. Kao[1], Y.H. Shih[1], K.Y. Hsieh[1] and C. Y. Lu[1], [1]Macronix Int'l Co., Ltd., [2]Fu Jen Univ. and [3]National Tsing Hua Univ. (Taiwan)
The top electrode (TE) material plays an important role in WOX ReRAM characteristics. A novel Ni TE WOX ReRAM shows superior performances such as a switching current density < 8x105A/cm2, > 100X resistance ratio window, and extremely good data retention of > 300 years at 85 °C.

15:00 E-8-5 (Late News)
Microstructural Characterization in Reliability Measurement of PRAM
J. Bae, K. Hwang, K. Park, S. Jeon, D. H. Kang, S. Park, J. Ahn, S. Kim, G. Jeong and C. Chung, Samsung Electronics Co., Ltd. (Korea)
The cell failures after cycling endurance in PRAM have been classified into 3 groups (Stuck set, Stuck reset, tails from reset distribution), which have been analyzed by TEM.

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F-8: Spintronics (Ⅲ) - Semiconductors - (Area 12)

14:00 F-8-2 (Invited)
Electrical detection of Spin Transport in Si using High-quality Schottky Contacts
K. Hamaya[1,2], Y. Ando[1] and M. Miyao[1], [1]Kyushu Univ. and [2]PRESTO, JST (Japan)
We show high-quality formation of ferromagnetic Schottky source and drain contacts for spin-transistor applications, and demonstrate electrical spin injection and detection in Si using these contacts.

14:30 F-8-3
Spin injection into GaAs from Fe/GaO_x Tunnel Injector
H. Saito[1], J. C. Le Breton[2], V. Zayets[1], Y. Mineno[1,3], S. Yuasa[1] and K. Ando[1], [1]National Inst. of Adv. Indus. Sci. and Tech, [2]Univ. of Twente and [3]Toho Univ. (Japan)
We examined the electrical injection of spin-polarized electrons into a GaAs-based light-emitting diode structure from a Fe/GaO_x tunnel injector whose electron-charge injection efficiency was comparable to that of a conventional Fe/n$^+$AlGaAs ohmic injector.

14:45 F-8-4
Large magnetoresistance of $Ge_{1-x}Mn_x$ single films and heterostructures with magnetic nanocolumns
S. Yada, R. Okazaki and M. Tanaka, Univ. of Tokyo (Japan)
We observed large positive magnetoresistance in single films and heterostructures of $Ge_{1-x}Mn_x$ with amorphous $Ge_{1-y}Mn_y$ nanocolumns. Hysteretic behavior of magnetoresistance was also observed in the heterostructure, which might be caused by magnetization of $Ge_{1-x}Mn_x$.

Coffee Break (2F Forum)

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G-8: Bio Nanofusion Technologies (Area 11)

14:00 G-8-2
Planer Multi Electrode Array Coupled CMOS Image Sensor for in vitro Electrophysiology
A. Nakajima[1], T. Noda[1,2], K. Sasagawa[1,2], T. Tokuda[1,2], Y. Ishikawa[1,2], S. Shiosaka[1,2] and J. Ohta[1,2], [1]NAIST and [2]JST-CREST (Japan)
Multi-electrode Array Coupled CMOS image (MARC) sensor was designed for *in vitro* electrophysiology. We report design of MARC sensor, fabrication of Pt black microelectrode and a preliminary result from functional validations by imaging mouse brain slice.

14:15 G-8-3
Atmospheric Pressure Micro Inductively Coupled Plasma Light Source towards Portable Spectrometry System
S. Kumagai[1], H. Matsuyama[1], M. Hori[2] and M. Sasaki[1], [1]Toyota Technological Inst. and [2]Nagoya Univ. (Japan)
Atmospheric pressure inductively coupled plasma device is developed from glass epoxy substrate for portable light source. Plasma generation at 35W RF power is confirmed. Emission spectra with sharp peaks and the device durability are demonstrated.

14:30 G-8-4
Controlled Thermal Emission of Narrow-band IR Waves for Downsizing Sensor Module
K. Masuno, S. Kumagai and M. Sasaki, Toyota Technological Inst. (Japan)
New narrow-band wavelength selective IR emitter suitable for downsizing is proposed. Radiance peak at λ=1.67μm, which corresponds to Wood's anomaly of grating, and higher power efficiency are confirmed.

14:45 G-8-5
Fabrication and Location of 3-nm Pt Wires onto Silicon Surfaces
M. Kobayashi[1,2], K. Onodera[2], Y. Watanabe[3], K. Shiba[1] and I. Yamashita[2,4], [1]Japanese Foundation for Cancer Res., [2]NAIST, [3]Univ. of Tokyo and [4]Panasonic Corp. (Japan)
Fabrication and location of high aspect ratio 3-nm Pt wires onto silicon surfaces was achieved using a tube-shaped tobacco mosaic virus, which could not be achieved using conventional lithography.

4F 244

H-8: 3D Integration (Area 2)

14:00 H-8-2
Self-Assembly with Metal Microbump-to-Microbump Bonding for Advanced Chip-to-Wafer 3D Integration
E. Iwata, Y. Ohara, K. W. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We demonstrate highly productive microbump-to-microbump bonding method for the chip-to-wafer 3D integration. We aligned chips onto Si wafer using self-assembly method and established conduction of daisy chains having 5-, 10-um-size microbumps.

14:20 H-8-3
Metal Micro-Bump Induced Stress in 3D-LSIs _ a micro-Raman Study
M. Murugesan, Y. Ohara, J. C. Bea, K. W. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
In the flip-chip bonded 3D-LSI die/wafer via metal micro bump, the metallic micro-joint exerted a large compressive stress for the region underneath the micro-bump, and it is extended up to more than 10 μm. Since this value is pretty close to the depletion region thickness, and for extremely thin LSI die/wafer it would have an adverse impact on the device characteristics.

14:40 H-8-4 (Late News)
High Density and Power Efficient SiP with SCS Technology
E. Hosomi[1], Y. Matsubara[1], Y. Fujimoto[1], M. Oida[2], H. Ezawa[1], M. Fukuda[1], K. Numata[1] and K. Miyamoto[1], [1]Toshiba Corp. and [2]J-Devices Corp. (Japan)
SiP with SCS (stacked chip SoC) enables high bandwidth connection between logic and memory devices. SCS technology has advantage against eDRAM in reliability and cost. SCS offers low power solution compared to the conventional SiP structure with wire bonding.

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I-8: Crystulline and Thin Film Silicon Solar Cell (Ⅰ) (Area 14)

14:00 I-8-2
Enhanced Power Conversion Efficiency for Silicon Solar Cells Utilizing a Uniformly Distributed Indium-Tin-Oxide Nano-Whiskers
C. H. Chang[1], M. H. Hsu, W. L. Chang[2], W. C. Sun and P. Yu[1], [1]National Chiao Tung Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
Distinctive ITO nano-whiskers, grown by electron-beam evaporation, have been employed as a cost-effective ARC for Si solar cells. The nanostructure exhibits excellent anti-reflection for the wavelength range of 450nm~1050nm. The ITO-whiskers cell achieves 17.1% efficiency.

14:15 I-8-3
Microstructures of polycrystalline silicon films formed through explosive crystallization induced by flash lamp annealing
K. Ohdaira[1,2], S. Ishii[1], N. Tomura[1] and H. Matsumura[1], [1]JAIST and [2]JST (Japan)
Flash lamp annealing (FLA) induces explosive crystallization, lateral crystallization driven by the liberated latent heat, and TEM observations have clarified the microstructures of the flash-lamp-crystallized poly-Si films having periodic two characteristic regions formed spontaneously during the explosive crystallization.

14:30 I-8-4
Stacked Solar Cells using Transparent and Conductive Adhesive
J. Takenezawa[1], M. Hasumi[1], T. Sameshima[1], T. Koida[2], T. Kaneko[2], M. Karasawa[2] and M. Kondo[2], [1]Tokyo Univ. of Agri. And Tech. and [2]AIST (Japan)
We demonstrate multi-junction solar cells by stacking top a-Si:H p-i-n cell on bottom HIT silicon cell using polyimide transparent adhesive dispersed with ITO conductive particles. The Voc increased to 1.34V under illumination of AM 1.5.

14:45 I-8-5
In-situ observation of polycrystalline Si thin films grown using Al-doped ZnO on glass substrate by the aluminum-induced crystallization
M. Jung[1], A. Okada[2], T. Saito, T. Suemasu[2] and N. Usami[1], [1]Tohoku Univ. and [2]Univ. of Tsukuba (Japan)
Recently, the poly-Si thin film grown on glass substrate is attracting for large area electronic and solar cell applications [1,2]. As a common approach of crystallizing amorphous Si (a-Si), there are solid phase crystallization [3], excimer laser annealing [4], and metal-induced crystallization (MIC) [5-7]. Among them, the MIC process using metals such as Ni, Ag, Al, and Au is promising to obtain large-grained high quality material with low thermal budget.

15:00 I-8-6
Photothermal Spectroscopy by Atomic Force Microscopy on Crystalline Silicon Solar Cell Materials
K. Hara and T. Takahashi, Univ. of Tokyo (Japan)
We have performed the PT spectroscopy by AFM on single crystalline Si solar cell materials and discussed the influences of the surface recombination as well as the minority carrier diffusion length on the PT signals.

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K-8: Si and Ge-based Materials and Devices (Area 8)

13:45 K-8-2
Formation of Pyramidal-shaped Etch Pits on Germanium Surfaces Using Catalytic Reactions with Metallic Nanoparticles in Water
T. Kawase, K. Nishitani, K. Dei, J. Uchikoshi, M. Morita and K. Arima, Osaka Univ. (Japan)
We present an environmentally friendly formation of pyramidal-shaped etch pits on a Ge(100) surface with metallic nanoparticles in water. We also discuss a possible mechanism by electronic energy relationships.

14:00 K-8-3
Fabrication of defect-free and relaxed Ge-rich SGOI-wire structures for CMOS applications
M. Oda, Y. Moriyama, K. Ideda, Y. Kamimuta and T. Tezuka, MIRAI-TOSHIBA (Japan)
Strain-relaxed and defect-free SGOI wire structures were demonstrated by the proposed condensation-melting-recrystallization process. This technique will enable us to fabricate non-planar Ge-rich SGOI CMOS devices with additional stressor techniques for high-performance or low-power consumption applications.

14:15 K-8-4
Fabrication of Poly-Si TFT on Polycarbonate Substrate at Temperatures below 135°C
G. Nakagawa[1], N. Kawamoto[2], T. Imamura[3], Y. Tomizawa[3], T. Miyoshi[2], K. Tadatomo[2] and T. Asano[1], [1]Kyushu Univ., [2]Yamaguchi Univ. and [3]TEIJIN Ltd. (Japan)
We demonstrate the fabrication of poly-Si TFTs on polycarbonate substrate at temperatures below 135°C, i.e. well below the glass transition temperature of polycarbonate. TFTs whose electron mobility is over 10 cm^2/Vs can be fabricated.

14:30 K-8-5
Strain-Induced Back Channel Electron Mobility Enhancement in Poly-Si TFTs Formed by Continuous-Wave Laser Lateral Crystallization
S. Fujii, S. I. Kuroki, K. Kotani and T. Ito, Tohoku Univ. (Japan)
The back interface of the CLC poly-Si films had larger tensile strain than the surface. As a result, back channel electron mobility was 1.2 times larger than front channel electron mobility.

14:45 K-8-6
Epitaxial $NiSi_2$ Buffer Technique for Fluoride Resonant Tunneling Devices on Si
K. Takahashi, Y. Yoshizumi, Y. Fukuoka, N. Saito and K. Tsutsui, Tokyo Tech (Japan)
To fabricate CaF2/CdF2/CaF2 RTDs on Si, we propose the introduction of NiSi2 buffer layers to control the chemical reaction between Si and CdF2. We investigated the growth condition of NiSi2 on Si.

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Coffee Break (2F Forum)

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A-9: Organic Transistors and Device Fabrication Ⅱ (Area 10)
(15:30-17:15)
Chairs: S. Aratani (Hitachi, Ltd.)
M. Nakamura (Chiba Univ.)

15:30 A-9-1
Excellent interface properties of pentacene based metal-oxide-semiconductor diodes utilizing HfON higk-κ gate insulator
M. Liao, Y. U. Song, J. Ishikawa, T. Sano, J. Gao, H. Ishiwara and S. Ohmi, Tokyo Tech (Japan)
Pentacene based MOS diodes using SiO_2, HfO_2 and HfON as gate insulators were investigated. It was found that pentacene based MOS diodes with HfON gate insulators show a small flat-band voltage shift and a negligible frequency dispersion in C-V characteristics.

15:45 A-9-2
Oxygen Plasma Process of Self-assembled Monolayer Gate Dielectric for 2-V Operation High-mobility Organic TFT
K. Kuribara[1], T. Nakagawa[1], K. Fukuda[1], T. Yokota[1], T. Sekitani[1], U. Zschieschang[2], H. Klauk[2], T. Someya[1], T. Yamamoto[3] and K. Takimiya[3], [1]Univ. of Tokyo, [2]Max Planck Inst for Solid State Res. and [3]Hiroshima Univ. (Japan)
We optimized parameters of oxgen plasma process of self-assembled monolayer gate dielectric for organic TFTs. Short exposure time of plasma process (200 W, 30 sec.) products good transistors with high mobility of 0.97 cm^2/Vs and small hysteresis.

16:00 A-9-3
Direct observation of carrier behavior leading to electroluminescence in tetracene field-effect transistor
Y. Ohshima, H. Satou, T. Manaka, H. Kohn, N. Hirako and M. Iwamoto, Tokyo Tech (Japan)
We probed the carrier behavior leading to the electroluminescence under AC electric field in tetracene field-effect transistor using optical second harmonic generation technique, and clarified the space charge field effect on carrier injection.

16:15 A-9-4
Diffuser micropump structured with extremely flexible diaphragm of 2 micron-thick polyimide film
Y. Liu, H. Komatsuzaki, Z. Duan and Y. Nishioka, Nihon Univ. (Japan)
The simple structured air-actuated valveless micropump with the 2.1 micron-thick polyimide membrane was designed, fabricated and measured. The micropump was fabricated on the 60 micron-thick thin Si wafer using surface micromachining techniques.

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B-9: Interface and Strain Characterization (Area 1)
(15:30-17:10)
Chairs: O. Nakatsuka (Nagoya Univ.)
S. Migita (AIST)

15:30 B-9-1
Measurements of Electrostatic Potential Across p-n Junctions on Oxidized Si Surfaces by Scanning Multi-Mode Tunneling Spectroscopy
L. Bolotov, T. Tada, M. Iitake, M. Nishizawa and T. Kanayama, AIST (Japan)
High-resolution measurements of the surface potential was demonstrated on oxidized Si surfaces by scanning multi-mode tunneling spectroscopy at optimized tunneling gap. The potential maps agree with build-in potential for p-n junctions, while nanometer-scale fluctuations were caused by structural and charge variations.

15:50 B-9-2
Interfacial atomic structure between Pt-added NiSi and Si (001)
N. Ikarashi, M. Narihiro and T. Hase, Renesas Electronics Corp. (Japan)
HAADF-STEM revealed that Pt segregates at lattice-matched areas of the interface and occupied the Ni sites at the first interfacial atomic layer of NiSi. This finding shows that Pt segregates to lower the interfacial strain, reducing the interface energy. Thus, we infer that the interface-energy lowering results in the NiSi layer being stabilized.

16:10 B-9-3
TO- and LO-mode analyses in asymmetric stretching vibrations in ultra thin thermally grown GeO_2 on Ge substrate
M. Yoshida[1], T. Nishimura[1,2], C. H. Lee[1], K. Kita[1,2], K. Nagashio[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
A IR investigation of thin GeO_2 was performed for the first time, with a conscious of both TO and LO modes. Local bond feature such as the bridging bond angle is governed by the oxidation temperature just like that in SiO_2, while macroscopic one such as void defect seems to be determined by both temperature and pO_2.

16:30 B-9-4
Quantitative Analysis of Stress Relaxation in TEM specimen fabrication by Raman Spectroscopy with High-NA Oil-Immersion Lens
D. Kosemura[1,2] and A. Ogura[1], [1]Meiji Univ. and [2]JSPS (Japan)
The stress relaxation in the TEM specimens of SSOI was evaluated by Raman spectroscopy with high-NA oil-immersion lens. It was confirmed that the values of the relaxation was 75% at the thickness of 240 nm.

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C-9: Emerging Device Technology (Area 3)
(15:30-17:15)
Chairs: D. Hisamoto (Hitachi, Ltd.)
S. Hayashi (Panasonic Corp.)

15:30 C-9-1 (Invited)
CVD Graphene for High Speed Electronics
B. C. Huang, C. Q. Miao, Y. Wang, Y. H. Xie and J. C. S. Woo, UCLA (USA)
Few-layer graphene film was deposited on Ni film and Ni dots using CVD method. Under low temperature growth condition, the uniformity of graphene was remarkably improved. Top-gated graphene transistors are made by transferring the graphene film onto a SiO2 substrate. Ambipolar conduction is clearly observed from I_{DS}-V_{GS} curve

16:00 C-9-2
High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization
J. Mitard[1], B. De Jaeger[1], G. Eneman[2,3], A. Dobbie[4], M. Myronov[4], M. Kobayashi[5], J. Geypen[1], H. Bender[1], B. Vincent[1], R. Krom[2], J. Franco[2], G. Winderickx[1], E. Vrancken[1], W. Vanherle[1], W. E. Wang[1], J. Tseng[6], R. Loo[1], K. De Meyer[2], M. Caymax[1], L. Pantisano[1], D. R. Leadley[4], M. Meuris[1], P. P. Absil[1], S. Biesemans[1] and T. Hoffmann[1], [1]IMEC, [2]K.U Leuven, [3]FWO, [4]Univ. of Warwick, [5]Stanford Univ. and [6]TSMC (Belgium)
High hole-mobility 65nm biaxially-strained Ge-pFETs, with reduced EOT while maintaining minimized SCE, have been fabricated and electrically characterized in-depth for the low and high field transport. We demonstrate a 35%-I_{ON} gain for nano-scaled s-Ge pFETs.

16:40 C-9-4
Analysis of the Junctionless Transistor Architecture
J. P. Colinge[1], J. P. Raskin[2], A. Kranti[1], I. Ferain[1], C. W. Lee[1], N. Dehdashti Akhavan[1], P. Razavi[1], R. Yan[1] and R. Yu[1], [1]Univ. College Cork. and [2]Université catholique de Louvain (Ireland)
Strain is used to improve mobility in junctionless transistors. A bulk silicon version of the device is studied by simulation, and performance similar to that of the SOI version of the device are obtained.

2F 221

D-9: Si Photonics (2) (Area 7)
(15:30-17:15)
Chairs: H. Yamada (Tohoku Univ.)
M. Tokushima (AIST)

15:30 D-9-1
Real-time synchrotron radiation X-ray diffraction and abnormal temperature dependence of photoluminescence from erbium silicates on SiO_2/Si substrates
H. Omi[1], T. Tawara[1], M. Tateishi[1], H. Komatsu[1], S. Takeda[2], Y. Tsusaka[3], Y. Kagoshima[3] and J. Matsui[2], [1]NTT Basic Res. Labs., [2]Univ. of Hyogo and [3]CAST (Japan)
We characterized the formation of erbium silicates on silicon oxide films in real time using synchrotron radiation grazing incidence X-ray diffraction (GIXD). We also characterized light emission from the erbium silicates by photoluminescence measurements.

15:45 D-9-2
Evaluation of optical absorption and light propagation loss in $Er_xY_{2-x}SiO_5$ crystal waveguides
K. Homma, T. Nakajima, T. Kimura and H. Isshiki, Univ. of Electro-Communications (Japan)
We demonstrate introduction of ErxY2-xSiO5 to the waveguide, resulting in suppression of CUC in this system. And optical absorption cross section of Er ions and light propagation loss in the ErxY2-xSiO5 crystal waveguide are evaluated.

16:00 D-9-3
Design and Simulation of Silicon Ring Optical Modulator with p/n Junctions along Circumference
Y. Amemiya, H. Ding and S. Yokoyama, Hiroshima Univ. (Japan)
Silicon ring optical modulator with p/n junctions along circumference is proposed. Its performance at 1 V is simulated. The modulation > 95% is obtained at $1x10^{17}$-$5x10^{17}$ cm^{-3} carrier concentration and propagation loss < 5 dB/cm.

16:15 D-9-4
Design of Broadband Optical Switch Based on Mach-Zehnder Interferometer with Si wire Waveguides
K. Kintaka, Y. Shoji, S. Suda, H. Kawashima, T. Hasama and H. Ishikawa, AIST (Japan)
2x2 optical switches based on Mach-Zehnder interferometer (MZI) with Si wire waveguides are designed for broadband operation. Wavelength dependences of MZI switches using directional couplers, multimode interference couplers, and wavelength-insensitive couplers are calculated numerically.

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E-9: ReRAM (Area 4:)
(15:30-17:15)
Chairs: K. Ishihara (Sharp Corp.)
K. Hamada (Elpida Memory, Inc.)

15:30 E-9-1 (Invited)
Overview and Future Challenges of Hafnium Oxide ReRAM
Y. S. Chen[1,2], H. Y. Lee[1,2], P. S. Chen[3], P. Y. Gu[1], Y. Y. Hsu[1], W. H, Liu[1], C. H. Tsai[1], S. M. Wang[1], S. S. Sheu[1], P. C. Chiang[1], W. P. Lin[1], W. S. Chen[1], F. T. Chen[1], C. H. Lien[2] and M. J. Tsai[1], [1]ITRI, [2]National Tsing Hua Univ. and [3]Mingshin Univ. of Sci. and Tech. (Taiwan)
A highly reliable Hafnium Oxide ReRAM with high speed, low power operation, and excellent reliabilities including nonvolatility and endurance is demonstrated. A 1 Kb array with robust cycling endurance can be achieved by effective verifications. Some challenges must be overcome to realize this memory as a promising nonvolatile memory.

16:00 E-9-2
A New Tunneling Barrier Width Model of the Switching Mechanism in Hafnium Oxide-Based Resistive Random Access Memory
Y. H. Tseng[1], S. S. Chung[1,2], S. Shin[2], S. S. M. Kang[2], H. Y. Lee[3] and M. J. Tsai[3], [1]National Chiao Tung Univ., [2]Univ. of California, Merced and [3]ITRI (Taiwan)
In this paper, the switching characteristics of Ti/HfO2/TiN resistive random access memory (RRAM) have been examined. A novel tunneling barrier width model based on WKB approximation is proposed to explain the pertinent current-voltage characteristic and the origin of the resistance changing in RRAM.

16:20 E-9-3
High OFF/ON-resistive NiO ReRAM using Post-Plasma-Oxidation (PPO) process
K. Okamoto, M. Tada, K. Ito, Y. Saito, S. Ishida and H. Hada, NEC Corp. (Japan)
NiO resistive change cells with a high OFF/ON resistance ratio of 10^5 are realized using low temperature, post-plasma-oxidation (PPO) while reducing cell-to-cell variation of forming voltages.

16:40 E-9-4
Effects of Reactive Ti Creating Oxygen Vacancy Inside TiO_2 on Resistive Switching Characteristics in Resistive Random Access Memory Device
S. J. Kim, M. G. Sung, W. G. Kim, J. Y. Kim, J. H. Yoo, J. N. Kim, B. G. Gyun, J. Y. Byun, M. S. Joo, J. S. Roh and S. K. Park, Hynix Semiconductor Inc. (Korea)
The effects of reactive Ti layer on the resistive switching characteristics of TiO2-based ReRAM are investigated. Ti acts as a good oxygen gettering layer which makes the TiO2 to have a higher concentration of oxygen vacancy.

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F-9: Spintronics (Ⅳ) - Device and Circuits - (Area 12)
(15:30-17:00)
Chairs: K. Ando (AIST)
M. Yamamoto (Hokkaido Univ.)

15:30 F-9-1 (Invited)
Spin transfer torque effects in nanopillar devices with perpendicular anisotropy
S. Mangin, IJL – Nancy Université (France)
Spin-polarized current is used to reverse magnetization orientation in nanomagnets with strong perpendicular anisotropy. We will discuss the efficiency of such geometry, dynamic behaviours as well as domain nucleation and propagation while a field is applied and a current is injected in the nanopillar

16:00 F-9-2
High Speed Spin-Transfer Switching in GMR Nanopillars with Perpendicular Anisotropy
H. Tomita[1], T. Nozaki[1], T. Seki[1], T. Nagase[2], E. Kitagawa[2], M. Yoshikawa[2], T. Daibou[2], M. Nagamine[2], S. Ikegawa[2], N. Shimomura[2], H. Yoda[2] and Y. Suzuki[1], [1]Osaka Univ. and [2]Toshiba R & D center (Japan)
We investigated high-speed (sub-nano second) spin-transfer switching property in giant magnetoresistance (GMR) nanopillar systems with perpendicular magnetic anisotropy.

16:15 F-9-3
Hierarchical Nonvolatile Memory with Perpendicular Magnetic Tunnel Junctions for Normally-Off Computing
K. Abe, K. Nomura, S. Ikegawa, T. Kishi, H. Yoda and S. Fujita, Toshiba Corp. (Japan)
Hierarchical nonvolatile-memory composed of embedded-MRAM for L3 cache and nonvolatile-SRAM with MTJs for L2 cache is proposed. The average power of microprocessor with the hierarchical nonvolatile-memory is reduced by 65% in long standby time.

16:30 F-9-4
Design of a Process-Variation-Aware Nonvolatile MTJ-Based Lookup-Table Circuit
D. Suzuki, M. Natsui, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)
This paper presents a process-variation-aware nonvolatile lookup table circuit for nonvolatile field-programmable gate array with ultra-low power and immediate wakeup capability using MOS/MTJ hybrid structure.

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G-9: Nanomaterial Applications (Area 11) (15:30-16:30) Chairs: I. Yamashita (NAIST) K. Sawada (Toyohashi Univ. of Tech.)	**H-9: Image Sensor (Area 2)** (15:30-16:25) Chairs: M. Kodera (Toshiba Corp.) M. Matsuura (Renesas Electronics Corp.)	**I-9: Crystulline and Thin Film Silicon Solar Cell (Ⅱ) (Area 14)** (15:30-16:45) Chairs: Y. Hayashi (AIST) N. Usami (Tohoku Univ.)			
15:30 G-9-1 **Free-Standing Lipid Bilayers Based on Nanoporous Alumina Films** *A. Hirano-Iwata[1,2], T. Taira[1], A. Oshima[1], Y. Kimura[1] and M. Niwano[1], [1]Tohoku Univ. and [2]PRESTO, JST (Japan)* Mechanical stability of free-standing bilayer lipid membranes (BLMs) was improved by suspending the BLMs in nanoporous alumina films. The membrane stability was investigated in terms of lifetime and breakdown voltage.	**15:30 H-9-1** **Characterization of LTO coating on microlens of CMOS image sensor** *J. Gambino, B. Leidy, C. Musante, K. Ackerson, B. Guthrie, J. Twombly, E. Cooney, P. Pokrinchak, D. Meatyard, J. Adkisson, R. J. Rassel and M. Jaffe, IBM (USA)* CMOS image sensors with an LTO coating on the microlens have been characterized for dark current, quantum efficiency, and reliability.	**15:30 I-9-1 (Invited)** **Impact of Metal Contamination in Silicon Solar Cells** *G. Coletti, ECN Solar Energy (the Netherlands)* Impact of transition metals on the conversion efficiency of silicon solar cells is presented. Fe, Cr and Ti reduce the internal quantum efficiency (IQE) at long wavelength reducing the carrier diffusion length. Ni reduces the IQE at short wavelength increasing recombination in the solar cell emitter region. Cu reduces the IQE at both short and long wavelength. A physical model is presented explaining the data.			
15:45 G-9-2 **Fabrication of CMOS-compatible Poly-Si Nanowire FET Sensor** *H. Y. Chen[1,2], C. Y. Lin[2], M. C. Chen[2], H. C. Chen[2], C. C. Huang[2] and C. H. Chien[1,2], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)* A low-cost, superior uniformity Poly-Si nanowire FET sensor fabrication method features entire CMOS processing is presented. A self-aligned nanowire fabrication in bulk-Si technology is also disclosed for the first time for highly integrated sensor system design.	**15:50 H-9-2** **Near-Infrared Image Sensor Fabricated Using Compliant Bump** *N. Watanabe[1,3], F. Hoashi[1], Y. Nagai[2], H. Inada[2], Y. Iguchi[2] and T. Asano[1], [1]Kyushu Univ. , [2]Sumitomo Electric Industries, Ltd. and [3]Fukuoka Industry Sci. and Tech. Foundation (Japan)* We demonstrated a near-infrared image sensor in which an InGaAs/InP photodiode chip was electrically connected to a CMOS read-out circuit chip through compliant bumps.	**16:00 I-9-2** **Optimum design of a-Si:H/μc-Si:H tandem thin film solar cells with a low-refractive-index AZO transparent conducting oxide** *J. W. Leem and J. S. Yu, Kyung Hee Univ. (Korea)* Aluminum-doped zinc oxide (AZO) thin films with low-refractive-index (low-n) as a transparent conducting oxide (TCO) layer for Si solar cells are deposited on Si and glass substrates by rf magnetron sputter using an oblique angle deposition technique. To improve the efficiency, the a-Si:H/μc-Si:H tandem solar cells with a TCO layer of low-n AZO are designed using a Silvaco ATLAS simulation.			
16:00 G-9-3 (Late News) **Carbon nanotube-based sensor Device compatible with the CMOS process** *J. T. Huang, P. L. Hsu, T. H. Lin, W. T. Hsieh, K. Y. Lee, C. K. Chen and T. C. Tsai, National Taipei Univ. of Tech. (Taiwan)* This paper presents a low temperature fabrication method of Carbon Nanotubes(CNTs)-based sensors device on a CMOS integrated circuit chip made by TSMC 0.35μm CMOS process.	**16:10 H-9-3 (Late News)** **MEMS Resonance Test for Mechanical Characterization of Nano-Scale Thin Films** *H. Yamagiwa[1], D. Goto[1], T. Namazu[1], T. Takeuchi[2], K. Murakami[2], Y. Kawashimo[2], T. Takano[3], K. Yoshiki[1] and S. Inoue[1], [1]Univ. of Hyogo, [2]Shinko Seiki Co. Ltd. and [3]The New Industry Research Organization (Japan)* The purpose of this study is to develop a quantitative measurement method for the Young's modulus of nanometer-thick films. We developed the test technique using a MEMS resonator array and measured the Young's moduli of Al and plasma-polymerization films made from CH4 and CHF3 gases.	**16:15 I-9-3** **Efficiency enhancement of a-Si thin film solar cells by using different light trapping structures** *C. W. Kuo[1], W. P. Chu[1], J. S. Lin[2,3], T. C. Lin[4], Y. S. Tsai[1], F. S. Juang[1], M. H. Chung[5], T. E. Hsieh[5] and M. O. Liu[3], [1]National Formosa Univ., [2]Osaka Univ., [3]Industrial Tech. Res. Inst., [4]KunSan Univ. and [5]National Chiao Tung Univ. (Taiwan)* This study produced various light trapping structures in order to enhance efficiency for a-Si solar cells. When combining V-shape with a cross-like pattern, Jsc and efficiency were shown to increase to 12.35mA/cm2 and 6.29%, respectively.			
16:15 G-9-4 (Late News) **Light-Addressable Potentiometric Sensors for Sodium Ion Detection by Fluorinated-Atomic Layer Deposition Hafnium Oxide Membrane** *C. H. Chin[1], J. H. Yang[1], T. F. Lu[1], C. E. Lue[1], C. M. Yang[2] and C. S. Lai[1], [1]Chang Gung Univ. and [2]Inotera memories Inc. (Taiwan)* In this study, an inorganic method was investigated for Na+ detection based on LAPS. The sensing membrane, HfO2 layer, was deposited by ALD and treated by RTA and CF4 plasma. The pH sensitivity was decreased and pNa sensitivity was increased by CF4 plasma. Finally, the highest pNa sensitivity was 34.8 mV/pNa measured from pNa 1 to pNa 4.		**16:30 I-9-4** **Three-terminal a-Si solar Cells** *C. H. Tai, C. H. Lin, C. M. Wang and C. C. Lin, National Dong Hua Univ. (Taiwan)* A new back-to-back pin-nip structure increases the average electric field in a solar cell. The 0.28-m-thick three-terminal a-Si solar cell achieved an efficiency of 11.4 %.			

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A-9: Organic Transistors and Device Fabrication Ⅱ (Area 10)

16:30 A-9-5
Printed Electrode for All-Printed Polymer Diode
M. Yoshida, K. Suemori, S. Uemura, S. Hoshino, N. Takada, T. Kodzasa and T. Kamata, AIST (JAPAN)
We have developed a mechanical sintering technique for printed metal patterns. Using this technique, printed electrode with various work functions from 3.5eV to 5eV could be prepared on a plastic substrate. These printed alloys were effective to improve the performance of printed diode and transistors.

16:45 A-9-6
A Tunable Emission Prepared by Novel Photo-induced Color-Change Materials
W. T. Liu and W. Y. Huang, National Sun Yat-sen Univ. (Taiwan)
An organic phospher C-545T was used as a green light dopant in this study. After protonation the protonated C-545T could be transformed into an orange or red emitter depending on the degree of protonation. Accordingly, green, orange and red emitting layers were fabricated by doping C-545T in PAG containing resin with different light exposures. In conjunction with a blue-light pumping source, the above emitting layers could be easily integrated into a white light emission.

17:00 A-9-7 (Late News)
Fabrication of Sol-Gel Alumina Dielectric for Low-Voltage Operating Pentacene Transistor
K. K. Han[1] and S. Seo[2], [1]Seoul National Univ. and [2]Kyungwon Univ. (Korea)
A sol-gel alumina dielectric for pentacene transistor has been introduced. With this alumina dielectric, the low voltage pentacene thin film transistor is fabricated and it is free from the threshold voltage shift problems.

1F 212

B-9: Interface and Strain Characterization (Area 1)

16:50 B-9-5
Uniaxial and Biaxial Strain Distribution Mapping in SOI Micro-Structures by Polarized Raman Spectroscopy
M. Kurosawa[1,2], T. Sadoh[1] and M. Miyao[1], [1]Kyushu Univ. and [2]JSPS (Japan)
We have newly developed a polarized Raman spectroscopy technique, which uses special polarization configurations of the incident and scattered light. This enables the evaluation of strain axis distributions in SOI structures for the first time. This technique is a powerful tool to optimize the strained SOI micro-structures of the advanced LSIs.

1F 213

C-9: Emerging Device Technology (Area 3)

17:00 C-9-5 (Late News)
Short-Channel Junctionless Nanowire Transistors
C. W. Lee, I. Ferain, A. Kranti, N. Dehdashti Akhavan, P. Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, S. Gheorghe, R. Murphy and J. P. Colinge, Univ. College Cork (Ireland)
Junctionless silicon nanowire transistors with a gate length down to 50 nm have been demonstrated. The devices show very small short-channel effects: SS=60mV/dec, DIBL=7mV.

2F 221

D-9: Si Photonics (2) (Area 7)

16:30 D-9-5
Development of Accelerometer Using Mach-Zehnder Interferometer Type Optical Waveguide
M. Suzuki[1], K. Nishioka[1], T. Takahashi[1], S. Aoyagi[1], Y. Amemiya[2], M. Fukuyama[2] and S. Yokoyama[2], [1]Kansai Univ. and [2]Hiroshima Univ. (Japan)
A novel inertial force sensor which uses a Mach-Zehnder Interferometer (MZI) type optical waveguide made of crystal silicon is developed. In this sensor, one branched waveguide of the MZI have floating beam structure which is formed by removal of its underlying SiO2 layer.

16:45 D-9-6
10-GHz Operation of a PLZT Electro-Optic Modulator with a Ring Resonator Formed on a Silicon Substrate
T. Shimizu[1,2], M. Nakada[1], H. Tsuda[3], H. Miyazaki[1], J. Akedo[3] and K. Ohashi[1,2], [1]MIRAI-Selete, [2]NEC Corp. and [3]AIST (Japan)
We developed a PLZT electro-optic modulator with a ring resonator formed on silicon substrate by aerosol deposition. A 10-GHz optical output signal was produced by the modulator with a resonator size of 150x190 micron.

17:00 D-9-7
Crosstalk inprovement in Si-wire optical cross-bar switch
H. Kawashima, Y. Shoji, K. Kintaka, S. Suda, T. Hasama and H. Ishikawa, AIST (Japan)
Improvement of crosstalk by cascading Si-wire cross-bar switches is demonstrated. Achieved lowest crosstalk is -50 dB for the bar state and is -30 dB for the cross state. We discuss on the limiting factors.

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E-9: ReRAM (Area 4:)

17:00 E-9-5 (Late News)
Novel Low Power RRAM with a U-type Cell Structure for Improving Resistive Switching Characteristics
K. C. Ryoo[1,2], J. H. Oh[1,2], S. Jung[1], H. Jeong[2] and B. G. Park[1], [1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)
We propose a novel RRAM structure which makes it possible to reduce the reset current by controlling the number of the electrical path. Numerical simulation is also performed to investigate the optimal process condition.

4F 242

F-9: Spintronics (Ⅳ)- Device and Circuits - (Area 12)

16:45 F-9-5 (Late News)
Magnetic Field Dependence of Quadrupoar Splitting and Nuclear Spin Coherence in a (110) GaAs/AlGaAs Quantum Well
J. Ishihara, M. Ono, G. Sato, S. Matsuzaka, Y. Ohno and H. Ohno, Tohoku Univ. (Japan)
We investigated magnetic field dependences of quadrupoar splitting in the NMR spectrum, the nuclear decoherence time, and the dephasing time involving the inhomogeneous broadening in a (110) GaAs quantum well (QW).

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G-9: Nanomaterial Applications (Area 11)	H-9: Image Sensor (Area 2)	I-9: Crystulline and Thin Film Silicon Solar Cell (Ⅱ) (Area 14)			