POSTER SESSION (13:15-14:45, Takeda Bldg.)

Area 1: Advanced Si Processing & Materials Science

P-1-1 Strained Si with Smooth and Uniformly Strained Surface Formed by Sputter Epitaxy

H. Hanafusa¹, N. Hirose², A. Kasamatsu³, T. Mimura², T. Matsu², H. M. H. Chong³, H. Mizuta³ and Y. Suda¹, ¹Tokyo Univ. of Agri. And Tech., ²National Inst. of Info. and Commun. Tech. and ³Univ. of Southampton (Japan)

Strained Si formed by our sputter epitaxy shows a smoother and more uniformly strained surface than with GS-MBE, which has been first clarified on the nanometer scale with a combination of AFM and Enhanced-Raman Spectroscopy.

P-1-2

Enhancement of Stress Memorization Technique (SMT) by High Thermal Annealing Temperature

H. Y. Chang and J. C. S. Woo, University of California, Los Angeles (USA)

In this paper, different annealing temperature at gate memorizing strain step is studied. Device performance shows SMT device with higher annealing temperature (1150°C) can induce more strain memorized in the gate. The experimental data of SMT device with higher annealing temperature shows significant improvement of electron mobility compared to lower annealing temperature (100°C).

P-1-3

$\label{eq:static} Evaluation \ of Si/SiO_2 \ Interface \ Properties \ for \ CMOS \ Fabricated \ on \ Hybrid \ Orientation \ Substrate \ with \ Amorphization/Templated \ Recrystallization \ Method$

P. C. Huang¹, S. L. Wu², S. J. Chang¹, J. F. Chen¹, Y. T. Huang¹, D. G. Hong², C. Y. Chang¹, C. Y. Wu², C. T. Lin³, M. Ma³ and O. Cheng³, ¹National Cheng Kung Univ., ²Cheng Shiu Univ. and ³UMC (Taiwan)

For the HOT substrates, we find that ATR-induced defects on (100) regions can be repaired further by extending defect-removal annealing time, and no appreciable impact on (110) regions is observed.

P-1-4

Efficient Activation of As in Ultrashallow Junction Induced by Thermal Plasma Jet Microsecond Annealing

K. Matsumoto, S. Higashi, H. Murakami and S. Miyazaki, Hiroshima Univ. (Japan) We carried out generation of high power density TPJ for microsecond RTA by using an orifice of 0.8 mm diameter instead of 2.0 mm to concentrate TPJ and could be annealing a range of microsecond annealing. We activated As in Si wafers by this annealing technique using µ-TPJ and could be efficient activation of As in comparison to TPJ irradiation.

P-1-5

Depth Profile and Retained Dose in SiO₂/Si Structure for B₁₈H_X⁺ Implantation

Y. Kawasaki^{1,2}, H. Yoshimura¹, K. Asai¹ and K. Shibahara², ¹Renesas Electronics Corp. and ²Hiroshima Univ. (Japan)

Retained dose for $B_{u_1H_X}$ implantation and surface sputtering was investigated. The surface sputtering was negligible for both SiO₂ and Si. However the retained boron dose remarkably decreased due to the surface SiO₂.

P-1-6

Effects of Al Incorporation into Pr-oxides Formed by Atomic Layer Deposition

K. Furuta, W. Takeuchi, M. Sakashita, K. Kato, H. Kondo, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan)

We examined PAO layers on Si substrates with ALD method and investigated the crystalline and electric properties. The oxide trap density and interface state density decrease by incorporation of Al into Pr oxide.

P-1-7

Analysis of Local Leakage Current of Pr Oxide Thin Films with Conductive Atomic Force Microscopy

M. Adachi, M. Sakashita, H. Kondo, W. Takeuchi, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan) We have investigated local leakage current in Pr oxide films by using C-AFM. We considered that leakage spots observed in C-AFM current images is strongly related to oxygen vacancy in the Pr oxide films.

P-1-8

In-situ Formation of HfN/HfSiON Gate Stacks with 0.5 nm EOT Utilizing ECR Sputtering on Three-Dimensional Si Structures

T. Sano and S. Ohmi, Tokyo Tech (Japan)

In-situ formation of HfN/HfSiON gate stacks by ECR sputtering was investigated. Annealing temperature was important parameter and the temperature of 600°C is suitable to suppress the D_{α} and the frequency dispersion.

P-1-9

(26 Papers)

The Influence of La and Zr Doping on TDDB Characteristics of HfO2 Thin Films

H. W. Chen¹, C. H. Liu², S. Y. Chen¹, Y. W. Liao¹, H. W. Hsu¹, H. S. Huang¹ and L. W. Cheng³, ¹National Taipei Univ. of Tech., ²National Taiwan Normal Univ. and ³UMC (Taiwan) Although time-dependent-dielectric-breakdown (TDDB) reliability is one major concern in advanced

Thursday, September 23

Attnoigh time-dependent-detectric-oreakdown (TDDB) remainity is one major concern in advanced technology, it has not yet been fully understood for Hf-based high- κ dielectrics, especially La-incorporated HfZrO2 (HfZrLaO) thin films.

P-1-10

Temperature Dependence of Exclusive SiO₂Formation during Thermal Oxidation of Si_{1-X} Ge_x Alloy Layer on Si(001) Surfaces

H. Hozumi¹, S. Ogawa¹, A. Yoshigoe², S. Ishidzuka³, J. R. Harries² and Y. Teraoka², Y. Takakuwa¹, ¹Tohoku Univ., ²JAEA and ³Akita Nat. Col. Tech. (Japan)

Qpix v.1 possesses 400 pixels and compact readout structure to guarantee that all stored data in the pixels can be read out in 2.6 µs in parallel mode and 54 µs in serial mode. A charge collection pad is included in each pixel to realize large area applications. The SAR ADC in each pixel is optimized to 10 bit 10 MSps without area increase. The power consumption has been reduced to 187.5 µW/pixel.

P-1-11

Fabrication of Ge-MOS Capacitors with High-Quality Interface by Ultra-Thin $\rm SiO_2/GeO_2$ Bi-Layer Passivation

K. Hirayama, R. Ueno, Y. Iwamura, K. Yoshino, D. Wang, H. Yang and H. Nakashima, Kyushu Univ. (Japan)

We established an effective electrical passivation method of Ge surface by ultra-thin SiO 2/GeO = 2 bi-layer. By using this method, we achieved the density of interface states of 3.7×10^{11} cm² eV¹ at around midgap for MOS capacitors.

P-1-12

Improvement of The Property of FET Having The HfO₂/Ge Structure Fabricated by Photo-Assisted MOCVD with Fluorine Treatment

D. Lee, H. Imajo, T. Kanashima and M. Okuyama, Osaka Univ. (Japan)

This paper describes about improvement of The HfO₂/Ge MISFET device by fluorine treatment. The device was treated by F_2 gas before each HfO₂ deposition on the few bottom layers. Therefore, we were able to fabricate a high speed Ge-based MISFET device.

P-1-13

Study on Native Oxidation of Ge (111) and (100) Surfaces

S. K. Sahari, H. Murakami, T. Fujioka, T. Bando, A. Ohta, K. Makihara, S. Higashi and S. Miyazaki, Hiroshima Univ. (Japan)

We have studied the growth of native oxides on HCl-last and HF-last Ge surfaces and examined the influence of crystallographic orientation and conduction type on the native oxidation.

P-1-14

Annealing Effects on Ge/SiO_2 interface Structure in wafer-bonded germanium-on-insulator substrates

O. Yoshitake¹, J. Kikkawa¹, Y. Nakamura¹, A. Sakai¹, E. Toyoda², H. Isogai² and K. Izunome², ¹Osaka Univ. and ²Covalent Silicon Co., Ltd. (Japan)

We have investigated annealing effects on Ge/SiO² interfaces in wafer-bonded Germanium (Ge) on Insulator (GOI) substrates using transmission electron microscopy and electron energy-loss spectroscopy.

P-1-15

Electrical characterization of wafer-bonded germanium-on-insulator substrates using a fourpoint-probe pseudo-MOSFET

Y. Iwasaki¹, Y. Nakamura¹, J. Kikkawa¹, A. Sakai¹, M. Sato², E. Toyoda², H. Isogai² and K. Izunome², ¹Osaka Univ. and ²Covalent Silicon Co., Ltd. (Japan)

The electrical characteristics of wafer-bonded GOI substrates were investigated using a pseudo-MOSFET. Annealing process in vacuum strongly influenced their electrical characteristics, which is explained by defect-induced energy band bending near the interface.

P-1-16

New Concept of Plasma-induced Damage in MNOS FET during Thick Dielectric Film Etching Using Fluorocarbon Gas Plasma

Y. Ichihashi, Y. Ishikawa and S. Samukawa, Tohoku Univ. (Japan)

We investigated the mechanism of damage by perfluorocarbon gas plasma. We found that charged carriers in SiO2 film were generated by UV irradiation of CF4 plasma and were trapped at Si dangling bonds.

P-1-17

A Novel Hot DI Water Rinse on SOD Filled Self-Aligned Shallow Trench Isolation for Highly Reliable NAND Flash Memory

C. H. Liu, Y. M. Lin, R. T. Peng, H. C. Wei, H. J. Chien, Y. T. Chiu, L. T. Kuo, H. P. Hwang, M. S. Lee and S. Pittikoun, Powerchip Semiconductor Corp. (Taiwan)

Significant improvements on 42nm node NAND flash memory with SOD filled STI by hot deionized water rinse technology: (1) Most good block ratio can be increased > 15%. (2)Better endurance/ retention: 0.37V less cell Vth shift after 10k cycling and 36.7% less Vt shift by retention test. (2) Stress induced leakage current life time is extended 54%.

P-1-18

High-Performance Poly-Si TFTs with Novel FinFet-like Channel

Y. H. Lue, P. Y. Kuo, Y. H. Wu and T. S. Chao, National Chiao Tung Univ. (Taiwan) High performance TFTs with novel FinFet-like channel structure (called FL-TFTs) exhibit VTH-0.5V, good S.S.~ 240mV/dec. and high Iratio>107 without any hydrogen-related plasma treatments. Nisalicidation and hydrogen-related plasma treatments further enhance S.S. to 190 mV/dec. and Iratio>108.

P-1-19

Fluorescence XAFS analysis of thermal stability for Ru/HfSiON/SiON/Si gate stack structure H. Ofuchi¹, H. Kamada², S. Toyoda^{23,4}, H. Kumigashira^{23,4}, T. Sukegawa⁵, K. Iwamoto⁵, Z. Liu⁵ and M.

Dishima^{23,4}, ¹JASRI, ¹Univ. of Tokyo, ⁴UT-SRRO, ¹JST-CREST and ¹STARC (Japan) Thermal stability of geometric structures for Ru/HISiON/SiON/Si films was investigated by fluorescence XAFS. The XAFS analysis has revealed that the appropriate annealing condition prevent the oxidation and silicidation of the metal gate Ru laver.

P-1-20

Strain and stress tensor evaluation in global and local strained-Si by electron back scattering pattern

M. Tomita¹, D. Kosemura^{1,2}, M. Takei¹, K. Nagata¹, H. Akamatsu¹ and A. Ogura¹, ¹Meiji Univ. and ²Research Fellow of the JSPS (Japan)

SSOI and Si substrates with patterned SiN films were evaluated by EBSP. Shear stresses were observed in both of the samples. Clear two-dimensional stress distribution was obtained, which was comparable to that obtained by UV-Raman.

P-1-21

Development of an STM simulator for quantitative dopant profiling

M. Nishizawa^{1,2}, L. Bolotov², T. Tada^{1,2}, H. Fukutome², H. Arimoto² and T. Kanayama^{1,2}, ¹MIRAI-AIST and ²NIRC-AIST (Japan)

In order to realize quantitative dopant profiling by STM, we developed an STM simulator. Our simulation reproduced the experimental topographic profile and I-V curves obtained at a p-n junction.

P-1-22 (Late News)

Many-electron charge transfer multiplet theory: O-atom vacancies in high-k dielectrics G. Lucovsky, L. Miotti and K. Paz Bastos, North Carolina State Univ (USA)

Soft X-ray absorption and photoemission spectroscopies (XAS and XPES) have been used to study conduction band edge, and O-vacancy defect states in Hf02. The d-state occupancy in O-vacancy d² defects is described Tanabe-Sugano diagrams for d to d' transitions for the excited states of these defects, as well as the negative ion states which act as electron traps

P-1-23 (Late News)

Momentum Transfer Implantation for Sidewall Doping of FinFET's

G. Fuse¹, M. Sugitani¹, H. Matsushita¹, H. Murooka¹, M. Kuriyama² and M. Tanaka², ¹SEN corporation and ²Sumitomo Heavy Industry (Japan)

As new doping technique into FinFET sidewalls, Momentum Transfer Implantation (MTI) is introduced. MTI consists of two processes; dopant film deposition and grazing angle implantation by heavy ions. Simulation and experiment results will be reported.

P-1-24 (Late News)

MIM Capacitors with Stacked TiO₂/Y₂O₃ Insulator Featuring High Capacitance Density and Low Leakage Current

C. C. Lin, Y. C. Hu, L. L. Chen, M. L. Wu, J. R. Wu and Y. H. Wu, National Tsing Hua Univ. (Taiwan) High-x dielectrics have been perceived as the enabling technology to implement high performance radio frequency and analog metal-insulator-metal (MIM) capacitors. Applications of HfO2 and ZrO2based materials to MIM capacitors have been extensively studied.

P-1-25 (Late News)

Fabrication of hp 25nm Si Pillar Using New Multiple Double Patterning Technique

M. Kushibiki^{1,4}, A. Hara^{2,4}, E. Nishimura^{1,4} and T. Endoh^{3,4}, ¹Tokyo Electron AT Ltd., ²Tokyo Electron Ltd., ³Tohoku Univ. and ⁴JST-CREST (Japan)

Novel method to fabricate hp 25nm pitch dense Si pillar that would apply to the fabrication of vertical cell devices was developed. By using proposed multiple double patterning technique, the hp25 Si pillar etching profile has enough uniformity in 300mm wafer.

P-1-26 (Late News)

Effect of Valence State of Pr on Interfacial Structure and Electrical Properties of Pr-oxide/ PrON/Ge Gate Stack Structure

K. Kato, M. Sakashita, W. Takeuchi, H. Kondo, O. Nakatsuka and S. Zaima, Nagoya Univ. (Japan) We investigated the relationship between the electrical properties and the valence state of Pr in AlProxide/PrON/Ge stacked structures, and discussed the importance of controlling the chemical bonding structure to suppress degradation of MOS characteristics.

Area 2: Advanced Interconnect /3-D Integration Science (10 Papers)

P-2-1

Development of Versatile Backside Via Technology for 3D System on Chip

Y. Ohara, K. Lee, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. Japan) We develop several key technologies in backside via to realize 3D LSIs. We apply them to a test chip with daisy chain. Fine sized Cu TSVs in diameter 10 µm and 30 µm depth are successfully formed.

P-2-2

RF Modeling of Through Silicon Vias (TSVs) in 3D IC

C. W. Luo, Y. C. Wu and J. Y. Wang and S. S. H. Hsu, National Tsing Hua Univ. (Taiwan) This paper proposed the TSV one-port test structures to extract the physical-based equivalent circuit model. The differences of S21 and S11 between the EM-simulation and the model are smaller than 0.03 dB and 2 dB.

P-2-3

Stress Mapping of Silicon Surrounded by Various Through Silicon Via (TSV) Patterns using Polychromator-Based Multi-Wavelength Raman Spectroscopy

A. D. Trigg¹, L. H. Yu¹, C. C. Kuo¹, R. Kumar¹, D. L. Kwong¹, T. Ueda², T. Ishigaki², K. Kang² and W. S. Yoo², 'Institute of Microelectronics and ²WaferMasters, Inc. (Singapore) We have studied the stress distribution in Si surrounded by TSVs, with various dimensions and pitches, to understand the potential impact of TSV layouts on device performance and reliability. The stress measurement and 3D stress mapping was successfully demonstrated using a polychromator-based, multi-wavelength Raman spectroscopy (MRS-300) system.

P-2-4

Above-CMOS Metal-Pattern Technique for Flexible Inductance Adjustment in Rapid Prototyping of RF SoCs

K. Kotani, A. Sugimoto, Y. Omiya and T. Ito, Tohoku Univ. (Japan)

Very simple yet flexible inductance adjustment scheme has been developed using above-CMOS metal pattern formation for rapid prototyping of RF SoCs. Above-CMOS simple processing with chip-bychip manner can both increase and decrease the on-chip inductances.

P-2-5

Modeling and Co-Design of Novel Packaging Interposer with IPD Layers

S. M. Wu¹, T. Y. Wu¹, B. H. Yu¹ and C. C. Wang⁷, ¹National Univ. of Kaohsiung and ²Electrical Lab., Corp. Design Division, Corporate R&D, Advanced Semiconductor Engineering (ASE) Inc., Kaohsiung (Taiwan)

Two innovations topics will be presented in this research. First, structure of packaging interposer with IPD layers is proposed and broad-band equivalent model of TSV will be extracted too. Second, codesign case, coplanar waveguide transfer layers from top to bottom by TSV, is simulated by equivalent model we performed and compared with full wave EM simulation.

P-2-6

Multi-Line De-Embedding Technique for Millimeter-Wave Circuit Design

Q. H. Bu, N. Li, N. Takayama, K. Okada and A. Matsuzawa, Tokyo Tech (Japan) A multi-line de-embedding method has been proposed up to millimeter wave. The de-embedding procedure is explained in the paper. Experimental results using the proposed method is shown.

P-2-7

Numerical Simulation of Organic Low-k Etching in H₂/N₂ Plasma

T: Yagisawa' and T: Makabe¹, Keio Univ. (Japan) Organic low-k material is one of the promising solutions for RC signal delay problem in the multilayer interconnect. The characteristics of organic low-k film by using H₂/N₂ plasma has been numerically investigated.

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P-2-8

Smooth Patterning of Ru Film by Electrochemical Etching using Organic based Solution

L. Yang¹, R. Sakae¹, M. Yashimaru², M. Yamaguchi², I. Kanno², M. Tanaka², C. Kimura¹ and H. Aoki¹, ¹Osaka Univ. and ²STARC (Japan)

In this paper, to avoid the bubbles generation and having smooth etching area, we have proposed an etching of Ru film using electrochemical etching in the organic based solution.

P-2-9

Effect of Annealing on Electrical Properties of Networked-Nanographite Wire Grown by Metal-Photoemission-assisted Plasma-enhanced CVD

M. Sato^{1,23}, S. Ogava^{3,4}, T. Kaga⁴, E. Ikenaga^{3,5}, Y. Takakuwa^{3,4}, M. Nihei and N. Yokoyama², ¹Fujitsu Ltd., ²Fujitsu Labs Ltd., ³CREST-JST, ⁴Tohoku Univ. and ³JASRI (Japan)

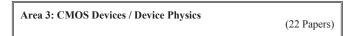
The annealing effect on the electrical properties of networked-nanographite (NNG) wires has been investigated using a TEM, Raman spectroscopy and resistivity measurement. The resistivity of NNG decreases as the annealing temperature increases.

P-2-10

In Situ High-Resolution Transmission Electron Microscopy of Electromigration in Silver Nanocontacts

H. Masuda and T. Kizuka, Univ. of Tsukuba (Japan)

EM in Ag NCs was directly observed by in situ TEM. The relationships between the structural modification, current density and stress were simultaneously analyzed. The threshold bias voltage was ~100 mV. In this experiment, we in situ observed the thinning process of the NCs.



P-3-1

Experimental Investigations on Ballistic Transport in Multi-Bridged Channel Field Effect Transistors (MBCFETs)

Y. C. Jung¹, B. H. Hong¹, L. Choi¹, S. W. Hwang¹, K. H. Cho², S. Y. Lee², D. W. Kim², G. Y. Jin² and K. S. Oh², ¹Korea Univ. and ²Samsung Electronics Co., Ltd. (Korea)

We present the experimental evidences of ballistic transport in MBCFET by investigating the device characteristics as a function of the gate length ranging from 48 to 500nm and temperature ranging from 300 to 4K.

P-3-2

The Effects of Quantum Confinement on Electrical Characteristics of 12-nm Silicon-on-Insulator (SOI) FinFETs by Quantum Transport Analysis

K. M. Liu, National Dong Hua Univ. (Taiwan)

The quantum confinement effects on the electrical characteristics of 12-nm SOI FinFETs are simulated and discussed by an in-house quantum transport simulator. Both the ballistic limit and the scattering effects are examined.

P-3-3

Technology Computer Aided Design of 65nm SOI MOSFETs through Integrated Process and Device Simulations

E. M. Bazizi¹², P. F. Fazzini¹, F. Cristiano¹, A. Pakfar², C. Tavernier², C. Zechner³, N. Zographos³ and A. Claverie¹, ¹CNRS-LAAS, ²STMicroelectronics, ³Synopsys Switzerland LLC and ⁴CEMES/CNRS (France)

Integrated process and device simulations were performed within a unique simulation tool to predict sub-65nm SOI device performance. Physically based process models were used to reproduce successfully the electrical characteristics of SOI devices

P-3-5

The Observation of the Random Dopant Fluctuation in Strained-SOI Devices

C. Y. Cheng¹, E. R. Hsieh¹, S. S. Chung⁷, R. M. Huang², Y. H. Lin², C. T. Tsai², G. H. Ma² and C. W. Liang², ¹National Chiao Tung Univ. and ²UMC (Taiwan)

The device performance and Vth variation of the MOS devices on the SOI and strained-SOI (SSOI) have been examined. For SSOIs, it shows the expected drain current enhancement and smaller $B_{\rm VT}$ than SOI ones. Furthermore, SSOIs exhibit a weak dependence of V_{th} variation on the drain bias as a result of the strain effect.

P-3-7

InGaAs and InGaAs-On-Insulator *n*-Channel MOSFETs Fabricated by Self-Align Gate First Process with Ni/Al,O, Gate Stacks

S. Lee¹, R. Iida¹, S. H. Kim¹, M. Yokoyama¹, N. Taoka¹, Y. Urabe², T. Yasuda², H. Takagi², H. Ishii², N. Miyata², H. Yamada³, N. Fukuhara³, M. Hata³, M. Takenaka¹ and S. Takagi¹, ¹Univ. of Tokyo, ²NAIST and ³Sumitomo Chemical Co., Ltd. (Japan)

We demonstrated self-align gate first InGaAs-on-insulator MOSFETs on Si substrates, fabricated by direct wafer bonding, for the first time. We found that III-V-on-insulator structure is a quite promising MOS structure for future technology nodes.

P-3-9

Characterization of Tunneling Resistance in Vertical Tunneling FETs

A. Tura and J. C. S. Woo, Univ. of California, Los Angeles (USA)

In this paper, the tunneling resistances of vertical p-i-n and p-n-p-n source tunneling nMOSFETs are experimentally investigated at different temperatures and gate voltages. Results show significant tunneling resistance reduction due to the n-type dopant pocket.

P-3-10

Improvement of High-k/metal gate pMOSFET performances and reliability with optimism Si cap/SiGe channel structure

C. W. Hsu¹, Y. K. Fang¹, C. Y. Chen¹, W. K. Yeh², C. T. Lin³ and P. Y. Chen⁴, ¹National Cheng Kung Univ, ²National Univ. of Kaohsiung, ³UMC and ⁴I-Shou Univ. (Taiwan)

The Hf-based high-k/metal gate SiGe pMOSFET with an optimism channel stack ratio has low V_{th} [~-0.3V] and C-V hysteresis (< 5mV), superior Ion-Ioff, and V_{th} roll-off. Besides, it achieves good NBTI and HCI reliability.

P-3-12

Development of a Multi-Scale Time Dependent Dielectric Breakdown Simulator Based on TBQC and KMC Method: Application to the Evaluation of a Gate Oxide Film for CMOS Technology

H. Tsuboi, K. Inaba, Y. Hayashi, H. Sato, Y. Obara, Y. Suzuki, T. Miyagawa, S. Nakamura, R. Nagumo, R. Miura, A. Suzuki, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)

We have succeeded in the development of a new multi-scale time dependent dielectric breakdown simulator using kinetic Monte Carlo method considering impact ionization, together with a tightbinding quantum chemical calculation to evaluate the trap depth.

P-3-13

Investigation of Low-Cost Stress Memorization Process on Layout and Low-Frequency Noise Performance for Strained-Si nMOSFETs

C. W. Kuo¹, S. L. Wu², H. Y. Lin¹, Y. T. Huang¹, S. J. Chang¹, D. G. Hong², C. Y. Wu², Y. C. Cheng³ and O. Cheng³, ¹National Cheng Kung Univ., ²Cheng Shiu Univ. and ³UMC (Taiwan) Impact of low-cost stress-memorization technique (SMT) on layout and low frequency noise of nMOSFETs performance is investigated. The DC characteristics of SMT device become more sensitive to the layout as the device is scaled down. Moreover, both devices show comparable noise level, indicating the SMT process will not degrade interface quality.

P-3-14

Characterization the random telegraph noise in 32nm high-k/metal gate CMOSFETs

W. K.Yeh¹, C. W. Hsu², Y. K. Fang², C. Y. Chen¹, C. T. Lin³ and P. Y. Chen⁴, ¹National Univ. of Kaohsiung, ²National Cheng Kung Univ., ³UMC and ⁴I-Shou Univ. (Taiwan) We find that the RTN fluctuation (Δ I₀) in nMOSFETs is larger than it in pMOSFETs, especially with during continuous during the startistic starting of the st

device scaling down. Drain current instability in 32nm generation and beyond should be considered more carefully for nMOSFETs.

P-3-15

Low-Frequency Noise Behavior of La-Doped Hf-Based Dielectric nMOSFETs

D. Y. Choi¹, C. W. Sohn¹, H. C. Sagong¹, M. S. Park¹, K. T. Lee¹, R. H. Baek¹, C. Y. Kang² and Y. H. Jeong¹, ¹POSTECH and ²SEMATECH (Korea)

We investigated the low-frequency noise behavior of nMOSFETs with La-doped Hf-based gate dielectrics. They showed enhanced contribution of mobility fluctuation compared to the nMOSFETs without La.

P-3-16

The Compact Modeling of Zero Temperature Coefficient (ZTC) Point of DTMOS

K. T. Wang, W. C. Lin and T. S. Chao, National Chiao Tung Univ. (Taiwan) For the first time, the compact analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. Newly analytical formulations are developed for both linear and saturation regions of DTMOS transistor operation.

P-3-17

A Simple Model for Threshold Voltage of Surrounding-gate MOSFETs With Interface Trapped Charges

T. K. Chiang, J. F. Lai and M. J. Yang, National Univ. of Kaohsiung (Taiwan)

Based on perimeter-weighted-sum method and scaling theory, a simple threshold voltage model for surrounding -gate MOSFETs with interface trapped charges is developed by considering the effects of equivalent oxide charges on the flat-band voltage. The model shows how various charge conditions and device structure parameters affect the threshold voltage behavior. The model is verified by the device simulator and can be efficiently used to explore the hot-carrier-induced threshold voltage degradation of the charge-trapped memory device.

P-3-18

A Forward Body Bias Characterization for Low Voltage CMOS Circuits

H. Aoki¹, M. Shimasue¹, M. Miyahara² and A. Matsuzawa⁷, ¹MODECH Inc. and ²Tokyo Tech (Japan) This paper proposes a modified transistor model to improve the accuracy under the forward body bias operation that is vital for low voltage circuits to reduce the power consumption of CMOS LSI.

P-3-19

Investigation of Illuminated High-Frequency Capacitance-Voltage Response in Deep Depletion of HfO₂ and SiO₂ MOS Capacitors with Ultra-thin Gate Oxides

J. Y. Cheng and J. G. Hwu, National Taiwan Univ. (Taiwan)

The correlation between illuminated C-V response and deep depletion was demonstrated in MOS structure via local depletion capacitance model. The smaller initiation voltage (0.12V) of deep depletion in HfO2 is observed from magnified C-V curves and the non-uniform area ratio increases in MOS device after the illumination was also investigated.

P-3-21

Investigation of SACVD-Based STI Process on Electrical Characteristics of Nanoscale NMOS-FETs

H. Y. Lin¹, S. L. Wu², C. W. Kuo¹, Y. T. Huang¹, S. J. Chang¹, D. G. Hong², C. Y. Wu², C. T. Huang³ and O. Cheng³, ¹National Cheng Kung Univ., ²Cheng Shiu Univ. and ³United Microelectronics Corp. (Taiwan)

Based on a detailed physical and electrical analysis, we have demonstrated that an improved densification anneal process of Sub-Atmospheric Chemical Vapor Deposition (SACVD)-based STI process to enhance NMOSFETs performance can be used in 40-nm node and beyond. Moreover, it would not affect on active gate oxide edge reliability for devices.

P-3-22

Calibration of Linear Piezo Resistance Coefficients using 3-Dimensional Stress Simulation of Si-MOSFETs Structures

A. Satoh¹, T. Tada¹, V. Poborchii¹, T. Kanayama¹, S. Satoh² and H. Arimoto¹, ¹AIST and ²Fujitsu Semiconductor Ltd. (Japan)

The linear Piezo resistance model was calibrated using stress tensor by a well calibrated 3-dimensional stress simulation. By using of precise stress distribution in channel region of Si-MOSFET, the calibrated mobility model could predict mobility dependencies on layout parameters of Si-MOSFET.

P-3-23

Investigation of Different Capping Layers and Strain Sources for SMT Process

C. C. Liao, M. C. Lin and T. S. Chao, National Chiao Tung Univ. (Taiwan)

The compressive nitride is a promising technique for strain coupling, gate leakage, and hot carrier immunity concern for SMT application. The mechanisms of strain source and hydrogen diffusion are also clarified.

P-3-24

X-Ray Radiation Effects on CMOS Image Sensor In-Pixel Devices

J. Tan¹, B. Buttgen¹ and A. J. P. Theuwissen^{1,2}, ¹Delft Univ. of Tech. and ²Harvest Imaging (the Netherlands)

This paper presents new results of radiation-induced degradation on 4-Transistor CMOS Image Sensor In-Pixel devices with the pinned photodiode and transfer-gate transistor due to the interface trap generation and trapped charges in the shallow trench isolation oxide during the radiation damage.

P-3-25

High-Performance (S. S.<100 mV/dec) Poly-Si TFTs with Laser Annealed Channel and High- κ Metal-Gate on Glass Substrate

Y. H. Lue¹, C. H. Chien¹, P. Y. Kuo¹, M. J. Yang¹, H. Y. Lin² and T. S. Chao¹, ¹National Chiao Tung Univ. and ²Toppoly Optoelectronics Corp. (Taiwan)

We demonstrate high performance LTPS-TFTs with a TaN/HfO2 and laser-annealed channel to combine glass substrate (called GSHM-TFTs). The GSHM-TFTs exhibit a low V_{TH}, steep S.S.~95, 154mV/dec. and high Iratio>10⁷, 10⁸ for N and P channel, respectively. The impact of grain boundaries in poly-Si is also investigated.

Thursday, September 23

P-3-26 (Late News)

Electron and hole mobility comparison in a single Ge-MOSFET fabricated on 50 nm-thick GeOI substrate

D. D. Zhao¹, C. H. Lee¹, T. Nishimura^{1,2}, K. Nagashio^{1,2}, K. Kita^{1,2} and A. Toriumi^{1,2}, ¹Univ. of Tokyo and ²JST-CREST (Japan)

We show a direct comparison of electron mobility with hole one in a single MOSFET fabricated on 50 nm-thick low-doped GeOI by using the modified double Lm method.

P-3-27 (Late News)

Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16-nm CMOS Devices

Y. Li^{1,2}, C. H. Yu¹, M. H. Han¹ and H. W. Cheng¹, ¹National Chiao Tung Univ. and ²National Nano Device Labs. (Taiwan)

We estimate metal-gate-work-function fluctuations using full 3D device simulation which is different from the result of averaged work-function method due to localized random work-functions. Effects of number and position for different grain orientation are analyzed.

Area 4: Advanced Memory Technology

(10 Papers)

P-4-1

Impedance analysis of controlled-polarization-type ferroelectric-gate TFT using RC distributed constant circuit

T. Fukushima, K. Maeda, T. Yoshimura, A. Ashida and N. Fujimura, Osaka Prefecture Univ. (Japan) By using RC-distribution-constant-circuit, it was analyzed that the reversal of PSFe in ferroelectricgate TFT was occurred only at the region near the source electrode by negative VG, and entire channel region by positive VG.

P-4-2

Effect of MIM type selection device on readout margin of cross-point bipolar ReRAM

J. Shin, I. Kim, J. Park, J. Lee, M. Jo, K. P. Biju, S. Jung, W. Lee, S. Kim, S. Park, D. Lee and H. Hwang, Gwangju Inst. of Sci. and Tech. (Korea)

We investigated an MIM type selection device that can alleviate the cross-talk effect in cross-point arrays. Also, a readout margin was analyzed depending on the memory size and an existence of a selection device.

P-4-3

One-Diode-One-Resistor Titanium-Oxide RRAM Fabricated at Room Temperature

C. W. Kuo, J. J. Huang, W. C. Chang and T. H. Hou, National Chiao Tung Univ. (Taiwan) A nonpolar Pt/TiO2/Pt RRAM and a high forward-current Ti/TiO2/Pt oxide diode are realized using identical TiO2 by room-temperature evaporation. Excellent characteristics are reported for the individual diode, RRAM, and diode / RRAM in series.

P-4-4

Improved Resistive Switching Uniformity of a Bilayer TiO₂ Films

I. Kim, S. Jung, J. Shin, K. P. Biju, K. Seo, M. Siddik, X. J. Liu, J. Kong, K. Lee and H. Hwang, Gwangju Inst. of Sci.and Tech. (Korea)

We investigated the resistive switching properties of bilayer TiO2 films. To solve inferior electrical problems of sol-gel process, we deposited additional thin ALD TiO2 layer. Also, switching mechanism is suggested based on exchange oxygen ions.

P-4-5

Miniaturization Limit of Memory Cell in Polycrystalline-NiO-ReRAM

K. Dobashi¹, K. Kinoshita^{1,2}, T. Yoda¹ and S. Kishida^{1,2}, ¹Tottori Univ. and ²Tottori Univ. Electronic Display Research Center (Japan)

Localized current distributions of polycrystalline NiO films were investigated by using C-AFM. It was suggested the minimum unit to generate the resistance change effect of polycrystalline NiO films was one crystal grain.

P-4-6

The observation of "Conduction Spot" on NiO resistance RAM

T. Fujii¹, H. Kondo¹, H. Kaji¹, M. Arita¹, M. Moniwa², T. Yamaguchi², I. Fujiwara², M. Yoshimaru² and Y. Takahashi¹, ¹Hokkaido Univ. and ²STARC (Japan)

We successfully demonstrate and observe the conduction spot (CS) which includes filamentary path. The CS size can be controlled. The results suggest NiO ReRAM device size will be reduced by reducing the forming power.

P-4-7

Impact of Engineered Buried Ti layer on the Memory Performance of HfOx RRAM

P. Š. Chen¹, H. Y. Lee²³, Y. S. Chen²³, P. Y. Gu², F. Chen⁵ and M. J. Tsai², ¹MingShin University of Science & Technology, ²Indus. Tech. Res. Inst. and ³National Tsing Hua Univ. (Taiwan) Impact of engineered Ti layer on the memory performance of 5-nm-thick HfOx RRAM devices are investigated. Two stacked layer, consisted of Ti/HfOx/TiN and TiN/HfOx/Ti, were prepared. With a Ti of 10 nm, more oxygen atoms in HfOx films are captured during the capping of Ti overlayer.

P-4-8

High Efficiency Charge Storage Layer for MLC NAND Non-Volatile Memory

S. H. Liu¹, W. L. Yang¹, C. W. Chiu¹ and T. S. Chao², ¹Feng Chia Univ. and ²National Chiao Tung Univ. (Taiwan)

Recently, multi-level cell (MLC) as a promising technique has been researching to increase the storage density of SONOS-type NAND non-volatile memory. However, the main challenge of MLC operation is an electrical reliability problem because charge data retention and device endurance influence discrimination of multi bit. Therefore, the level of voltage offset between state and state (11, 10, 01, and 00) plays one of the key factors for MLC.

P-4-9

Evaluation of ALD grown strontium-doped HfO₂ thin films as capacitor dielectric for 40nm DRAM Device and beyond

J. S. Lim, J. H. Choi, S. J. Chung, S. Y. Kang, M. Y. Park, Y. Kim, K. Cho and C. Y. Yoo, Samsung Electronics Co., Ltd. (Korea)

Sr doped HfO2 (Sr-HfO2) films with tetragonal crystal structure was fabricated by atomic layer deposition method and 550°C post deposition anneal. The specific dielectric constant of the tetragonal Sr-HfO2 film was as high as 40.

P-4-10 (Late News)

Organic Nonvolatile Memories Based on PMMA and PHEMA Dielectric Layers

Y. C. Chen¹, C. Y. Huang², H. C. Yu¹, C. Y. Cheng¹, Y. K. Su¹ and T. H. Chang¹, ¹National Cheng Kung Univ. and ²National Taitung Univ. (Taiwan)

We have fabricated the resistor-type memories with poly(2-hydroxyethyl methacrylate) PHEMA and poly(methyl methacrylate) PMMA active layer, respectively. From the I-V characteristics, the devices with PMMA active layer have a lower erasing voltage (1.9 V) than that (2.6 V) of PHEMA- devices.

Area 5: Advanced Circuits and Systems

(13 Papers)

P-5-2

A 1 Gb/s Differential Input Threshold Detection Based BPSK Receiver For IR-UWB Communication Using 180 nm CMOS Technology

M. Hafiz, N. Sasaki and T. Kikkawa, Hiroshima Univ. (Japan)

A complete non-coherent differential input threshold detection based receiver for UWB-IR communication is demonstrated. The chip developed in 180 nm CMOS technology, occupying an area of 3.4 mm², retrieves a BPSK data of 1 Gb/s using a supply voltage of 1.8 V while consuming 76 pJ/bit.

P-5-3

A Fractional-N Frequency Synthesizer-Based Multi-standard I/Q Carrier Generation System in 0.13um CMOS

W. Lou, X. Yan, Z. Geng and N. Wu, Institute of Semiconductors, Chinese Academy of Sciences (China) This paper presents a carrier generation system based on fractional-N frequency synthesizer with three Quadrature VCOs and it generates I/Q LO frequency. The locked frequency range is 2.8-6.1GHz. And successive divide_by_2 prescalers make the frequency from 0.7 to 6.1 GHz continuously by the reasonable frequency planning.

P-5-5

The Effect of Field-Plate Technique on CMOS Ring Oscillator

H. C. Chen¹, C. H. Kuo¹ and S. S. Lu², ¹National Taiwan Univ. of Sci. and Tech. and ²National Taiwan Univ. (Taiwan)

Field-plate technique is applied to ring oscillators in 0.35-µm CMOS technology. Ring oscillators constructed from field-plate transistors and standard ones achieve phase noises of -85.4/-82.9 dBc/Hz at 100-kHz offset, respectively. It improves the oscillator phase noise by 2-3 dB in the 1/f⁴ region but it makes no difference over the 1/f⁴ region.

P-5-6

A 12b Two-Stage Single-Slope ADC with Time to Digital Converter

M. Shin, M. Ikebe, J. Motohisa and E. Sano, Hokkaido Univ. (Japan) Applying a TDC with multi-phase-clock signals reduced the number of circuit elements, achieved consistency between a single-slope ADC and the TDC, and realized robust meta-stability. We designed a 12-bit ADC by using 0.25-um CMOS process.

P-5-7

Self-Dithered Digital Delta-Sigma Modulators for Fractional-N PLL Synthesizers Z. Xu, J. G. Lee and S. Masui, Tohoku Univ. (Japan)

2. At, J. O. Lee and S. Mastir, Toroku Oniv, (Appan) We propose a novel dithering method with simple implementation and non-hardware overhead to eliminate spurs of digital delta-sigma modulators (MASH and single-loop) applied in PLL applications. Simulation results compared with conventional solutions prove its effectiveness.

P-5-8

g_m/I_b Lookup Table Based Operational Transconductance Amplifier Design Featuring Settling Time Optimization

T. Kashimura, T. Konishi and S. Masui, Tohoku Univ. (Japan)

We propose the gm/I_{\rm p} lookup table based OTA design method featuring settling time optimization, which can achieve the target settling time with the minimum power consumption by employing an iterative design sequence.

P-5-9

A Novel Soft-Start Control Circuit for Current-Mode Buck DC-DC Converters

K. Shibata and C. K. Pham, The University of Electro-Communications (Japan) This paper proposes a soft-start control circuit for Current-Mode DC-DC Converters. The circuit achieved the soft-start characteristics of 150 µs. The control circuit is not sensitive to the input voltage, operating temperature and inductor value.

P-5-10

A Multiple Time Programmable On-chip Trimming Technique for CMOS Bandgap Reference Circuits

C. H. Wu, H. Lin and M. K. Wang, National Chung Hsing Univ. (Taiwan)

An alternative trimming technique for voltage reference circuits using multiple time programmable (MTP) devices is proposed using TSMC 0.35µm CMOS process in smaller chip area with more flexibility. The measurement results demonstrate the variation of reference voltages could be reduces from 120mV to 20mV after the trimming method was applied.

P-5-11

A Sub-nanoampere Two-stage Power Management Circuit in 0.35- μm CMOS for Dust-Size Batteryless Sensor Nodes

M. Ugajin, T. Shimamura, S. Mutoh and M. Harada, NTT Corp. (Japan)

A sub-nanoampere two-stage power management circuit that uses off-chip capacitors for energy accumulation is presented. The simulated and experimental results for the power management circuit describe the operation for a 1-nA current source.

P-5-12

An Energy Harvest Current-Mode Demodulator for Low Power 3-D Stacked Retinal Prosthesis

K. Kiyoyama¹², T. Fukushima², M. Koyanagi² and T. Tanaka², ¹Nagasaki Institute of Applied Science and ²Tohoku Univ. (Japan)

In this paper, the proposed current-mode demodulator using clamped current which is usually disposed thermal energy at clamp circuit is described.

P-5-13

A Novel RectifierArchitecture for UHF RFID Transponder

J. Cui, J. Akita and A. Kitagawa, Univ. of Kanazawa (Japan)

This paper presents a novel rectifier structure for wireless biomedical temperature monitoring tags. The proposed rectifier has an advance in realizing high power conversion efficiency (PCE) as well as gaining high output voltage simultaneously. This circuit has been fabricated in a standard CMOS process. Measurement results show a PCE of 32% at -30dBm incident power.

P-5-14

Distribution of Characteristic Changes in MOSFETs Induced by Resin-Molded Packaging Stress

N. Ueda, E. Nishiyama and H. Watanabe, RICOH Company, Ltd. (Japan) Packaging-induced performance reductions for a small-scale IC are evaluated using specially designed test chips. The results reveal that not only MOSFET selection but also the orientation should be considered for increasing the precision of ICs.

P-5-15 (Late News)

Low-Voltage and High-Speed Voltage-Controlled Ring Oscillator with Widely Tuning Range in 0.18µm CMOS

Y. S. Tiao, M. L. Sheu and L. J. Tsao, National Chi-Nan Univ. (Taiwan)

A new differential delay cell with a complementary current control to increase the control voltage range as well as the operation frequency is proposed for low-voltage op-eration. The measured results show that a wide operation frequency range with a best FOM from 8.36GHz to 1.29GHz and from 4.09GHz to 0.479GHz are achieved at the full range control voltage of 1.8V and 1V, respectively.

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Area 6: Compound Semiconductor Electron Devices and Related Technologies

P-6-1 Characterization of SiGe Thin Films Deposited by RF Magnetron Sputtering for Infrared Imaging Sensor

K. Yamaki¹, S. Sekino², T. Tai¹, S. Nakamura², T. Yoshitake² and A. Furukawa¹, ¹Tokyo Univ. of Sci. and ²NEC Corp. (Japan)

An alternating multi-stacked SiGe film was deposited by using RF magnetron sputtering technique for infrared imaging sensor. The film annealed in an Ar atmosphere exhibited a large TCR and a high conductivity.

P-6-3

The low frequency noise analysis in bottom-gated ZnO Thin film Transistors with different active layer thickness

K. S. Jeong¹, Y. S. Kim², J. G. Park¹, S. D. Yang¹, Y. M. Kim¹, H. J. Yun¹, H. D. Lee¹ and G. W. Lee¹, ¹Chungnam National Univ. and ²National NanoFab Center (Korea)

In this paper, 1/f noise is analyzed to characterize the quality of the active layer of ZnO TFTs with different thicknesses of 40 nm and 80 nm. The extracted Hooge's parameter (aH) indicates that the ZnO film of 80nm with the larger grain size has better quality, which explains well the inferior Vth instability of the ZnO film of 40nm.

P-6-5

Short Channel Effect of Indium-Gallium-Zinc-Oxide Thin Film Transistors

S. H. Kuk, D. W. Kang, J. S. Lee, S. J. Kim, J. Y. Kwon and M. K. Han, Seoul National Univ. (Korea) We have fabricated and investigated short channel IGZO TFTs. And we have investigated the current conduction mechanism of IGZO TFTs. When we design IGZO TFTs, we should consider the whole active layer, because IGZO films have high mobility and high carrier concentration.

P-6-6

Physics-Based Modeling and Analysis of Compound Semiconductor Devices and Circuits in Extreme Environments

M. Turowski, A. Raman and A. Fedoseyev, CFD Research Corp. (CFDRC) (USA) Mixed-mode simulations combining 3D device physics with external load circuit enable prediction of transient radiation effects in circuits with III-V HEMTs and SiGe HBTs. Including circuit parasitics is critical for computing results matching experimental data.

P-6-8

10-Gb/s InGaAs P-I-N photodetector with planar buried heterostructure

Y. S. Wang^{1,3}, S. J. Chang¹, Y. Z. Chiou², S. P. Chang¹, Y. H. Wu³, R. T. Hsu³ and W. Lin³, ¹National Cheng Kung Univ., ²Southern Taiwan University and ³LandMark Optoelectronics Corp. (Taiwan) The authors report the fabrication of high performance planar InGaAs P-I-N buried heterostructure photodetectors (BH-PD) by introducing mesa etching and refilling with semi-insulating InP. It was found that measured 3-dB bandwidth for the fabricated BH-PD was 12.4 GHz.

P-6-9

Enhanced Device Performance of AlGaN/GaN MOSHEMT with Thermal Oxidation

S. Liu¹, J. Wang¹, R. Gong¹, Z. Dong¹, M. Yu¹, C. P. Wen¹, C. Zeng², Y. Cai² and B. Zhang², ¹Peking Univ. and ²Suzhou Inst. of Nano-tech and Nano-bionics (China)

Bottom-gated thin-film transistors (TFTs) were fabricated on Corning 1737 glass substrates using ZnO channel layer grown by MOCVD and Si3N4 gate dielectric by PECVD. It is demonstrated that the VI/ II ratio used for the growth of ZnO film as well as the incorporation of a thin MgZnO layer at the ZnO/ Si3N4 interface affects TFT performance.

P-6-12

Normally-off GaN MOSFET with ITO Schottky Barrier Source/Drain and $(\rm NH_{\rm d})_2S_{\rm X}$ Surface Treatment

T. H. Kim¹, C. J. Lee¹, D. S. Kim¹, S. Y. Sung¹, B. K. Jung², Y. W. Heo¹, J. H. Lee¹ and S. H. Hahm¹, ¹Kyungbook National Univ: and ²Electronics and Telecommunications Res. Inst. (Korea) We demonstrated the schottky barrier metal oxide semiconductor field effect transistor applying indium-tin-oxide to the source and drain for the first time on the highly resistive GaN layer grown on silicon substrate. Using the (NH₄)₂S_x pretreatment of GaN substrate, the I-V characteristics were improved.

P-6-13

(11 Papers)

Improved optical properties of a-plane InGaN/GaN multiple quantum wells with gradient-stages MQW structure $% \mathcal{M} = \mathcal{M} = \mathcal{M} + \mathcal{M$

H. C. Hsu¹, Y. K. Su², S. J. Huang¹, C. Y. Cheng¹, H. C. Chen¹, J. H. Hong¹, K. C. Chen¹, Y. J. Wang³, C. Y. Wu³ and M. C. Chou³, ¹National Cheng Kung Univ., ²Kun Shan Univ. of Tech. and ³ITRI South Micro Systems Tech. Center (Taiwan)

In this paper, the crystal quality of a-plane InGaN \setminus GaN MQWs was further improved by implanting the gradient-stage MQWs before the active region. The a-palne InGaN \setminus GaN MQWs with N (N=0, 5, 8, and 11) pairs of gradient-stage MQWs structure was also investigated.

P-6-14

Investigation of Bias Temperature Instability in HfInZnO Thin Film Transistor

J. S. Chang¹, S. W. Kim¹, D. W. Kwon¹, J. H. Kim¹, J. C. Park², I. Song², U. I. Jung², C. J. Kim² and B. G. Park¹, 'Seoul National Univ. and 'Samsung Adv. Inst. of Tech. (Korea) In the HflnZnO TFT, some reliability issues such as NBTI and PBTI are investigated. PBTI causes threshold voltage shift, and it is attributed to electron injection and hopping into SiO2 bulk layer.

P-6-15

$Study \ of \ the \ CeO_{/} HfO_{/} In As \ metal-oxide-semiconductor \ capacitors \ with \ different \ post-deposition-annealing \ temperatures$

T. E. Shie¹, C. H. Chang¹, Y. C. Lin¹, K. Kakushima², H. Iwai², P. C. Lu¹, T. C. Lin¹, G. N. Huang¹ and E. Y. Chang¹, ¹National Chiao Tung Univ. and ²Tokyo Inst. of Tech. (Taiwan) We have fabricated CeO2/HfO2/InAs two layers high-k dielectric MOS capacitor. The device shows the good C-V characteristics and higher capacitance value than HfO2/InAs. It is an candidate for high performance low power logic device applications.

P-6-16 (Late News)

Transparent oxide thin-film transistors using modulation-doped heterostructures

S. Taniguchi¹, M. Yokozeki¹, M. Ikeda¹ and T. Suzuki², 'Sony Corp. and ¹JAIST (Japan) Employing n-ITO / IGZO modulation-doped het-erostructures, we confirmed enhancements of electron mo-bilities and TFT performances. Modulation doping is a promising method for improvements of TFT characteristics using TOSs.

Area 7: Photonic Devices and Optoelectronic Integration (21 Papers)

P-7-1

Electrorefractive Effect in Strained InGaAs/InAIAs Five-Layer Asymmetric Coupled Quantum Well

T. Wajima¹, T. Arakawa and K. Tada², ¹Yokohama National Univ. and ²Kanazawa Inst. Of Tech. (Japan)

We theoretically analyze an InGaAs/InAlAs strained five-layer asymmetric coupled quantum well for optical modulators based on phase modulation. It is expected to exhibit large electrorefractive index change over a wide wavelength range with low voltage.

P-7-2

Modification of Material Parameters for InGaAs/InAlAs Quantum Wells

H. Yamada, Y. Iseri and T. Arakawa, Yokohama National Univ. (Japan) We discuss material parameters for InGaAs/InAlAs quantum wells comparing experimental and calculated data. Using the modified material parameters, we succeeded in obtaining the calculated absorption coefficient spectra more consistent with the experimental.

P-7-3

Influence of Intrinsic Layer Impurity in InGaAs/InAlAs Asymmetric Triple Coupled Quantum Well on Its Electrorefractive Index Change

Y. Amma, K. Ema and T. Arakawa, Yokohama National Univ. (Japan) We theoretically discuss the electrorefractive effect in an InGaAs/InAIAs ATCQW for 1.55-umwavelength regions and the influence of intrinsic layer impurity on the electrorefractive index change of the ATCOW.

P-7-4

Dry Etching of Al-rich $\rm Al_xGa_{1:x}As$ Holes with High Aspect Ratio for Photonic Crystal Fabrication

M. Mochizuki, T. Nakajima, D. Satoi, F. Ishikawa, M. Kondow, M. Hara and H. Aoki, Osaka Univ. (Japan)

We investigate ICP dry etching of AlxGa1-xAs for Photonic crystals fabrication. Avoiding the formation of oxide deposition, we obtain the air holes having its aspect ratio of 8 with its small diameter 110 nm.

P-7-5

Two-terminal device based on white-light emitting in GaAs single layer

S. Choi¹, Y. W. Lee², B. J. Kim¹, J. Choi, G. W. Seo³ and H. T. Kim^{1, -1}ETRI, ²Pukyong National Univ. and ³Univ. of Science and Tech. (Korea)

The two-terminal based on p-type GaAs single layer shows a white light emission(WLE) with a wavelength of 500–800 nm in visible ray. The light intensity can be controlled by isolation size of film, thickness of film, and carrier concentration. Furthermore, a WLE can be applied as quantum dot laser source, various light fixtures, and photo-diodes.

P-7-6

Optical Characterization of Broadband Asymmetrical Quantum Well for Laser Array Application

W. L. Chen, National Changhua Univ. of Edu. (Taiwan)

A 98nm photoluminescence bandwidth centered at 1520nm was achieved by an AlGaInAs asymmetrical quantum well design and transition features have been identified by photoreflectance. The performance of DFB laser array was compared with optical characterization.

P-7-7

The Output Characteristics of a Soliton Cavity Laser Diode

M. C. Shih, W. C. Su and C. S. Chen, National Univ. of Kaohsiung (Taiwan)

We present the output characteristics of a novel semiconductor laser diode with an intra cavity of solitons waveguide. It shows a different output characteristics from the traditional linear laser stripe lasers.

P-7-8

Enhanced Light Output of Vertical GaN-Based LEDs with Surface Roughening Using Sizu-Controllable ${\rm SiO}_2$ Nanotube Arrays

D. M. Kuo¹, S. J. Wang, K. M. Uang², T. M. Chen, W. C. Lee¹ and P. R. Lee, ¹National Cheng Kung Univ. and ²Wufeng Inst. of Tech. (Taiwan)

The use of SiO2 nanotube arrays for nano-roughened n-GaN surface to improve the optoelectronic properties of vertical structure GaN-based LEDs shown a typical increase in light output power by 49.8% at 350 mA

P-7-10

An Investigation of GaN-Based LED with MBE Grown Nanopillars by MOCVD.

K. L. Chuang, J. R. Chang, P. M. Tu, C. H. Chiu, Y. J. Li, H. W. Zan, H. C. Kuo and C. Y. Chang, National Chiao Tung Univ. (Taiwan)

High quality GaN-based LED was fabricated by MOCVD using MBE GaN NPs template. Room temperature Raman shift and TEM demonstrated great reduction in the strain of sample and the quality enhancement mechanism, void-induced dislocation-gathering and stress-relaxation.

P-7-11

High Quality Vertical LEDs Fabrication by Means of Mechanical Lift-off

P. M. Tu¹, S. C. Hsu², M. H. Lo¹, H. W. Zan, H. C. Kuo, S. C. Wang, Y. J. Cheng³ and C. Y. Cheng¹, ¹National Chiao Tung Univ.,² Tamkang Univ. and ³Academia Sinica (Taiwan) We report the fabrication of mechanical lift-off high quality thin GaN by using Hexagonal Inversed Pyramid (HIP) structures as a sacrificial layer during wafer bonding process for vertical light emitting diodes.

P-7-12

The Improvement of Light Intensity for Nitride-Based MQW LEDs by Gradient-Stage Emitter Layer

S. J. Huang, Y. K. Su, C. Y. Tseng, S. C. Lin and H. C. Hsu, National Cheng Kung Univ. (Taiwan) The light intensity of nitride-based LEDs is improved by an emitter layer (EL) with gradient depth of quantum wells (QWs). The results shows about 20% increment compared to dual-stage LED.

P-7-13

Manipulative Polarization of a-plane InGaN/GaN Photonic Crystals for Enhanced Spontaneous Emission

Y. C. Lee¹, H. H. Huang², Y. R. Wu and P. Yu¹, ¹National Chiao Tung Univ. and ²National Taiwan Univ. (Taiwan)

Polarization characteristics of a-plane InGaN/GaN photonic crystal microcavities are manipulated to enhance spontaneous emission (SpE) without compromising cavity Q and modal volume. Enhanced SpE rates are investigated for different quantum well thicknesses and indium compositions

P-7-14

Reduction in efficiency droop in InGaN/GaN MQWs light-emitting diodes grown on free standing GaN substrate

C. H. Chiu¹, C. L. Chao¹², D. W. Lin¹, Z. Y. Li, H. C. Kuo, T. C. Lu and S. C. Wang, ¹National Chiao Tung Univ. and ²Indus. Tech. Res. Inst. (Taiwan)

The LEDs fabricated on the free-standing GaN template exhibit smaller EL peak wavelength blue shift (1.2 nm), great enhancement of the light output and reduced efficiency droop compared with the conventional LEDs.

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P-7-15

Estimating the Junction Temperature of InGaN and AlGaInP LEDs

Y. J. Lee, C. J. Lee and C. H. Chen, National Taiwan Normal Univ. (Taiwan) This work proposes an approach for directly determining the dependence of junction temperature on injected currents in InGaN and AlGaInP LEDs. Various important physical parameters that affect the junction temperature of an LED are also considered.

P-7-16

Characteristics of $\mu\mbox{-Slice InGaN/GaN}$ Light Emitting Diodes Formed by Focused Ion Beam Process

C. K. Hsu¹, J. K. Sheu, J. K. Wang, M. L. Lee², K. H. Chang¹, S. J. Tu and W. C. Lai, ¹National Cheng Kung Univ. and ²Southern Taiwan Univ. (Taiwan)

In this study, we used focused ion beam to mill GaN/InGaN LED wafer into single micro scale device. The electrical and optical properties have been studied to investigate the damage caused by the ion beam.

P-7-17

GaN-based MIS Ultra-violet Photodetectors with the $\rm ZrO_2$ Insulating Layer

C. H. Chen, Y. H. Tsai, S. Y. Tsai and C. F. Cheng, Cheng Shiu Univ. (Taiwan) GaN MIS UV photodetectors with ZrO2 insulating layer were successfully fabricated and characterized. It was found that we can achieve the small dark current and large photocurrent to dark current contrast ratio from the proposed device with the use of ZrO2 insulating layer.

P-7-18

Fabrication of Multi-Stack Ge Quantum-Dots for Blue to Near-Ultraviolet MOS Photodetectors R. H. Yeh¹, S. Y. Lo², C. H. Yang, J. T. Horng and J. W. Hong, ¹Asia Univ. and ²National Central Univ.

(Taiwan) Metal-oxide-semiconductor photodetectors (PDs) with multi-stack and discrete Ge quantum dots (QDs) embedded in a-SiON/SiO2 matrix for visible to near-ultraviolet photodetection have been fab-

ricated with thermal anneal of as-deposited amorphous alloy layers.

P-7-20

Mach-Zehnder Electro-Optic Modulator Fabricated on Silicon-on-Insulator (SOI) Substrate Based on the Multimode Interference (MMI) Effect

R. W. Chuang^{1,3}, M. T. Hsu¹, Y. C. Chang, S. H. Chou³ and Y. J. Lee³, ¹National Cheng Kung Unix, ²National Nano Device Laboratories, Hsinchu City and ³National Nano Device Laboratories, Tainan (Taiwan)

The design of MMI-based 3dB MZI power splitter/combiner with dimensions of 6000um x 40um was proposed and analyzed. The operation of this device was based on the carrier injection effect, from which an approximate extinction ratio of -18.3 dB was obtained using BPM simulation. As for the device measurements, when the driving power was set at 0.2 W, the first π phase shift was observed.

P-7-21

Low loss junction of Si-wire waveguides and silica based waveguides for a hybrid waveguide photonic integrated circuit

Y. Wakayama, T. Kita and H. Yamada, Tohoku Univ. (Japan)

The concept of the proposed hybrid waveguide photonic integrated circuit is that silica based waveguide is used for long distance optical interconnection and Si-wire waveguides are used for making sharp bend.

P-7-22

Migration-limited relaxation in Er_xY_{2-x}SiO₅ crystals

T. Nakajima, T. Kimura and H. Isshiki, Univ. of Electro-Communications (Japan) Er_2iO_5 crystal is a key light source material for Si-photonics. In this system, the energy transfer can occurred between Er^{3*} - Er^{3*} in ${}^{4}I_{13/2}$.

P-7-23

Transmission enhancement of metal-patterned resonant filters on silicon substrates in terahertz frequencies

P. K. Chung, H. C. Huang and S. T. Yen, National Chiao Tung Univ. (China) We demonstrated a substrate-supported metal-patterned resonant filter with peak transmittance approaching transmittance of the substrate. The filter showed over 10 % increase in the peak transmittance and a comparable quality factor comparing with conventional filters.

Area 8: Advanced Material Synthesis and Crystal Growth Technology

(16 Papers)

P-8-1

Growth of semipolar InN (10-13) on LaAlO₃(112) substrate

W. C. Chen^{1,4}, S. Y. Kuo³, W. T. Lin³, J. S. Tian⁷, F. I. Lat³, C. N. Hsiao¹ and L. Chang⁴, ¹National Applied Research Labs., ²Chang Gung Univ., ³Yuan-Ze Univ. and ¹National Chiao Tung Univ. (Taiwan) In this study, we report the growth and characterization of semipolar (10-13) InN films grown on LaAIO3 (112) substrate by metalorganic molecular beam epitaxy. InN films were grown at various substrate temperatures in the range of 465–540 °C.

P-8-2

Growth Mechanism of Nonpolar A-Plane GaN on Patterned M-Plane Sapphire

K. L. Chuang, J. R. Chang, S. P. Chang, P. M. Tu, Y. C. Hsu, W. Y. Chen, H. W. Zan, T. C. Lu, H. C., Kuo and C. Y. Chang, National Chiao Tung Univ. (Taiwan) Growth mechanism of a-GaN on trench-patterned m-sapphire by MOCVD under different V/III ratio was demonstrated. For V/III ratio from 350 up to 9000, growth of GaN from +c plane sidewalls is dominated.

P-8-4

Laser Treatment of AlN Co-doped ZnO Film for p-type ZnO Fabrication

L. W. Lai, K. W. Lin, C. H. Chang and J. T. Chen, Indus. Tech. Res. Inst. (Taiwan) High quality p-type ZnO film can be obtained by co-sputtering of ZnO and AlN targets under adequate N2/Ar flow ratio of 4% and laser activation energy density at 150mJ/cm2.

P-8-5

Zinc oxide (ZnO) grown by Vertical-Plasma-Enhanced Metal Organic Chemical Vapor Deposition (VPEMOCVD)

P. H. Lei, H. F. Kao, F. S. Juang and X. M. Wu, National Formosa Univ. (Taiwan) In this article, we have successfully fabricated ZnO film by VPEMOCVD. The growth temperature changed from 300 to 600 °C under the growth pressure of 30 mtorr and RF power of 100mW. The optical and electrical measurement indicated that the optimum growth temperature is around 500 °C.

P-8-6

Fabrication of transparent p-NiO/n-ZnO heterojunction diodes for ultraviolet photodetector S. Y. Tsai¹, M. H. Hon¹ and Y. M. Lu², ¹National Cheng Kung Univ. and ²National University of Tainan (Taiwan)

The fabrication and the properties of an optically transparent p-n heterojunction photodiode consisting of p-NiO and n-ZnO thin films. The structural and optical properties of the n-ZnO/p-NiO heterojunction were characterized by X-ray diffraction (XRD), UV-visible spectroscopy, Hall measurement, and I-V photocurrent measurements.

P-8-7

Preparation and Characterization of white ZnS:Pr,Mn,KCl Phosphor

S. H. Yang, C. H. Wang, Y. H. Ling and C. F. Do, National Kaohsiung University of Applied Sciences (Taiwan)

Approaches of mixing complementary phosphors and codoping of activators were used to prepare white ZnS-based phosphors. Photoluminescence of the phosphor prepared by codoping was higher than that of the phosphor prepared by complementary mixing.

P-8-8

Growing evaporated Ge dots with high crystallinity on patterned Si substrate by post thermal annealing

C. W. Chiu, T. W. Liao, H. J. Huang, J. H. Lin and C. H. Kuan, National Taiwan Univ. (Taiwan) To obtain the evaporated Ge dots with high crystallinity on Si substrate, a method of using nano-structure and post thermal annealing is demonstrated. With well-designed hole-array pitch, the distribution of oxygen and quality of Ge QDs can be optimized. The processed Ge QDs size is over 20 nm which is estimated with the phonon confinement model of Raman scattering and confirmed by TEM image.

P-8-9

Site- and shape-controlled growth of single and pair of InAs quantum dots using AFM anodic oxidation

K. M. Cha¹, K. Shibata¹, I. Horiuch¹, T. Ueda¹ and K. Hirakawa¹², ¹IIS/INQIE, Univ. of Tokyo and ²CREST-JST (Japan)

Site- and shape-controlled InAs QDs have been fabricated by AFM-assisted anodic oxidation at various applied voltages. It was found that site-controlled QDs have clear facets, suggesting their excellent crystalline quality. The size-control of InAs QDs was carried out by changing the applied voltage V and found that the lateral size of the QDs can be reproducibly controlled over a range of 30-140 nm simply by tuning V.

P-8-10

Graphene Layers on Sapphire Substrates Grown by Alcohol CVD method

Y. Miyasaka, A. Nakamura and J. Temmyo, Shizuoka Univ. (Japan) We evaluated graphene layers on sapphire substrates synthesized by alcohol CVD using UV-VIS spectral transmittance measurement and Raman spectroscopy. The results indicates a significance of a certain amount of thermal energy to form graphene networks on sapphire substrates.

P-8-11

High electron mobility InSb films grown on Si (111) substrate via $\sqrt{7}\times\sqrt{3}$ -In and 2×2-In surface reconstructions

S. Khamseh, K. Nakatani, K. Nakayama, M. Mori and K. Maezawa, Univ. of Toyama (Japan) The heteroepitaxial growth of InSb films with high electron mobility achieved via InSb bi-layer with two step growth procedure. This study shows the efficiency of the InSb bi-layer and two-step growth procedure for the improvement of the electrical property of the InSb films.

P-8-12

Facile Fabrication of Two-dimensional Assemblies of Gold Nanoparticles by Using Solvent evaporation method

K. Sugawa, Y. Tanoue, D. Tanaka and T. Sakai, Nihon Univ. (Japan)

A novel approach for the rapid and facile preparation of thetwo-dimensional assemblies of gold nanoparticles by solventevaporation method was established. The detailed structures of the assemblies were confirmed by absorption spectra and SEM.

P-8-13

Fabrication and Photoelectrochemical Properties of Multilayer Assemblies Consisting of Silvernanoparticles, Polydiacetylene, and Polyions

T. Akiyama¹, A. Masuhara², Y. Matsuda³, T. Arakawa⁴, T. Munaoka⁴, T. Onodera³, H. Okikawa³ and S. Yamada⁴, ¹The University of Shiga Prefecture, ²Yamagata Univ., ³Tohoku Univ. and ⁴Kyushu Univ. (Japan)

We attempted to fabricate multilayer assemblies, which consisted of Ag NPs, polydiacetylene, and polyions by the LbL technique. Furthermore, we evaluated the photon-to-current conversion efficiency of the multilayer assemblies fabricated on ITO electrodes.

P-8-15

Efficient Preparation of Size-Controlled Nanoparticles using Thin Film Laser Ablation in Water M. Fukudome and H. Ikenoue, Kochi Nat'l Col. of Tech. (Japan)

We could successfully develop a novel method for efficient preparation of size-controlled nanoparticles with narrow size distribution using thin film laser ablation in water.

P-8-16

Degradation Mechanism for CLC Poly-Si n-TFTs under Low Vertical-Field HC Stress with Different Laser Annealing Powers

S. Y. Chang¹, M. C. Wang¹², Z. Y. Hsieh² and C. Chen³, ¹Ming Hsin University of Science & Technology, ²National Taipei Univ. of Tech. and ³National Chiao Tung Univ. (Taiwan)

The CLC poly-Si n-TFT with various laser annealing powers was investigated in this research. The degradation mechanism of device under voltage stress is dominated by HCE at the low vertical field.

P-8-17

Polarized Thermoreflectance and Reflectance Study of ReS2 and ReS2: Au Single Crystals

T. P. Huang¹, D. Y. Lin¹, J. D. Wu² and Y. S. Huang², ¹National Changhua Univ. of Edu. and ²National Taiwan Univ. of Sci. and Tech. (Taiwan)

We have presented optical characterization of ReS2 and ReS2:Au by using PTR and R measurements. The indirect band gaps and direct band edge excitonic transitions at various polarization angles have been observed. The temperature dependences, broadening parameters and doping effects are discussed.

P-8-19 (Late News)

Fabrication of coaxial p-copper oxide/n-ZnO nanowire photodiodes

H. T. Hsueh^{1,2}, S. J. Chang¹, F. Y. Hung¹ and T. J. Hsueh², ¹National Cheng Kung Univ. and ²National Nano Device Labs. (Taiwan)

The authors report the fabrication of p-copper oxide/n-ZnO nanowire photodiodes. It was found that we can achieve Cu2O/ZnO, Cu4O3/ZnO and CuO/ZnO nanowire photodiode by changing the O2 flow rate. The responses were also discussed.

Thursday, September 23

Area 9: Physics and Application of Novel Functional Devices and Materials

(14 Papers)

P-9-1

Full-dimensional analysis of coherent spin dynamics in a semiconductor

T. Inagaki^{1,2}, H. Koacka^{1,2}, Y. Rikitake^{1,2}, H. Imamura^{4,2}, Y. Mitsumori^{1,2} and K. Edamatsu¹, ¹Tohoku Univ., ²CREST-JST, ³Sendai National College of Technology and ⁴AIST (Japan) We demonstrate full-dimensional analysis of electron spin dynamics by applying the developed TKR method. The analysis clarified that the spin x-state, which is parallel to the applied magnetic field, only decays without the Larmor precession, and the spin lifetime of any prepared spin state are approximately equal to 600 ps without significant basis dependency.

P-9-2

Ultrasonic wave induced mechanoluminescence

N. Terasaki⁷, H. Yamada⁷ and C. N. Xu², ¹AIST and ²JST (Japan) Mechanoluminescent particles emit intensive light under application of mechanical stress. From the viewpoint of a ubiquitous light source, we have investigated mechanoluminescence induced by ultrasonic wave, non-destructive and non-inventive stimulation, and successfully detect it.

P-9-3

Effects of interface grading on electronic states and optical transitions in GaAb type-II quantum dots in GaAs

T. Kawazu¹ and H. Sakaki^{1,2}, ¹NIMS and ²Toyota Technological Inst. (Japan)

We theoretically analyze the effects of the Sb/As intermixing on a GaSb/GaAs type-II QD system and discuss how the spatial overlap of holes and electrons and the PL intensity is affected by the intermixing.

P-9-4

Source Engineering for Tunnel Field-Effect Transistor: Elevated Source with Vertical Silicon-Germanium/Germanium Heterostructure

G. Han, P. Guo, Y. Yang, L. Fan, Y. S. Yee, C. Zhan and Y. C. Yeo, National Univ. of Singapore (Singapore)

Source engineering for TFET with in situ B-doped Si0.5Ge0.5 source was investigated. A Ge layer inserted beneath the Si0.5Ge0.5 source effectively increased the ION and subthreshold swing of the TFET due to the reduction of tunnel barrier and the suppression of B diffusion into Si channel.

P-9-5

NIS tunneling junction fabricated by superconducting Boron-doped diamond

R. Nomura¹, S. Kitagoh¹, M. Watanabe¹, Y. Takano², T. Yamaguchi² and H. Kawarada¹, ¹Waseda Univ. and ²NIMS (Japan)

We fabricated Normal conductor — Insulator — Superconductor (NIS) tunneling junction operates with heavily boron doped diamond layer as superconductor. The typical characteristics of current-voltage and dl/dV-voltage are observed. We thought this junction has a potential to be a promising detector or some such devices.

P-9-6

Improved Characteristics of MOCVD Grown ZnO TFTs by Controlling VI/II Ratio of ZnO Film Growth and Using a Modified TFT Layer Structure

K. Remashan, Y. S. Choi, S. J. Park and J. H. Jang, GIST (Korea)

The incorporation of the MgZnO layer and the use of higher VI/II ratio grown ZnO channel greatly enhanced TFT performance in terms of μ_{FE} , S, and on/off current ratio. This is due to the larger grains in, and lower growth rate of the ZnO film.

P-9-7

High-Performance Polycrystalline Silicon Thin-Film Transistor with Nickel-Titanium Oxide by Sol-Gel Spin-Coating and Fluorine Implantation

S. C. Wu¹, T. H. Hou¹, S. H. Chuang², H. C. Chou², P. Y. Kuo¹, T. S. Chao¹ and T. F. Lei¹, ¹National Chiao Tung Univ. and ²National Univ. of Kaohsiung (Taiwan)

A high-performance poly-Si TFTs is reported without additional hydrogenation or advanced phase crystallization techniques. Excellent electrical characteristics are attributed to the promising high-k NiTiO3 by sol-gel spin-coating and the trap passivation by fluorine implantation.

P-9-8

Correlating phonon frequency shift with magnetoelectric effect in the $PbTiO_3\text{-}CoFe_2O_4$ multiferroic system due to interfacial stress

C. Y. Tsai¹, T. C. Huang² and W. F. Hsieh^{1,3}, ¹National Chiao Tung Univ., ²National Taiwan Normal Univ. and ³National Cheng Kung Univ. (Taiwan)

We report on the correlation between local behavior of interfacial phonon and ferromagnetic properties in three multiferroic consisting of different geometric shapes of ferromagnetic CoFe2O4 (CFO) embedded in the ferroelectric matrix of PbTiO3 (PTO) by using micro-Raman spectroscopy and SQUID.

P-9-9

Light Enhancement of Si-Nanocrystals-Embedded SiOx film on Silicon-on-Insulator Substrate C. C. Chen¹, Y. H. Lin², M. H. Shil³, G. R. Lin² and H. C. Kuo¹, ¹National Chiao Tung Univ, ²National Taiwan Univ. and ²Academia Sinica (Taiwan)

We reported light enhancement from a Si-nanocrystals-embedded SiOx film on a silicon-on-insulator substrate in visible light range. Compared with SiOx film on a Si substrate, A strong emission from the SOI substrate was observed from SiOx film on SOI substrate was observed.

P-9-10

Multistep Electron Injection in a PtSi-Nanodots/Silicon-Quantum-Dots Hybrid Floating Gate in nMOSFETs

M. Ikeda, S. Nakanishi, N. Morisawa, A. Kawanami, K. Makihara and S. Miyazaki, Hiroshima Univ. (Japan)

The multistep electrons injection in an nMOSFET with a PtSi-NDs/Si-QDs hybrid floating FG has been demonstrated. This result can be interpreted in terms of the electron injection into the PtSi-NDs through the discrete charged states of Si-QDs.

P-9-11

Monolithic Integration of Ni-SPC Poly-Si TFTs and Lateral Large-grained Poly-Si TFTs

A. Hara, K. Kondo, T. Sato and T. Sato, Tohoku Gakuin Univ. (Japan) In this paper, Ni-SPC poly-Si TFTs and lateral large-grained poly-Si TFTs were fabricated on different regions of a glass substrate, and then, the performance of each was evaluated.

P-9-12

Electric properties of SONOS memories with embedded silicon nanocrystals in nitride

M. C. Hsieh, T. Y. Chiang, H. A. Dai, C. C. Chen, C. H. Chiang, J. F. Wang, Y. J. Lin, J. Y. He, Y. N. Chen, T. S. Chao and J. F. Chen, National Chiao Tung Univ. (Taiwan) Interface states at the SiO2(S)-substrate interface are identified by experiment and simulation. Embedded Si-NCs in nitride are confirmed as a formation of Si-quantum dots in nitride. The Si-NCs form quantum confined states above conduction band.

P-9-13

Analysis of MOSFET Electrometer Sensitivity by Radio-Frequency Reflection

M. Kawai, V. Singh, M. Nagasaka, H. Satoh and H. Inokawa, Shizuoka Univ. (Japan) By the use of the RF reflection, electrometer consisting of 70-nm-gate MOSFET could operate at the speed of 25 MHz with a charge sensitivity of 5E-3 e/Hz⁺0.5 at room temperature. It was also found that the down scaling of the gate length is effective in improvement of the charge sensi-tivity.

P-9-14 (Late News)

Room-Temperature Number-Resolving Single-Photon Detection by SOI MOSFET

W. Du, H. Inokawa and H. Satoh, Shizuoka Univ. (Japan)

SOI MOSFET was evaluated as a single-photon detector. The device showed dark counts less than 0.02 cps even at 300 K, and the output waveforms exhibited clear separation of current levels, indicating the possibility of photon-number resolution. The recombination mechanism of the holes was also investigated, and indirect transition was suggested.

Area 10: Organic Materials Science, Device Physics, and Applications (20 Papers)

P-10-1

A stacked organic/inorganic vapor barrier structure encapsulated flexible plastic substrates prepared using plasma-enhanced chemical vapor deposition

M. S. Jeng¹, C. S. Chuang², L. W. Lai², B. Y. Lin¹ and D. S. Liu¹, ¹National Formosa Univ. and ²Indus. Tech. Res. Inst. (Taiwan)

A stacked organosilicon/SiOx layered-structure prepared by PECVD using the TMS monomer was applied to encapsulate the plastic substrate. An ultra-low WVTR was achieved from the PET substrate coated with a six-pair organosilicon/SiOx barrier structure.

P-10-2

Roll-type Micro-contact printing process with PDMS stamp for patterning conductive Metal Line with Ag ink

J. H. Kim, M. Y. Lee, Y. J. Park and C. K. Song, Dong-A Univ. (Korea)

In this paper, we fabricated the conductive metal line by roll type micro-contact printing with PDMS stamp using nano Silver ink. The ink transfer characteristic during printing was improved by optimizing a coating condition, inking speed, printing speed, printing pressure and Ag content. As a result, printed a line width of 30um, thickness of ~300nm, roughness less than 40nm.

P-10-3

Synthesis and Optical Properties of Polysilanes Containing Anthryl Groups

S. Ishibe, T. Mizuno and H. Tachibana, AIST (Japan) Liner and network polysilane possessing antihyl group were synthesized, and the effect of heat and/or treatment on UV-vis-NIR spectroscopy is investigated. The result indicates heat treatment afford lower energy shift of the polymer absorption.

P-10-5

Estimation of Electron Injection Barrier Height at Metal/ Polymer Interface by Internal Photoemission Spectroscopy and its Schottky Current Analysis

E. Itoh and S. Takaishi, Shinshu Univ. (Japan)

We have estimated the electron injection barrier height at metal/polyfluorene based polymer interface by internal photoemission spectroscopy technique and current analysis as a function of electronegativity of cathode materials and the interfacial mid-gap states.

P-10-6

Extraction of Energy Density Profile of Bulk and Interface Trap States in Pentacene

S. H. Jeong and C. K. Song, Dong-A Univ. (Korea)

We extracted energy density of bulk and interface trap states in pentacene on PVP by using temperature dependent space charge limited current and temperature dependent transfer characteristics respectively. The bulk trap states exhibited a large state at 1.3 eV and the interface trap states also produced a large energy states at 1.2 eV.

P-10-7

Effect of Device Structure on Electrical Conduction of Terphenyl-based Molecule

T. Goto¹, H. Inokawa², Y. Ono¹, A. Fujiwara¹ and K. Torimitsu¹, ¹NTT Basic Res Labs. NTT Corp. and ²Shizuoka Univ. (Japan)

A recent study of phenylene-based molecular devices has revealed many intriguing features. In this report, a phenylene-based molecule is selected, and the effect of device structure on electrical conduction is investigated.

P-10-8

High Efficiency Electrophosphorescence Red OLEDs Using a Thin BPY-OXD Cleaving Layer in an Ir-complex Doped Emitter Layer

C. H. Chen, K. R. Wang, Y. H. Tsai, S. F. Yen, P. Y. Su and C. F. Cheng, Cheng Shiu Univ. (Taiwan) The authors demonstrate a considerable increase in current efficiency of Ir(piq)2(acac) doped phosphorescent organic red-light emitting device in which a thin Bpy-OXD layer acts as a cleaving layer. When a 5 nm Bpy-OXD layer divides the emitting layer (EML) into two sub-EMLs, a maximum luminance of 9830 cd/m2 and current efficiency of 4.36 cd/A were obtained, which is higher than that of the device without it.

P-10-9

Oriented PFO Films Dye-Doped for Whitening of Polarized EL Devices

C. Heck, T. Mizokuro and N. Tanigaki, AIST (Japan)

We report on the combination of vapor transportation and friction transfer methods for doping linear fluorescent dyes into oriented polymer films. The ultimate aim is to produce white polarized EL devices by doping an orange dye into a blue emitting oriented PFO film in a way that the dye orientation is parallel to the orientation of the PFO film.

P-10-10

Application of a Porous Titanium Film to a Counter Electrode of a Dye-sensitized Solar Cell

M. Rahman, R. Kojima, M. E. F. Fihry, Y. Kimura and M. Niwano, Tohoku Univ. (Japan) Here we developed a new counter electrode with porous Ti film for dye sensitized solar cells. It is seen that DSC with porous Ti shows better performance than that of usual Pt counter electrode.

P-10-11

Annealing Effects on Polymer Solar Cells with High Polythiophene- fullerene Concentrations

C. S. Ho¹, E. L. Huang¹, W. C. Hsu¹, C. S. Lee², Y. N. Lai¹ and W. H. Lai¹, ¹National Cheng Kung Univ. and ²Feng Chia Univ. (Taiwan)

Composites of conjugated P3HT and PCBM with 3 and 5 wt% concentrations are prepared to study the thermal annealing effect at different temperatures. In the case of 3 wt% film, absorption spectrum shows a small increase of intensity upon annealing between 110 and 150°C whereas an obvious degradation as the temperature is higher than 170°C.

P-10-12

Construction and Evaluation of Organic Solar Cells Using a Spray-Coating Method

Y. Murakami, H. Ishihara, T. Mizutani, K. Kojima and S. Ochiai, Aich Inst. of Tech (Japan) In this study, we fabricated orgnic solar cells by spray-coating method. As a result, the short circuit current density is 2.07mA/cm², the open circuit voltage is 0.45V, and the power conversion efficiency 0.35%.

Thursday, September 23

P-10-13

Silver Nanoparticle-Assisted Photocurrent Generation in Polythiophene-Fullerene Thin Films

J. You, T. Arakawa, H. Yoneda, T. Akiyama and S. Yamada, Kyushu Univ. (Japan) We have tried to use LSPR of silver nanoparticles in order to enhance light absorption and resultant photocurrent generation from polythiophene-fullerene thin films. The effects of LSPR were verified.

P-10-14

Performance Improvement of OTFT by controlling Crystal Morphology of TIPS-Pentacene

M. J. Kim, G. S. Ryu, J. W. Hwang and C. K. Song, Dong-A Univ. (Korea) In this paper, we controlled crystal morphology of TIPS pentacene by adjusting the moving velocity of edge contact line of droplet to be matched with the velocity of crystal formation at the edge.

P-10-15

Numerical Simulation of Contact Resistance in Organic Field-Effect Transistors

S. Nishigami, T. Nagase, T. Kobayashi and H. Naito, Osaka Prefecture Univ. (Japan) We have carried out the two dimensional simulation of top-contact and bottom-contact OFETs in the presence of localized states and disorder regions in order to investigate the origin of contact resistance

P-10-16

Frequency Response of Polymer Field-Effect Transistors Fabricated by a Self-Aligned Method

H. Hatta¹, Y. Miyagawa¹, T. Nagase^{1,2}, T. Kobayashi^{1,2}, S. Murakami³, M. Watanabe⁴, K. Matsukawa⁴ and H. Naito, ¹Osaka Prefecture Univ, ²The Res. Inst. for Molecular Electronic Device, ³Tech. Res. Inst. of Osaka Prefecture and ⁴Osaka Municipal Technical Res. Inst. (Japan) We have investigated frequency characteristics of po-lymer-based OFETs fabricated by the selfaligned method. The impedance spectroscopy of the self-aligned OFETs reveals the three-orders-ofmagnitude decrease in parasitic capacitance from conventional OFETs and frequency de-pendence of channel formation process in OFETs.

P-10-17

UV-patternable polymer dielectric for organic thin film transistors

C. M. Wu, H. T. Wang, S. H. Su and M. Yokoyama, I-Shou Univ. (Taiwan) The OTFTs using a UV-patternable polymer material, mr-UVCur06, as the gate dielectric have been fabricated and characterized. The pattern resolution can reach 3 μm and the pentacene-based OTFTs exhibit an on-off ratio around 105.

P-10-18

Improvement of Pentacene Organic Thin-Film Transistor Considering Quantum Effect A. Heya and N. Matsuo, Univ. of Hyogo (Japan)

Carrier transport in organic thin-film transistors (OTFTs) was investigated by using pentacene OTFT and sample for vertical transport evaluation with various film thickness from 1 to 50nm. The Ion of 3nm OTFT was higher than that of 50nm OTFT. It is considered that the triangle potential was formed at interface between pentacene and SiO2.

P-10-19

Temperature Dependence of Charge Transport in Polythiophene-Based Field-Effect Transistors

M. Yoshikawa¹, T. Banno¹, T. Nagase², T. Kobayashi¹, S. Murakami² and H. Naito, ¹Osaka Prefecture Univ. and ²Tech. Res. Inst. of Osaka Prefecture (Japan)

Field-effect transistor (FET) measurements of Organic FETs based on regioregular polythiophenes in a wide temperature range from 9 K to 300 K have been performed to investigate charge transport mechanism in OFETs.

P-10-20

Reverser off-set Printing Process for Gate Electrodes of OTFT-Backplane

J. E. Park, M. Y. Lee and C. K. Song, Dong-A Univ. (Korea)

For gate electrodes and lines of OTFT-backplane, first, screen printing was applied to uniformly deposit Ag ink thin film over the area of substrate, and then etching resist was patterned by reverse off-set printing. The final gate electrodes were obtained through etching Ag ink layer. By using this process the line feature of 50 um was obtained with the resistance of 1 W/square over 6° substrate.

P-10-21 Wettability Improvement by Silica Nanoparticle Addition in Solution-Processed TIPS-Pentacene Field-Effect Transistors

S. Yamazaki¹², T. Hamada², S. Tokai¹, M. Yoshikawa², T. Nagase²³, T. Kobayashi, Y. Michiwaki⁴, S. Watase², M. Watamabe³, K. Matsukawa² and H. Naito²³, ¹Citizen Holdings Co., LTD., ²Osaka Prefecture Univ., ³Res. Inst. Molecular Electronic Dev., ⁴Fuso Chemical Co., LTD. and ³Osaka Municipal Technical Res. Inst. (Japan)

We report the improvement of the wettability of soluble organic semiconductors of TIPS-pentacene on hydrophobic poly(methylsilsesquioxane) gate dielectrics by the addition of silica nanoparticles. Silica nanoparticle addition also allows the direct patterning with ink-jet process. Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) (13 Papers)

P-11-1

Detection of Antigen-Antibody Reaction Using Si Ring Optical Resonators Functionalized with an Immobilized Antibody-Binding Protein

M. Nishida, M. Fukuyama, Y. Abe, Y. Amemiya, T. Ikeda, A. Kuroda and S. Yokoyama, Hiroshima Univ. (Japan)

Rapid immobilization technique for variety of antibodies on Si-ring optical-resonator biosensor has been developed using Si-tagged protein A, which leads to the integrated high-throughput biosensors. Green fluorescent protein and prostate specific antigens were actually detected

P-11-2

Control of Supported Lipid Bilayer Self-Spreading through Nanogap by Local Electric Field

Y. Kashimura, K. Furukawa and K. Torimitsu, NTT Basic Res. Labs. NTT Corporation (Japan) We demonstrated that the development of the self-spreading lipid bilayers could be controlled by the temporal switching of the electric field applied to a nanogap.

P-11-3

Surface Infrared Spctroscopic Study of ATP Synthesis in Mitochondria

Y. Aonuma¹, R. Yamaguchi¹, M. Abe¹, A. Hirano-Iwata², Y. Kimura¹, Y. Shinohara³ and M. Niwano¹², ¹Tohoku Univ, ²JST and ³Univ. of Tokushima (Japan)

We have monitored ATP synthesis in isolated mitochondria by using IRAS in the multiple internal reflection (MIR) geometry. Through real-time monitoring of oxidative phosphorylation in mitochondria, it is demonstrated that conversion processes between ADP and ATP can be detected by the IR spectral changes of phosphate groups in adenine nucleotides.

P-11-4

Rapid Biosensing Platform based on Monitoring Changes in the Optical Reflectance of Porous Silicon due to Penetration by Functionalized Superparamagnetic Beads

P. J. Ko¹², Y. Morimoto¹, R. Ishikawa¹², B. Cho³, H. Sohn³ and A. Sandhu^{12,4}, ¹Tokyo Tech, ²Tokyo Tech. Global COE program, ³Chosun Univ. and ⁴Toyohashi Univ. of Tech. (Japan) We demonstrated the feasibility of a novel biosensing method utilizing superparamagnetic beads for medium varving index reflectivity of PSi.

P-11-5

Differential setup of light-addressable potentiometric sensor with an enzyme reactor

K. Miyamoto¹, M. Yoshida¹, T. Wagner¹, Y. Tatsuo¹ and M. J. Schöning^{2,3}, ¹Tohoku Univ., ²Aachen Univ. of Applied Sciences and ³Research Centre Jülich (Japan)

The light-addressable potentiometric sensor was applied for the differential measurement in flow channels to detect enzymatic reactions. The differential measurement was demonstrated to suppress the drift in the sensor signal.

P-11-6

Optimization of Urea-EnFET Based on Ta2O5 Layer with Post Annealing

T. C. Yu¹, C. E. Lue¹, W. Y. Chuang¹, C. M. Yang², D. Pijanowska³ and C. S. Lat¹, ¹Chang Gung Univ., ²Device Section, Department of WAT and Devices, Inotera Memories Inc. and ³Institute of Biocybernetics and Biomedical Engineering, Polish Academy of Sciences (Taiwan)

In this study, the highest performance of pH sensitivity, hysteresis, drift, and light induced drift, were observed on Ta2O5-ISFET with post N2 annealing. In addition, for the application of urea detection, the best sensing properties were also performed on the EnFET based on the annealed Ta2O5 layer.

P-11-7

A study of olfactory signal sensing with FET biosensor

M. S. Kim¹, W. J. Cho¹, J. Y. Choi² and J. O. Lim², ¹Kwangwoon Univ. and ²Kyungpook National Univ. (Korea)

In this study, we fabricated and investigated field effect transistors (FETs) with living olfactory neural cells of rat pup (day 0.5~1) for real-time diagnosis of chronic obstructive pulmonary disease.

P-11-8

Impact of Quantum Mechanical Effects on Silicon Nanowire Biosensors

B. K. Y. Lu and P. Su, National Chiao Tung Univ. (Taiwan) In this work, we investigate the impact of Quantum mechanical effects on Si-NW biosensors. Our results indicate that by exploiting the O.M. effect, the sensitivity of Si-NW biosensors can be enhanced.

P-11-10

Novel Reference Electrode-Insulator-Nitride-Oxide-Semiconductor (RINOS) Structure with Sm₂O₃ Sensing Membrane for pH-sensor Application

H. Y. Shih, J. Č. Wang, T. F. Lu, Č. S. Lai, C. H. Kao and T. M. Pan, Chang Gung Univ. (Taiwan) In this article, a novel RINOS device with ONO (oxide-nitride-oxide) structure was proposed with the Sm2O3 as the sensing membrane. Through voltage stress, the great improvement on the pH-sensitivity compared with the fresh sample is obtained.

P-11-11

Compact Electro-Magnetically Operated Microfluidic System for Detection of sub-200 nm Magnetic Labels for Biosensing without External Pumps

T. Takamura¹, Y. Morimoto¹ and A. Sandhu¹², ¹Tokyo Tech and ²Toyohashi Univ. of Tech. (Japan) We demonstrated a novel biosensing protocol based on mon-itoring the electrostatic manipulation and magnetic capture of 2.8 micrometer diameter superparamagnetic columnar beads used as a probe by the 130-nm-diameter target beads in pumpless liquid microchannels.

P-11-12

Monodisperse silver nanoparticles of controlled size for biomedical applications

A. P. Z. Stevenson¹, D. B. Bea², S. A. Contera¹, A. I. Cerbeto² and S. Trigueros¹, ¹Univ. of Oxford and ²National Center for Scientific Research (UK)

We present the characterization of monodisperse silver, silver-functionalized and silver-alloy nanoparticles of controlled size synthesized via a novel one-step optimization of the citrate-reduction method.

P-11-13

Fabrication of various metallic nanogap electrodes using molecular ruler technique

T. Nishino^{1,2}, R. Negishi³, H. Tanaka³, T. Ogawa³ and K. Ishibashi^{1,2}, ¹RIKEN, ²Chiba Univ. and ³Osaka Univ. (Japan)

In addition to conventional nanogap electrodes, Au-Au and Pt-Pt, we demonstrated the fabrications of Al-Al, Nb-Nb, Co-Co, and asymmetric Nb-Co nanogap electrodes using molecular ruler technique the methods of which were improved. We show these methods and single electron transport properties of nanogap applying device.

P-11-14

Study of electronic structure of catalyst at Triple Phase Boundary in the cathode catalyst layer of PEFCs by using computational chemistry method

D. Kim, H. Kobayashi, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)

It is necessary to design high-efficient catalyst for implementation of polymer electrolyte fuel cells expected as a sustainable energy technology. It is important to study about the Triple Phase Boundary of catalyst layer and estimate the effect of interface on catalyst properties. In this study, we constructed the TPB model and analyzed the catalyst properties by using computational chemistry method.

| | | P-1 |
|------------|---|-----|
| | Area 12: Spintronic Materials and Devices | Sin |
| (6 Papers) | gro | |

P-12-1

Power-Aware Bit-Serial Binary Content-Addressable Memory Using Magnetic-Tunnel-Junction-Based Fine-Grained Power-Gating Scheme

S. Matsunaga, M. Natsui, H. Ohno and T. Hanyu, Tohoku Univ. (Japan)

Ultra-low-standby-power bit-serial binary content-addressable memory (CAM) is proposed by using a nonvolatile MTJ-based fine-grained power-gating scheme. Since a single MTJ device is used as not only a storage element, but also a logic-operation element, 1T-1R CAM cell is implemented with simplicity of bit-cell level fine-grained power gating.

P-12-2

Fan-out Value in a Current-Field Driven Spin Transistor

K. Konishi¹, T. Nozaki¹, H. Kubota², A. Fukushima², S. Yuasa², M. Shiraishi¹ and Y. Suzuki¹, ¹Osaka Univ. and ²AIST (Japan)

We proposed novel type of spin transistor, which is driven by current induced magnetic field. We obtained fan-out of 1.2 in this device with an assisting ac magnetic field.

P-12-3

Operational Conditions of Proposed Spin-Photon Memory

V. Zayets, H. Saito, S. Yuasa and K. Ando, AIST (Japan)

High-speed non-volatile optical memory was proposed. It was proved that the recording speed of the memory can reach 2.2 TBit/sec. The low-resistivity contact between Fe nanomagnet and n-GaAs was successfully fabricated.

P-12-4

HCP-disordered CoPt electrode and exchange control layer for MgO based perpendicular magnetic tunnel junctions

W. Lim, S. C. Oh, J. H. Jeong, W. J. Kim, Y. H. Kim, H. J. Shin, J. E. Lee, S. Choi and C. Chung, Samsung Electronics Co., Ltd. (Korea)

This letter presents a study of the perpendicular magnetic tunnel junction consisting of HCP-disordered CoPt electrode and non-magnetic exchange control layer (NM ECL). The insertion of NM ECL such as Ti, Mg, Ru, or Al improved the texture of CoFeB/MgO as well as enhanced the perpendicular magnetization anisotropy of CoPt/CoFeB.

Thursday, September 23

P-12-5 Co Doping Enhanced Giant Magnetocaloric Effect In Mn_{1.5}Co,As Films Epitaxied On GaAs

Ex US, *Nie, K. Meng, S. Wang, L. Chen and J. Zhao, State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences (China)* We found that the Co-doped MnAs films grown on GaAs exhibit enhanced magnetocaloric effect around room temperature with transition temperature tunable by varying Co content, which may be applied in construction of layered magnetic regenerator refrigerators with drastically enhanced refrigerating power.

P-12-6

Magnetic properties of quaternary magnetic semiconductor (Cd,Mn,Cr)Te grown by MBE K. Ishikawa and S. Kuroda, Univ. of Tsukuba (Japan)

The magnetic properties of a quaternary DMS compound (Cd,Mn,Cr)Te were investigated. Thin films of Cd_{1,sey}Mn₂Cr₂Te with a fixed Mn content x ~ 0.2 and varied Cr contents in the range of y = 0 ~ 0.07 were epitaxially grown on a GaAs (001) substrate by MBE. In the magnetization measurements, a ferromagnetic behavior, such as hysteretic loops in the *M*-*H* curves, as well as superparamagnetic features such as the blocking phenomenon in the *M*-*T* curves, were observed in Cd_{1,sey}Mn₂Cr₂Te containing Cr contents less than 1%. The paramagnetic Curie temperature Θ_P changes its sign from negative to positive with the incorporation of Cr. These results suggest that the interaction between Mn spins becomes ferromagnetic due to the presence of a small amount of Cr.

Area 13: Application of Nanotubes, Nanowires, and Graphene (13 Papers)

P-13-1

Operation Mechanism of Single-Wall Carbon Nanotube Network FET Studied by Scanning Gate Microscopy

N. Aoki, T. Yahagi, K. Maeda and Y. Ochiai, Chiba Univ. (Japan)

SWNT network FET has been observed by a high resolution SGM. The SGM responses are obtained only at some specific junctions of SWNTs in the channel region. Such junctions would play an important role for the FET operation.

P-13-2

Simple Fabrication Technique for an Array of Field-effect Transistors Using High-quality asgrown Single-walled Carbon Nanotubes from Dip-coated Catalyst by Substrate Surface Modification

S. Aikawa¹², R. Xiang¹, E. Einarsson¹, S. Chiashi¹, J. Shiomi¹, E. Nishikawa² and S. Maruyama¹, ¹Univ. of Tokyo and ²Tokyo Univ. of Sci. (Japan)

We selectively coated catalyst at the edge of pre-formed electrode by using self-assembled monolayer. An array of field-effect transistor having an as-grown single-walled carbon nanotube from dip-coated catalyst was fabricated and evaluated the properties.

P-13-3

Electrical Performance Improvement of Carbon Nanotube Network Transistors by Direct Microwave Treatment

J. Y. Han¹, U. J. Kim² and W. Park¹, ¹Hanyang Univ. and ²Samsung Advanced. Inst. of Tech. (Korea) This is about the I-V improvement of carbon nanotube network transistor using microwave treatment. Through this method, we dramatically increased on-off ratio of carbon nanotube transistor.

P-13-4

DFT Study on the Adsorption and Dissociation of Hydrogen Peroxide on Fe-filled Single-walled Carbon Nanotubes

J. Moreno^{1,2}, M. David², T. Roman¹, M. Sakaue¹ and H. Kasai¹, ¹Osaka Univ. and ²De La Salle Univ. (Japan)

The adsorption possibilities for hydrogen peroxide on Fe-filled single-walled carbon nanotubes were investigated through density functional theory calculations. Results indicated molecular adsorption followed by dissociative chemisorption where hydrogen peroxide dissociated into hydroxyl radicals.

P-13-5

Investigation of UV Polymerized Fullerene Nano Whisker by ESR and FET Characteristics

T. Dol¹, K. Koyama¹, N. Aoki¹, J. P. Bird² and Y. Ochiai¹, ¹Chiba Univ. and ²Univ. at Buffalo (Japan) We have studied on UV polymerized FNW-FET which remain to perform in air. The results of electron transport qualitatively correspond with ESR results which FNW polymer is closer to metallic.

P-13-6

Dependency of Young's modulus on diameter in Crystalline C70 Nanotubes

T. Tokumine¹, K. Miyazawa² and T. Kizuka¹, ¹Univ. of ⁷Sukuba and ²National Institute for Material Science (Japan) We performed bending tests of individual C70 NTs by in situ TEM. From the measurements of the

force-flexure relationships of the C70 NTs, the Young's modulus was estimated to be 61-110 GPa.

P-13-7

Epitaxial Graphene Field Effect Transistors on SiC substrate with Polymer Gate Dielectric

M. H. Jung, H. Handa, R. Takahashi, H. Fukidome and M. Suemitsu, Tohoku Univ. (Japan) We investigated the electrical characteristics of the graphene FET with a polymer gate dielectric on SiC substrate. The graphene FET shows negative Vdirac shift and a carrier mobility of 580 cm³/vs.

P-13-8

Study on the graphene transfer process from graphitized SiC substrates

S. K. Lim¹, C. H. Cho¹, S. Y. Lee¹, H. J. Hwang¹, C. G. Kang¹, Y. G. Lee¹, J. Ahn² and B. H. Lee¹, ¹Gwangju Inst. of Sci.and Tech. and ²Hanyang Univ. (Korea) Graphene has attracted a great deal of attention due to excellent electrical properties and unique physi-

cal charac-teristics. However, the physical and chemical exfoliation of graphite can produce only a tiny piece of graphene. Thus, the processes to fabricate a large area, high quality, single layer graphene have been studied intensively.

P-13-10

Ellipsoidal Band Structure Effects on Maximum Ballistic Current in Silicon Nanowires

N. Mori^{1,3}, H. Minari^{1,3}, S. Uno^{2,3} and J. Hattori^{2,3}, ¹Osaka Univ., ²Nagoya Univ. and ³CREST-JST (Japan)

An isotropic effective-mass approximation is often used for calculating the subband levels in a silicon nanowire (SiNW) with circular cross-section. In the present study, we investigate the validity and limitation of the isotropic approximations by comparing the maximum ballistic current densities in SiNWs.

P-13-12

Co-existence of Random Telegraph Noise and Single-Hole-Tunneling State in Gate- All-Around PMOS Silicon Nanowire Field-Effect-Transistors

B. H. Hong¹, S. J. Lee¹, S. W. Hwang¹, Y. Y. Lee², D. Ahn², K. H. Cho³, K. H. Yeo³, D. W. Kim³, G. Y. Jin³ and D. Park³, 'Korea Univ, ²Univ. of Seoul and ³Samsung Electronics Co., Ltd. (Korea) we report the co-existence of RTN and single hole tunneling (SHT) state in a PMOS gate-all-around (GAA) silicon nanowire field effect transistors (SNWFWTs). We successfully identify dual SHT states which are switching between themselves by single hole trapping of a hole trap state.

P-13-13

Performance Comparisons of Schottky Barrier Transistors Using Si-, Ge- and Ge-Si Core-Shell Nanowires as Channels

J. Pu, L. Sun and R. Han, Peking Univ. (China)

The characteristics of Si-, Ge- and Ge-Si core-shell nanowire Schottky barrier transistors are simulated. For core-shell devices, most holes tunnel at the source near the heterojuction and transport in the Ge core region, and the drain current is relatively insensitive to barrier heights of source/drain contact.

P-13-15

Enhanced Efficiency of ZnO Nanowires Based Dye-Sensitized Solar Cells with Hetrosensitizer

P. H. Wang', S. J. Wang', K. M. Uang', T. M. Chen', P. R. Wang', T. C. Wang' and R. M. Ko', 'National Cheng Kung Univ. and 'Wufeng Inst. of Tech. (Taiwan) In this work, to increase PCE, we report a tandem structure with two different sensitizer dyes (hetro-In this work, to increase PCE, we report a tandem structure with two different sensitizer dyes (hetro-

sensitizer) as well as ZnO-NWs by a simple hydrothermal growth method for DSSCs.

P-13-17

Synthesis of Co-Doped Fullerene Nanowhiskers and Cobalt-Encapsulated Carbon Nanocapsules D. Matsuura¹, K. Miyazawa² and T. Kizuka¹, ¹Univ, of Tsukuba and ²National Institute for Material

D. Maisuura , K. Miyazawa ana I. Kizuka , Oniv. of isukuba ana National Institute for Material Science (Japan)

It was found that (1) Co-doped FNWs can be synthesized by the liquid-liquid interfacial precipitation method, and (2) Co- and Co₂C-encapsulated CNCs can be synthesized by heating of Co-doped FNWs in a vacuum.

Area 14: Photovoltaics & Power Semiconductor Devices

(12 Papers)

P-14-1

Lateral High-Voltage 4H-SiC MOSFETs

W. S. Lee¹, C. W. Lin⁷, M. S. Yang¹, C. F. Huang¹, J. Gong² and Z. Feng³, ¹National Tsing Hua Univ., ²TongHai Univ. and ³University of South Carolina (Taiwan)

The characteristics of lateral high-voltage 4H-SiC MOSFETs built on the Si-face of a 4H-SiC semiinsulating substrate are reported. DIBL effect in these devices is also investigated.

P-14-2

First Principles Calculations on CSL Grain Boundary Impurities in Multicrystalline Silicon

A. Suvitha, N. S. Venkataramanan, R. Sahara, H. Mizuseki and Y. Kawazoe, Tohoku Univ. (Japan) We have carried out DFT studies on the Sigma 5(210) and Sigma 9 (221) CSL GB of multicrystalline silicon. Energy calculation shows substitution site is the preferred for the transition metals in the GB region of Sigma 5 whereas, in the Sigma 9 GB plane except chromium other metal favors segregation at both the sites.

P-14-4

Material Research on High Quality Passivation Layers with Controlled Fixed Charge for Crystalline Silicon Solar Cells

T. Tachibana¹, T. Sameshima, Y. Iwashita^{1,2}, Y. Kiyota, T. Chikyow², H. Yoshida^{1,4}, K. Arafune, S. Satoh^{1,4} and A. Ogura^{1,4}, ¹Meiji Univ, ³NIMS, ²Univ. of Hyogo and ⁴CREST-JST (Japan) In this study, we evaluated and controlled positive and negative fixed charge in the binary composition oxide thin layers fabricated by the combinatorial pulsed laser deposition

P-14-5

a-Si:H Solar Cell with Hexagonal Nano-Cylinder Array on Glass Substrate

W. C. Tu, Y. T. Chang, C. H. Yang, D. J. Yeh, C. I. Ho and S. C. Lee, National Taiwan Univ. (Taiwan) A simple method of light trapping in a-Si:H solar cells was investigated. By nanosphere lithography, we patterned hexagonal nano-cylinder array on the glass substrate and reported 29% efficiency enhancement compared to the flat solar cell.

P-14-6

Application of sputtered ZnO1-xSx buffer layer for Cu(In, Ga)Se2 solar cells

A. Okamoto, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan) We have applied the $ZnO_{1,s}S_s$ by co-sputtering of ZnO and ZnS, which should have high controllability of the compositional ratios of O and S for the buffer layers of Cu(In,Ga)Se₂ solar cells.

P-14-7

Surface morphology and device performance of CuInS₂ solar cells prepared by single and two step evaporation methods

S. Fukamizu, T. Kondo, Y. Oda, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan) CuInS₄(CIS) films were fabricated by two-step evaporation methods that Cu-rich Cu-In-S deposited at 50 °C in the first step and In-S deposited in the second step to control good flatness and In-rich CIS films.

P-14-8

Improvement of Film Quality in CIS Thin Films Fabricated by Non-vacuum, Nanoparticlesbased Approach

Y. Zhang^{2,2}, M. Ito², A. Yamada¹ and M. Konagai, ¹Tokyo Tech and ²Toppan Printing Corp., Ltd. (Japan)

A new approach to fabricate a high quality CIS thin film has been developed. The fabrication was carried out through using copper selenide (Cu-Se) nanoparticles, indium selenide (In-Se) nanoparticles, with thiourea.

P-14-9

Interpretation of Crossover in J-V Characteristics of Cu(In,Ga)Se₂ Solar Cell Using Lift-off Process

Y. Abe, T. Minemoto and H. Takakura, Ritsumeikan Univ. (Japan)

Although the photo J-V characteristics of the CIGS solar cell using a lift-off process were particular shape, this cause has not been interpreted yet. We investigated thebehavior of photocurrent of the CIGS solar cells.

P-14-10

$Simulation \ of \ temperature \ characteristics \ of \ InGaP/InGaAs/Ge \ triple-junction \ solar \ cell \ under \ concentrated \ light.$

Y. Sakurada, Y. Ota and K. Nishioka, Univ. of Miyazaki (Japan)

Temperature characteristics of InGaP/InGaAs/Ge triple-junction solar cell under concentrated light conditions were calculated using SPICE. We can accurately estimate the temperature characteristics of triple junction solar cells under concentrated light.

P-14-11

Shallow Carrier Trap Levels in GaAsN Investigated by Photoluminescence

M. Inagaki¹, H. Suzuki², A. Suzuki, K. Mutaguchi, A. Fukuyama, N. Kojima¹, Y. Ohshita and M. Yamaguchi, ¹Toyota Technological Inst. and ²Univ. of Miyazaki (Japan) The shallow carrier trap levels in GaAsN grown by chemical beam epitaxy were investigated by the temperature dependence of photoluminescence spectra. N-related trap level is ~17 meV below band edge with independently N composition.

Thursday, September 23

P-14-12

Enhancement of the efficiency of GaAs-based solar cells by sol-gel-synthesized ZnO nanowire arrays as the antireflection layer

Y. K. Su, C. Y. Cheng, J. Y. Huang and Y. W. Lee, National Cheng Kung Univ. (Taiwan) In recent decades, global-warming issues coupled with high oil prices, and photovoltaic is one of green energies which provide electricity without any pollution. We would like to develop high-efficiency and low-cost photovoltaics.

P-14-13

Fabrication of high quality TiO_2 thin films for high conversion efficiency dye-sensitized solar cells by multiple electrophoresis depositions

W. H. Chiu¹, K. M. Lee² and W. F. Hsieh^{1,3}, ¹National Chiao Tung Univ., ²Indus. Tech. Res. Inst. and ³National Cheng Kung Univ. (Taiwan)

A multiple electrophoretic deposition (EPD) for binder-free deposition has been successfully developed to improve the TiO2 photoanode quality, and the device gave a high efficiency up to 6.63% under AM 1.5G one sun irradiation. Thursday, September 23