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A-3: Organic Light Emitting Diodes (Area 10)
(9:00-10:30)
Chairs: S. Naka (Univ. of Toyama)
S. Aratani (Hitachi, Ltd.)

9:00 A-3-1
Improved the power efficiency of white phosphorescent organic light-emitting diode with thin double emitting-layers and hole-trapping mechanism
F. S. Juang[1], S. H. Wang[1], Y. S. Tsai[1], M. H. Gao[1], Y. Chi[2] and H. P. Shieh[3], [1]National Formosa Univ., [2]National Tsing Hua Univ. and [3]National Chiao Tung Univ. (Taiwan)
Highly-efficiency white PHOLED can be achieved by using thin double-emission layers and doping red phosphor on interface between two emission layers. The yield and power efficiency reach 23.5 cd/A and 17.5 lm/w at 1000 cd/m^2.

9:15 A-3-2
Current Density Dependence of Transient Properties in Green Phosphorescent Organic Light-Emitting Diodes
H. Kajii, N. Takahota, Y. Wang and Y. Ohmori, Osaka Univ. (Japan)
We studied the current density dependence of transient characteristics of green phosphorescent OLEDs. We discussed the transient electroluminescence of green phosphorescent OLEDs using pulses of alternating current sine-waves with various frequencies.

9:30 A-3-3
High efficiency phosphorescent organic light-emitting diode by incorporating an electron transport material into emitting layer
F. S. Juang[1], S. H. Wang[1], Y. K. Tsai[1], B. S. Hsieh[1], Y. Chi[2] and H. P. Shieh[3], [1]National Formosa Univ., [2]National Tsing Hua Univ. and [3]National Chiao Tung Univ. (Taiwan)
Hole transport-type host (TCTA) and electron transport material (TmPyPB) incorporated as mixed-host structure to improve the injection of carriers. White PHOLED shown the yield of 32 cd/A and power efficiency of 20 lm/W (1000 cd/m2).

9:45 A-3-4
Enhancing Efficiency of Organic Light-Emitting Diodes Using a CsI-Doped Electron Transporting Layer
T. W. Kuo, S. H. Su, C. M. Wu and M. Yokoyama, I-Shou Univ. (Taiwan)
Metal compound (CsI) is firstly doped into Alq3 film as an ETL in OLED. It reveals an effective way to promote the electron injection into the EML and further enhance the luminous efficiency.

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B-3: High-k Gate Stack (Area 1)
(9:00-10:30)
Chairs: T. Nabatame (NIMS)
K. Shiraishi (Univ. of Tsukuba)

9:00 B-3-1 (Invited)
Atomic mechanism of Flat band voltage shifts by Oxide dipole Layers in High K-Metal Gate Stacks
J. Robertson and L. Lin, Cambridge Univ. (UK)
The atomic mechanism of the flat band voltage shifts by oxide capping layers is obtained from ab-initio calculations. It is due to the group electronegativity effect, and change of screening at the dielectric interface.

9:50 B-3-3
Fermi-level Pinning and NBTI Free of CMOS HfO_2 By Pre-CF_4 Plasma Passivation
H. H. Chiu, C. S. Lai and J. C. Wang, Chang Gung Univ. (Taiwan)
Advanced performance and reliability were achieved with a zero-IL CMOS by CF4 plasma pre-treatment. A new physical model of interfacial reaction suppression and F re-incorporation were presented to explain FLP free and turn-around NBTI phenomenon.

10:10 B-3-4
Enhanced Electrical Uniformity and Breakdown of Multi-Step Deposited and Annealed HfSiO-Insight by Scanning Tunneling Microscopy
K. S. Yew[1], D. S. Ang[1], K. L. Pey[1], G. Bersuker[2], P. S. Lysaght[2] and D. Heh[2], [1]Nanyang Tech. Univ. and [2]SEMATECH (Singapore)
Grain-boundaries in crystallized high-k film have been shown to induce higher voltage loading on underlying IL, therefore accelerating stack breakdown. Through STM characterization, we show directly multi-step deposition and annealing process improve electrical and breakdown performance of high-k film.

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C-3: Tunnel & Schottky-S/D FETs (Area 3)
(9:00-10:30)
Chairs: K. Okano (Toshiba Corp.)
T. Hase (Renesas Electronics Corp.)

9:00 C-3-1 (Invited)
Tunnel FET Promise and Challenges
T. -J. King Liu and S. H. Kim, Univ. of California Berkeley (USA)
This paper reviews recent advancements in tunnel field effect transistor (TFET) technology and assesses its promise for overcoming the energy efficiency limit of CMOS technology. Challenges for practical implementation of low-cost, low-power TFET digital logic are discussed.

9:30 C-3-2
Optimization of Silicon ρ-channel Tunnel FET with Dual κ Spacer
H. Virani, S. Gundapaneni and A. Kottantharayil, Indian Inst. of Tech. (India)
A dual-k spacer concept is proposed and evaluated in underlap and non-underlap p-channel Silicon tunnel FETs for the first time using extensive device simulations. The dual-k spacer consist of an inner layer made of a high k material and an outer layer made of a low-k material.

9:50 C-3-3
Drive Current Improvement in Si Tunnel Field Effect Transistors by means of Silicide Engineering
D. Leonelli[1,2], A. Vandooren[1], R. Rooyackers[1], A. S. Verhulst[1], S. De Gendt[1,2], M. M. Heyns[1,2] and G. Groeseneken[1,2], [1]IMEC and [2]Katholieke Univ. Leuven (Belgium)
We present a novel Si Multiple Gate Tunneling Field Effect Transistor (MuGTFET) with high-k gate dielectric and metal gate with enhanced electric field by silicide encroachment. The pTFET device exhibits a record on-state current of 7μA/μm at VDD of -0.9V and high I_{ON}/I_{OFF} ratio. Temperature measurements and TCAD simulations confirm the presence of multiple transport mechanisms which explain the degradation of the subthreshold swing.

10:10 C-3-4
Metal Schottky S/D Technology of Ultra Thin SOTB (Silicon on Thin Box) MOSFET
A. Shima, N. Sugii, N. Mise, D. Hisamoto, K. Takeda and K. Torii, Hitachi, Ltd. (Japan)
We reports a novel approach to decrease the parasitic resistance in UT-SOI MOSFET utilizing metal Schottky raised-S/D. Selectively deposited NiSi2 with dopant segregation fabricated by laser spike annealing lowered effective SBH and the contact resistance.

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D-3: GaN LED (Area 7)
(9:00-10:45)
Chairs: Y. Ishikawa (Univ. of Tokyo)
N. Iizuka (Toshiba Corp.)

9:00 D-3-1
InGaN-based Blue Light-Emitting Diodes with Electron Blocking Layer Fabricated on Patterned Sapphire Substrates
K. T. Liu[1], C. K. Hsu[2] and S. J. Chang[2], [1]Univ. of Cheng Shiu and [2]National Cheng Kung Univ. (Taiwan)
InGaN-based blue light-emitting diode (LED) with electron blocking layer (EBL) fabricated on patterned sapphire substrate (PSS) have been investigated. It is found that PSS-EBL LED have a 209% enhancement in light output power as compared with that of the conventional LED. The improvement can be attributed to the reduction in dislocation density and the better carrier confinement from EBL.

9:15 D-3-2
Enhanced Light Output of Vertical GaN-Based Light-Emitting Diodes with a Distributed Bragg Reflector and a Roughened GaO_x Surface Film
W. C. Lee[1], K. M. Uang[2], T. M. Chen, D. M. Kuo[1], P. R. Wang, P. H. Wang and S. J. Wang, [1]National Cheng Kung Univ. and [2]Wufeng Inst. of Tech. (Taiwan)
The use of a highly reflective DBR CB layer and surface roughening by KrF excimer laser for the fabrication of high-power VLEDs are demonstrated. Enhancement in Lop by 68% at 350 mA has been obtained.

9:30 D-3-3
Epitaxial-Lateral-Overgrowth of Gallium Nitride for Embedding the Micro-Mirror Array
H. M. Ku[1], C. Y. Huang[1,2], C. Z. Liao[2] and S. Chao[1], [1]National Tsing Hua Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)
We showed the effect of temperature and pressure on the ELOG process for embedding a MMA in GaN. We demonstrated that nearly double the wall-plug efficiency can be obtained for the MQW-LED with the MMA structure.

9:45 D-3-4
High performance GaN-based light emitting diodes grown on 4-inch Si (111)
Y. Zhu, A. Watanabe, L. Lu, Z. Chen and T. Egawa, Nagoya Inst. of Tech. (Japan)
GaN-based LEDs grown on 4-inch Si (111) substrate by MOCVD have been demonstrated. The light output power can be improved by increasing the thickness of n-GaN with the maximum value of 1.7 mW.

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E-3: Flash Memory Ⅱ (Area 4)
(9:00-10:50)
Chairs: Y. Sasago (Hitachi, Ltd.)
M. Moniwa (Renesas Electronics Corp.)

9:00 E-3-1 (Invited)
Current Development Status and Future Challenges of Charge-Trapping NAND Flash
H. T. Lue, K. Y. Hsieh and C. Y. Lu, Macronix International Co., Ltd. (Taiwan)
Although conventional floating gate (FG) Flash memory has already gone into the 2Xnm node, the technology challenges are formidable beyond 20nm. 3D Charge-trapping (CT) NAND is forecasted as a promising solution to continue NAND Flash scaling for another decade. In this paper, technology challenges of 3D CT NAND and the poly-silicon thin film transistor (TFT) issues will be addressed in detail.

9:30 E-3-2
Collective Tunneling Model in Charge Trap Type NVM Cell
M. Muraguchi[1], Y. Sakurai[2], Y. Takada[2], Y. Shigeta[4], M. Ikeda[3], K. Makihara[3], S. Miyazaki[3], S. Nomura[2], K. Shiraishi[2], T. Endoh[1], [1]Tohoku Univ., [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Univ. of Hyogo (Japan)
We propose new tunneling model in the charge trap NVM cell, where the electron collectively tunnels to the trap sites in the programming mode. This insight is very important to design for MLC CT-cell.

10:10 E-3-4
Atomistic Design of Guiding Principles for High Quality MONOS Memories-First Principles Study of H and O Incorporation Effects for N Vacancies in SiN Charge Trap Layers-
K. Yamaguchi, A. Otake and K. Shiraishi, Univ. of Tsukuba (Japan)
We found N vacancies in SiN layer are suitable charge traps for MONOS-type memory based on first principles calculations. N vacancy maintains its high P/E endurance characteristics even when H and O atoms are incorporated.

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F-3: Spin Manipulation and Photon Detection (Area 9)
(9:00-10:45)
Chairs: H. Gotoh (NTT Corp.)
H. Kosaka (Tohoku Univ.)

9:00 F-3-1 (Invited)
Quantum media conversion from a photon to an electron spin
H. Kosaka, H. Shigyou, T. Inagaki, Y. Mitsumori, K. Edamatsu, T. Kutsuwa, M. Kuwahara, K. Ono, Y. Rikitake, N. Yokoshi and H. Imamura, Tohoku Univ. (Japan)
We present a way of quantum media conversion from a photon to an electron together with the reverse conversion from an electron to a photon using a semiconductor quantum structure.

9:30 F-3-2
Spin-relaxation Dynamics of Excited Trion States in an InAs Quantum Dot
Y. Igarashi[1,2], M. Shirane[1,2], Y. Ota[2,3], M. Nomura[2], N. Kumagai[2], S. Ohkouchi[2], A. Kirihara, S. Ishida, S. Iwamoto, S. Yorozu and Y. Arakawa[2,3], [1]NEC Corp., [2]INQIE and [3]Univ. of Tokyo (Japan)
We performed photoluminescence and photon cross-correlation measurements of charged (bi) exciton states in a quantum dot (QD).
Compared with numerical simulations, we evaluated spin-relaxation rates of QD hole-spins.

9:45 F-3-3
Single-Photon Detection by Individual Dopants and the Effect of Channel Shape in SOI-FET
A. Udhiarto[1], D. Moraru[1], R. Nakamura[1], S. Miki[1], T. Mizuno[1], V. Mizeikis[2] and M. Tabe[1], [1]Univ. of Shizuoka and [2]Univ. of Shizuoka (Japan)
We demonstrated single-photon detection by individual dopants in SOI-FET based on trapping and de-trapping of single photo-generated electrons. We show that detection sensitivity can be controlled by channel shape.

10:00 F-3-4
Spin Resonant Tunneling through Quantum Dots with Engineered g-factors
S. M. Huang[1,2], Y. Tokura[3,4], H. Akimoto[1], K. Kono[1], J. J. Lin[2], S. Tarucha[4,5] and K. Ono[1,4], [1]Low temperature physics lab., RIKEN, [2]Inst. of Physics, National Chiao Tung Univ., [3]NTT basic research lab., NTT, [4]Quantum spin information project, ICORP-JST and [5]Univ. of Tokyo (Japan)
We investigate the resonance tunneling through double quantum dots with different g-factors. We found that it is suppressed even though one of the Zeeman sublevels is aligned. The level broadening effect releases the suppression.

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G-3: Modeling, Variation and Reliability (Area 5)
(9:00-10:50)
Chairs: J. C. Guo (National Chiao Tung Univ.)
K. Mizobuchi (Texas Instruments Japan Ltd.)

9:00 G-3-1 (Invited)
A Practical Modeling Solution for Nanodevices with Strain Engineering
D. Chen, R. Lee, U. C. Liu, M. Yeh, B. Huang, M. F. Wang, G. S. Lin, M. K. Tsai, J. H. Lai and C. S. Yeh, UMC (Taiwan)
A compact model solution for layout-dependent effects in advanced CMOS technologies with strain engineering is proposed. Without modeling these effects, the pre-layout and post-layout simulations may have more than 10% difference in device behaviors.

9:30 G-3-2
Analysis of Within-Die and Die-to-Die CMOS-Process Variation With Reconfigurable Ring-Oscillator Arrays
T. Ansari, W. Imafuku, A. Kawabata, M. Yasuda, T. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
Process variations for 180nm CMOS technology in horizontal and vertical chip direction are analyzed with a large ring-oscillator array. Measured within-die variations are found to correlate with simulation results based on the HiSIM model.

9:50 G-3-3
Large Scale Test Circuits for Systematic Evaluation of Variability and Noise of MOSFETs' Electrical Characteristics
Y. Kumagai, K. Abe, T. Fujisawa, S. Watabe, R. Kuroda, N. Miyamoto, T. Suwa, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)
Test circuits that statistically and systematically evaluate variability of Vth, noise, gate leakage current and junction leakage current of MOSFETs are reported.

10:10 G-3-4
A 65nm CMOS 400ns Measurement Delay NBTI-Recovery Sensor by Minimum Assist Circuit
T. Matsumoto[1], H. Makino[1], K. Kobayashi[2] and H. Onodera[1,3], [1]Kyoto Univ., [2]Kyoto Inst. of Tech. and [3]CREST-JST (Japan)
We proposed a NBTI-recovery sensor with 400ns measurement delay which is constructed from a PMOS DUT and two assist NMOSes. It enables high-fidelity NBTI recovery measurement and NBTI recovery follows log t from 400ns.

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H-3: Oxides and Nanowires (Area 8)
(9:00-10:30)
Chairs: A. Yamada (Tokyo Tech)
M. Nakada (OITDA)

9:00 H-3-1
Crack-Free Epitaxial ZnO film on Si(111) with $Gd_2O_3(Ga_2O_3)$ buffer layer
B. H. Lin[1,2], W. R. Liu[1,2], C. C. Kuo[1], C. H. Hsu[2,1], W. F Hsieh[1,3], M. Hong[4] and J. Kwo[4], [1]National Chiao Tung Univ., [2]National Synchrotron Radiation Research Center, [3]National Cheng Kung Univ. and [4]National Tsing Hua Univ. (Taiwan)
In this letter, we report the growth of crack-free epitaxial ZnO films on Si (111) substrates buffered with Gd2O3(Ga2O3) (GGO). The structural properties of ZnO/GGO/Si(111) hetero-epitaxial system was thoroughly examined by X-ray diffraction (XRD) and transmission electron microscopy (TEM).

9:15 H-3-2
Optical properties of ZnO/Au core/shell nano-tips
Y. H. Ko and J. S. Yu, Kyung Hee Univ. (Korea)
We fabricated the Au/ZnO core/shell nano-tips (NTs) by hydrothermal method and thermal evaporation because the Au has excellent stability for acid dye solution in ZnO based dye sensitized solar cells and good capacity to enhance the light absorption.

9:30 H-3-3
Conductance of Zinc Oxide Nanocontacts Studied by In Situ Transmission Electron Microscopy
T. Kase and T. Kizuka, Univ. of Tsukuba (Japan)
We investigated the relationship the structure and measured I-V characteristic of ZnO NCs by in situ TEM. The results show that the ZnO NC not has rectification property but liner relation showed by I-V curve.

9:45 H-3-4
The Role of Aluminum Catalyst Atoms in Shaping the Structural and Electrical Properties of Epitaxial Silicon Nanowires
O. Moutanabbir[1], S. Senz[1], M. Alexe[1], Y. Kim[1], R. Scholz[1], H. Blumtritt[1], C. Wiethoff[2], T. Nabbefeld[2], F. J. Meyer zu Heringdorf[2], M. Horn-von Hoegen[2], D. Isheim[3] and D. N. Seidman[3], [1]Max Planck Institute of Microstructure Physics, [2]Univ. Duisburg-Essen and [3]Northwestern Univ. (Germany)
To date, a variety of metals have been used to synthesis high-density epitaxial Si nanowires through metal-catalyzed vapor phase epitaxy. Understanding the impact of the catalyst on the intrinsic properties of nanowires is critical for precise manipulation of the emerging Si nanowire-based devices.

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I-3: III-V Device Technologies (Area 6)
(9:00-10:30)
Chairs: K. Maezawa (Univ. of Toyama)
Y. Miyamoto (Tokyo Tech)

9:00 I-3-1 (Invited)
Terahertz Oscillating InGaAs/AlAs Resonant Tunneling Diodes
S. Suzuki and M. Asada, Tokyo Tech (Japan)
We report on our recent results of terahertz oscillators using resonant tunnelling diodes. The characteristics of oscillation frequency, output power, and frequency change with bias voltage and frequency modulation utilizing this property are discussed.

9:30 I-3-2
InSb MOS Diodes on a Si (111) Substrate Grown by Surface Reconstruction Controlled Epitaxy
A. Kadoda, T. Iwasugi, K. Nakatani, K. Nakayama, M. Mori and K. Maezawa, Univ. of Toyama (Japan)
Al_2O_3/InSb MOS diodes were fabricated on a Si (111) substrate. Owing to the novel growth technique, good C-V characteristics showing inversion and accumulation were demonstrated.

9:45 I-3-3
Effect of Fluorine Incorporation on WSi_x/Al_2O_3/GaAs Gate Stack
B. S. Ong[1], K. L. Pey[1], C. Y. Ong[1], C. S. Tan[1], C. L. Gan[1], H. Cai[1], D. A. Antoniadis[2] and E. Fitzgerald[2], [1]Nanyang Tech. Univ. and [2]Massachusetts Institute of Technology (Singapore)
We study the effect of fluorine on the dielectric constant and the device performance on WSi_x/Al_2O_3/GaAs gate stack. The dielectric constant of Al_2O_3 decreases but the device performance improves after fluorine treatment.

10:00 I-3-4
Dependence of Optical Response Time on Gate-to-Source Voltage for InAlAs/InAs/InGaAs Pseudomorphic High Electron Mobility Transistors
T. Ando, H. taguchi, K. Uchimura, M. Mochiduki, T. Iida and Y. Takanashi, Tokyo Univ. of Sci. (Japan)
InAs-PHEMTs exhibited an ultra-high optical response, which the minimum value was as low as 8.1×10^{-12} s. From the calculation using the Auger recombination theory, it was found the concentration of holes reaches larger than $2.8\times10^{18}cm^{-3}$.

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J-3: Graphene Photonics and Electronics (Area 13)
(9:00-10:30)
Chairs: T. Otsuji (Tohoku Univ.)
K. Nagashio (Univ. of Tokyo)

9:30 J-3-2
Size and Chirality Dependence on Thermoelectric Properties of Graphene Nanoribbons
W. Huang and G. Liang, National Univ. of Singapore (Singapore)
We have studied the thermoelectric properties of GNRs. We find that chirality plays an important role on thermoelectric properties of GNR, and the results show that GNR potentially can be applied to the cooling devices.

9:45 J-3-3
Performance Potentials of Bilayer Graphene and Graphene Nanoribbon FETs
H. Hosokawa, H. Ando and H. Tsuchiya, Kobe Univ. (Japan)
Graphene is expected as a new channel material for FETs. In this paper, we have performed a comparative study on performance potentials between bilayer graphene- and graphene nanoribbon-FETs based on a first-principles approach.

10:00 J-3-4
Epitaxial Graphene-On-Silicon Logic Inverter
A. E. Moutaouakil[1], H. C. Kang[1], H. Handa[1], H. Fukidome[1,3], T. Suemitsu[1,3], E. Sano[2,3], M. Suemitsu[1,3] and T. Otsuji[13], [1]Tohoku Univ., [2]Hokkaido Univ. and [3]CREST-JST (Japan)
We report on the complimentary logic inverter, using two neighboring back-gate epitaxial graphene-on-silicon FETs. The inverting operation was obtained at as low VDD bias as 0.1V, with a matched output/input voltage.

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K-3: Compound Power Semiconductor Devices (Area 14)
(9:00-10:30)
Chairs: P. Mawby (Univ. of Warwick)
I. Omura (Kyushu Inst. of Tech.)

9:00 K-3-1 (Invited)
Recent Progress in High Voltage MOS-gated Power Transistors in GaN
T. P. Chow, Rensselaer Polytechnic Institute (U.S.A.)
We review the progress in the development of high-voltage MOS-gated power switching FETs in GaN. We present the advantages and disadvantages of various device structures explored. We also discuss technology and reliability issues as well as future trend of GaN vs. SiC for power electronics.

9:30 K-3-2 (Invited)
Progress in SiC Power Semiconductor Devices
T. Shinohe, Toshiba Corp. (Japan)
Silicon carbide (SiC) power semiconductor devices are regarded as the next generation high performance power devices that realize high efficient compact power converters in the various application fields. This presentation shows the current development status of SiC power semiconductor devices and their applications.

10:00 K-3-3
Effects of surface and crystalline defects on reverse characteristics of 4H-SiC JBS diodes
T. Katsuno[1], Y. Watanabe, H. Fujiwara[2], M. Konishi, T. Yamamoto[3] and T. Endo, [1]Toyota Central R&D Labs., Inc., [2]Toyota Motor Corp. and [3]DENSO Corp. (Japan)
Good relations between the reverse characteristics of 4H-SiC JBS diodes and the surface defects were obtained. Micropipe and particle, and carrot-like defect were caused to the low blocking voltage and high leakage current, respectively. Furthermore, the leakage current depended on the threading dislocations.

10:15 K-3-4
High hole current achievement of hydrogen-terminated diamond MOSFETs coated with Poly-tetra-fluoro-ethylene
S. Sato, K. Tsuge, T. Tsuno, T. Ono and H. Kawarada, Waseda Univ. (Japan)
We report that a hydrogen-terminated diamond MOSFET coated with PTFE shows high drain current of -1.2 A/mm and transconductance of 430 mS/mm; the highest value reported in diamond FETs to date.

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L-3: Nano Structures and Devices (Area 11)
(9:00-10:30)
Chairs: M. Sasaki (Toyota Technological Inst.)
S. Sasaki (OMRON Corp.)

9:00 L-3-1 (Invited)
Applications of Nanotechnology in Biomedical Micro/Nano Devices
G. J. Wang, National Chung Hsing Univ. (Taiwan)
Nanobiotechnology is the branch of nanotechnology that has biological and biochemical applications. In this presentation, fabrications of biomedical micro/nano devices such as the orderly nanostructured PLGA scaffold, nano-patterned microvessel scaffold, high aspect ratio alumina-metal coaxial nanorod and nanotube, and high sensitive 3D nanobiosensor using the anodic aluminum oxide templates are introduced.

9:30 L-3-2
Development of Nanoscale Patterning Method of Self-Assembled Monolayer using Photothermal Desorption in Near-field
Y. Yamamoto, Y. Taguchi and Y. Nagasaka, Keio Univ. (Japan)
We have proposed a novel patterning method of self-assembled monolayer (SAM) in nanoscale using near-field photothermal desorption. This paper reports the patterning principle and the validity of the proposed method.

9:45 L-3-3
Positional control of crystal grains in silicon thin film utilizing cage shaped protein
Y. Tojo[1], A. Miura[1,2], I. Yamashita[1,3,4] and Y. Uraoka[1,4], [1]NAIST, [2]National Chiao Tung Univ., [3]Panasonic Corp. and [4]CREST (Japan)
We propose crystallization method of silicon thin film utilizing cage-shape protein. We performed the selective adsorption of Ni ferritins. The location control of crystal grain was successfully achieved with the optimal size at low temperature.

10:00 L-3-4
Control of Activation Energy for Electron Transport in Two-Dimensional Array of Si Nanodisks
M. Igarashi[1], C. H. Huang[1], T. Morie[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]Kyushu Inst. of Tech. (Japan)
The transformation from pulse input signals to decayed analog outputs through 2D array of Si-nanodisks was clearly observed. The activation energy for this transformation in this array could be controlled by changing the nanodisk thickness.

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A-3: Organic Light Emitting Diodes (Area 10)

10:00 A-3-5
Maskless Patterning of Vapor-Deposited Photosensitive Film and its Application to Organic Light-Emitting Diodes
M. Muroyama, W. Saito, S. Yokokura, K. Tanaka and H. Usui, Tokyo Univ. of Agri. and Tech. (Japan)
A patterned of emissive layer (EML) of organic light-emitting diode was prepared by coevaporating carbazole acrylate monomer and photoinitiator followed by UV exposure and rinsing in a solvent. It was found that the patterning process polymerizes the EML and stabilizes the device characteristics and can be repeated to prepare multiple patterns.

10:15 A-3-6
Direct Probing of Carrier Behavior in Electroluminescence IZO/α-NPD/Alq3/LiF/Al Diode by Time-Resolved Optical Second-Harmonic Generation
D. Taguchi, L. Zhang, J. Li, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
By using electric-field-induced optical second-harmonic generation and transient electroluminescence (EL) measurements, we directly probed carrier transient leading to EL in organic light-emitting diodes. The charging-/discharging-time at multi-layer interface was responsible for EL response time.

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B-3: High-k Gate Stack (Area 1)

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C-3: Tunnel & Schottky-S/D FETs (Area 3)

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D-3: GaN LED (Area 7)

10:00 D-3-5
GaN based Light Emitting Diode with Enhanced Optical Output and Improved Luminescence by employing Excimer Laser Irradiation in contact formation
G. H. Wang[1], T. Sudhiranjan, T. C. Wong, X. Wang[2], H. Y. Zheng, T. K. Chan[3], T. Osipowicz and Y. L. Foo[1], [1]Inst. of Materials Res. And Eng., [2]Singapore Inst. Of Manufacturing Tech. and [3]National Univ. of Singapore (Singapore)
We report the fabrication of laser annealed p contact on GaN for enhanced optical output from LEDs. At an optimal laser fluence, excimer laser irradiation led to contact resistivity reduction, resulting in a lower turn on voltage. LEDs with laser annealed contacts further show 2.3 times enhanced electroluminescence in the blue light region.

10:15 D-3-6
Light Emission Enhancement of GaN-Based Photonic Crystal With Ultraviolet AlN/AlGaN Distributed Bragg Reflector
C. C. Chen[1], J. R. Chen[1], Y. C. Yang[2], M. H. Shih[1,2] and H. C. Kuo[1], [1]National Chiao Tung Univ. and [2]RCAS (Taiwan)
We demonstrated two-dimensional photonic crystal band-edge coupling operation with an ultraviolet AlN/AlGaN distributed Bragg reflector (UVDBR). A five-fold enhancement in photoluminescence emission was also achieved at 374 nm wavelength. We also employed the photonic crystal band-edge mode examined with plane-wave expansion (PWE) simulation.

10:30 D-3-7
Light Output Enhancement of Ultraviolet Light Emitting Diodes with Pattern HfO_2/SiO_2 Distributed Bragg Reflector
B. S. Cheng[1], C. H. Chiu[1], M. H. Lo[1], H. C. Kuo[1], T. C. Lu[1], Y. J. Cheng[2] and S. C. Wang[1], [1]National Chiao Tung Univ. and [2]Academia Sinica (Taiwan)
The UVLEDs with pattern DBR structure were fabricated via an e-gun evaporation system and ELOG technique. The luminous intensity of this novel structure can be enhanced approximately 75% than the conventional UVLED structure.

4F 241

E-3: Flash Memory Ⅱ (Area 4)

10:30 E-3-5
Dynamics of the Charge Centroid in MONOS Memory Cells during Avalanche Injection and FN Injection Based on Incremental-Step-Pulse-Programming
J. Fujiki, T. Haimoto, N. Yasuda and M. Koyama, TOSHIBA Corp. (Japan)
we have extracted charge-centroid dynamics during avalanche injection, on the basis of ISPP analysis. We confirmed carriers are trapped near the middle of the charge layer at first and then reach the top interface of the charge layer. In contrast, with higher electric field, carriers are captured near the top interface of the charge layer.

4F 242

F-3: Spin Manipulation and Photon Detection (Area 9)

10:15 F-3-5
Coherent Manipulation and Bi-Directional Polarization of Nuclear Spins in a Quantum Dot Device
R. Takahashi[1,2], K. Kono[1,2], S. Tarucha[3,4] and K. Ono[2,5], [1]Tokyo Tech, [2]RIKEN. [3]Univ. of Tokyo, [4]ICORP-JST and [5]CREST-JST (Japan)
We introduce an electrically pumped bi-directional dynamic nuclear polarization with using a double quantum dot device. We confirmed that directions of this bi-directional polarization can be switched only source-drain voltage. In double quantum dot devices, this bi-directional polarization appears not depending on device structures and materials.

10:30 F-3-6
Transmission Characteristics of a Quantum Point Contact for Edge Magnetoplasmons
K. Washio[1], M. Hashisaka[1], H. Kamata[1,2], K. Muraki[2] and T. Fujisawa[1], [1]Tokyo Tech and [2]NTT Basic Res. Labs. (Japan)
We investigate transmission characteristics of edge magnetoplasmons at a quantum point contact acting as a beam splitter. The obtained transmission characteristics of edge magnetoplasmons are different from conventional tunneling characteristics.

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

1F 211	1F 212	1F 213	2F 221	4F 241	4F 242
Short Presentation P-10 (11:00-12:15) Chairs: E. Itoh (Shinshu Univ.) S. Naka (Univ. of Toyama)	Short Presentation P-1 (11:00-12:15) Chairs: Y. Hayami (Fujitsu semiconductor Ltd.) S. Tsujikawa (Sony Corp.)	Short Presentation P-3 (11:00-12:15) Chairs: Y. Nishida (Renesas Electronics Corp.) F. Boeuf (ST Microelectronics)	Short Presentation P-7 (11:00-12:15) Chairs: J. Fujikata (NEC Corp.) M. Tokushima (AIST)	Short Presentation P-4 (11:00-12:15) Chairs: M. Moniwa (Renesas Electronics Corp.) T. Eshita (Fujitsu Semiconductor Ltd.)	Short Presentation P-9 and P-12 (11:00-12:15) Chairs: K. Ono (RIKEN) Y. Uraoka (NAIST) K. Yagami (Sony Corp.) M. Oogane (Tohoku Univ.)

12:15-13:15 Lunch

Thursday, September 23

4F 243

G-3: Modeling, Variation and Reliability (Area 5)

10:30 G-3-5
Prediction of Circuit Degradation with Transient BTI and HC Simulations
D. Hagishima, T. Ishihara, K. Matsuzawa and K. Masuda, Toshiba Corp. (Japan)
We have developed the circuit simulation coupled with dynamic transistor degradations. Our simulation predicts the circuit characteristics more precisely than the conventional methods by self-consistent calculations between circuit and reliability simulations.

4F 244

H-3: Oxides and Nanowires (Area 8)

10:00 H-3-5
Growth and Characterization of GaAsP Nanowires on GaAs(111)B Substrate by Selective-Area Metal Organic Vapor Phase Epitaxy
S. Fujisawa, T. Sato, S. Hara, J. Motohisa, K. Hiruma and T. Fukui, Hokkaido Univ. (Japan)
To form vertical one-dimensional heterostructure, we fabricated GaAsP nanowires on GaAs(111) B substrates by using selective-area MOVPE. By analyzing the growth conditions, we succeeded in forming nanowire array with good crystal quality.

10:15 H-3-6
Fabrication of Rectifying $Pt/TiO_x/Pt$ by RF-Magnetron Sputtering
N. Zhong[1,2], H. Shima[1,2] and H. Akinaga[1,2], [1]AIST and [2]CREST-JST (Japan)
Rectifying Pt/TiOx/Pt was prepared by RF-magnetron sputtering. An Ohmic contact is always found at BE/TiOx interface due to the intrinsic-dead layer. I-V characteristic of Pt/TiOx/Pt depends on the TiOx/TE interface. Devices with TiOx layer prepared closing to the oxide mode exhibit rectifying properties. By optimize post annealing treatment process, the rectifying ratio at ±1.0V increases from 20 to 4×10^3.

4F 245

I-3: III-V Device Technologies (Area 6)

10:15 I-3-5
Defect-free GaAs/AlGaAs Heterostucture Etching Process by Chlorine/Argon Mixed Gas Neutral Beam
X. Y. Wang[1,3], C. H. Huang[1,3], Y. Ohno[1,3], M. Igarashi[1,3], A. Murayama[2,3] and S. Samukawa[1,3], [1]Tohoku Univ., [2]Hokkaido Univ. and [3]CREST-JST (Japan)
Using chlorine/argon mixed gas neutral beam, we developed a dry etching process for fabricating $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructure with characteristics of defect-free, etching selectivity of $GaAs/Al_{0.3}Ga_{0.7}As$ closes to 1, atomically smooth etched surface, and vertical etch profile.

4F 246

J-3: Graphene Photonics and Electronics (Area 13)

10:15 J-3-5
Study of Hot Carriers in Optically Pumped Graphene
A. Satou[1,3], T. Otsuji[1,3] and V. Ryzhii[2,3], [1]Tohoku Univ., [2]Univ. of Aizu and [3]Japan Science and Technology Agency (Japan)
We studied theoretically hot carriers in optically pumped graphene which can be utilized as THz laser. We showed that the population inversion is possible with sufficiently strong pumping.

2F 222

K-3: Compound Power Semiconductor Devices (Area 14)

2F 223

L-3: Nano Structures and Devices (Area 11)

10:15 L-3-5
Optical Characteristics of Two-dimensional Array of Si Nano-disks Fabricated by Defect-free Neutral Beam Etching with Bio-template
C. H. Huang[1,4], M. Igarashi[1,4], M. F. Budiman[1], R. Oshima[2,4], I. Yamashita[3,4], Y. Okada[2,4] and S. Samukawa[1,4], [1]Tohoku Univ., [2]Univ. of Tokyo, [3]NAIST and [4]CREST (Japan)
We created a 2D Si-ND array with a high-density and well-ordered arrangement using bio-template. The *Eg* and PL emission peaks can be easily controlled by changing the ND thickness.

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

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Short Presentation
P-5 (11:00-12:15)
Chairs: S. Sugawa (Tohoku Univ.)
T. Koide (Hiroshima Univ.)

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Short Presentation
P-2 and P-8 (11:00-12:15)
Chairs: Y. Hayashi (Renesas Electronics Corp.)
N. Nakano (Keio Univ.)
A. Yamada (Tokyo Tech)
H. Hibino (NTT Basic Res. Labs.)

4F 245
Short Presentation
P-6 (11:00-12:15)
Chairs: T. Hashizume (Hokkaido Univ.)
S. Tanaka (Shibaura Inst. Tech.)

4F 246
Short Presentation
P-13 (11:00-12:15)
Chairs: J. Motohisa (Hokkaido Univ.)
S. Uno (Nagoya Univ.)

2F 222
Short Presentation
P-14 (11:00-12:15)
Chairs: K. Ohdaira (JAIST)
K. Nishioka (Univ. of Miyazaki)

2F 223
Short Presentation
P-11 (11:00-12:15)
Chairs: Y. Taguchi (Keio University)
I. Yamashita (NAIST)

12:15-13:15 Lunch

Thursday, September 23

1F 211

A-4: Organic Memory and Related Materials (Area 10)
(15:10-16:25)
Chairs: K. Kato (Niigata Univ.)
S. H. Su (I-Shou Univ.)

15:10 A-4-1 (Invited)
Molecular Memory Nano-interfaced with Organic Molecules
H. Lee[1] and M. H. Jung[2], [1]SungKyunkwan Univ. and [2]Electronics and Telecommunications Res. Inst. (Korea)
For the demonstration of new concept of organic nonvolatile memory devices, herein we report an OFET memory device built on a silicon wafer and based on films of pentacene and a SiO2 gate insulator that are separated by push-pull organic molecules (PPOMs) acting as a gate dielectric. We like to briefly report the design motif and synthesis of PPOMs.

15:40 A-4-2
The dry etching process for patterning P(VDF-TeFE) thin film with various conditions
D. Terashima, J. H. Jeong, C. Kimura and H. Aoki, Osaka Univ. (Japan)
We have used P(VDF-TeFE) thin film for piezo-electric micro-generator. Increasing the surface area, the film was etched by dry etching processes. In this study, we changed the dry etching conditions and observed its variation.

15:55 A-4-3
The influence of the intensity of an electric field on properties of P(VDF-TeFE) thin films during the annealing process
J. H. Jeong, D. Terashima, C. Kimura and H. Aoki, Osaka Univ. (Japan)
To improve properties of P(VDF-TeFE) thin film, we have carried out the annealing process at a temperature higher than melting point with an electric field. In this study, we have studied the relationship between the film properties and the intensity of an electric field on the annealing process.

16:10 A-4-4
Carrier Transport in Electrical Bistable Device based on Hyperbranched Polymer and Gold Nanoparticle Composite Thin Films
H. Ichikawa[1], K. Yasui[2], M. Ozawa[2], K. Ôdoi[2] and K. Fujita[1], [1]Kyushu Univ. and [2]Nissan Chemical Indus. Ltd. (Japan)
Organic electrical bistable devices utilizing hyper-branched polymer and metal nanoparticle composite has been investigated. It is suggested that the conductivity of this device depends on tunnel current, according to the temperature dependency.

1F 212

B-4: Process Integration (Area 1)
(15:10-16:20)
Chairs: J. Yugami (Renesas Electronics Corp.)
S. Tsujikawa (Sony Corp.)

15:10 B-4-1 (Invited)
High-k/Metal Gate Technology toward 14nm generation
M. Takayanagi, Toshiba America Electronic Components, Inc. (USA)
High-k/metal gate technology for current node is reviewed. In addition, remaining challenges and perspective to future node toward 14nm generation is discussed in this paper.

15:40 B-4-2
Analytical Approach for Enhancement of nMOSFET Performance with Si:C Source/Drain Formed by Molecular Carbon Ion Implantation and Laser Annealing
T. Yamaguchi, Y. Kawasaki, T. Yamashita, N. Miura, M. Mizuo, J. Tsuchimoto, K. Eikyu, K. Maekawa, M. Fujisawa and K. Asai, Renesas Electronics Corp. (Japan)
The channel strain induced by Si:C-S/D formed using molecular carbon ion implantation and laser annealing was successfully measured by UV Raman spectroscopy. It was also confirmed that the performance of nMOSFETs is effectively improved by strained Si:C-S/D.

16:00 B-4-3
Mechanism to Achieve PMOS and NMOS Band Edge Work Function using Low Temperature Tuning Process for Low Power Application
C. S. Park[1], G. Bersuker[1], T. Ngai[1], J. Huang[1], K. H. Lin[2], J. Barnett[1], J. Price[1], K. Rader[1], P. Lysaght[1], B. Taylor[1], P. D. Kirsch[1] and R. Jammy[1], [1]SEMATECH and [2]UMC (USA)
Band edge work function metal gates for N- and P-MOSFETs, respectively, were achieved at low EOT with excellent gate leakage through the low temperature process flow using WF tuning techniques.

1F 213

C-4: Tr & SRAM Variabilities (Area 3)
(15:10-16:25)
Chairs: T. Tanaka (Fujitsu Semiconductor Ltd.)
F. L. Yang (National Nano Device Labs.)

15:10 C-4-1
Effective Suppression of Random-Dopant-Induced Characteristic Fluctuation Using Dual Material Gate Technique for 16 nm MOSFET Devices
K. F. Lee, Y. Li, C. Y. Yiu and T. T. Khaing, National Chiao Tung Univ. (Taiwan)
Threshold voltage (Vth) fluctuation has become a crucial problem for nowadays nano-CMOS devices. The random dopant fluctuation (RDF) has shown as the major source of variation. Suppression of RD-induced Vth fluctuation is urgent for variability of sub-22-nm device technologies. Dual material gate (DMG) was recently proposed to improve device performance.

15:30 C-4-2
High Temperature Characteristic of Radom Variability of Drain Current in Scaled FETs
T. Tsunomura[1], A. Kumar[2], T. Mizutani[2], A. Nishida[1], K. Takeuchi[1], S. Inaba[1], S. Kamohara[1], K. Terada[3], T. Hiramoto and T. Mogami[1], [1]MIRAI-Selete, [2]Univ. of Tokyo and [3]Hiroshima City Univ. (Japan)
High temperature characteristic of random variability of drain current is analyzed. It is clarified that the drain current variability decreases at high temperature. This reduction is mainly due to the current onset component.

15:50 C-4-3
Device Engineering to Improve SRAM Static Noise Margin
J. Luo[1], L. Wei[1], F. Boeuf[2], D. Antoniadis[3], T. Skotnicki[2] and H. S. P. Wong[1], [1]Stanford Univ., [2]STMicroelectronics and [3]MIT (USA)
We examine the impact of device I-V characteristics on SRAM SNM by analyzing the switching trajectories. 12% improvement in both read and write SNM are achieved by decreasing the transistor DIBL from 150mV/V to 50mV/V.

16:10 C-4-4 (Late News)
Qualitative Differences Between Conduction Band Edge Excitonic States and Electron Tapping in (i) SiO_2 and (ii) Si_3N_4 and Si Oxynitride Alloy Films
G. Lucovsky, NC State Univ (USA)
Many electron wavefunctions and X-ray absorption spectrocopy are combined to provide sigifincant information about band edge, and O and N vacancy defects.

2F 221

D-4: Photonic Crystal Devices (Area 7)
(15:10-16:25)
Chairs: M. Tokushima (AIST)
N. Iizuka (Toshiba Corp.)

15:10 D-4-1 (Invited)
Information processing and sensing with photonic crystal microcavities in SOI
P. M. Fauchet, Univ. of Rochester (USA)
The optical transmission in 2-D photonic crystal microcavities made in SOI is strongly affected by a small change in the refractive index inside the defect hole. This principle has been used to develop biosensors capable of detecting tiny amounts of biological targets such as a single virus, and electro-optic (E-O) modulators that require only ~1 fJ of electrical energy to switch an optical bit.

15:40 D-4-2
Pulse selection by on-the-fly wavelength conversion in 2D photonic crystals
T. Asano, J. Upham, Y. Tanaka and S. Noda, Kyoto Univ. (Japan)
We propose and demonstrate an application of ultrafast on-the-fly wavelength conversion technique developed previously. We selectively deflect an input light pulse from a photonic crystal waveguide by combining that technique and a photonic crystal nanocavity.

15:55 D-4-3
Demonstration of a Silicon photonic Crystal Slab LED with Efficient Electroluminescence
S. Nakayama, S. Iwamoto, S. Ishida and Y. Arakawa, Univ. of Tokyo (Japan)
We report the first demonstration of silicon photonic crystal (PhC) LEDs. Lateral p-i-n diodes with PhC structures were fabricated and efficient electroluminescence was observed from this structure compared to that without PhC patterns.

16:10 D-4-4
Optimized Micro-Cavity and Photonic Crystal in GaN-based Thin-Film Light-Emitting Diodes for Highly Directional Beam Profiles
C. F. Lai, C. H. Chao and W. Y. Yeh, Indus. Tech. Res. Inst. (Taiwan)
Highly directional far-fields of GaN PhC ultra-thin film LED (uTFLED) have been demonstrated. Output power enhancement of ~3.78x compared to non-PhC uTFLED and highly directional far-field with half intensity angle of ±17°have been achieved.

4F 241

E-4: Flash Memory Ⅲ (Area 4)
(15:10-16:10)
Chairs: Y. C. Chen (Macronix International Co., Ltd.)
T. Endoh (Tohoku University)

15:10 E-4-1
Y-disturb Study of Charge-trapping Type Non-volatile Memory Cell for 45nm Generation Node
T. F. Ou, C. H. Cheng, W. C. Tzeng, G. D. Lee, S. H. Ku, C. H. Liu, K. W. Liu, N. K. Zous, W. J. Tsai, S. W. Huang, M. S. Chen, W. P. Lu, K. C. Chen and C. Y. Lu, Macronix Intl Co., Ltd. (Taiwan)
In 45nm virtual ground array, the disturbance in the width direction is mainly induced by secondary hot electrons. Fine tuning the junction implantations or increasing the program WL bias can effectively improve the disturbance.

15:30 E-4-2
In-Depth Study on Mechanism of the Performance Improvement by High Temperature Annealing of the Al_2O_3 in a Charge-Trap Type Flash Memory Device
J. K. Park[1], Y. Park[1], S. K. Lim[2], J. S. Oh[2], M. S. Joo[3], K. Hong[3] and B. J. Cho[1], [1]KAIST, [2]National Nanofab Center and [3]Hynix Semiconductor Inc. (Korea)
In TANOS device, enhanced retention property upon high temperature oxygen annealing can be contributed to not suppressing the trap-assisted tunneling current but changes of the conduction band offset of the crystallized Al2O3.

15:50 E-4-3
POST-BREAKDOWN RECOVERABLE METAL NANOCRYSTAL-BASED AL_2O_3/SIO_2GATE STACK FOR NON-VOLATILE MEMORY
*Y. N. Chen[1,2], K. L. Pey[1], K. E. J. Goh[2], Z. Z. Lwin[1], P. K. Singh[3], S. Mahapatra[3], Q. X. Wang[4] and J. Zhu[4], [1]Nanyang Tech. Univ., [2]Inst.of Material Res.and Eng., A*STAR, [3]Indian Inst.of Tech. and [4]GlobalFoundries Singapore Pte. Ltd (Singapore)*
Recovery of electrical performance in post-breakdown Ru metal nanocrystal-based high-k/SiO2 non-volatile memory gate stack is realized with electrical methods. A physical model based on oxygen vacancy annihilation is proposed for the recovery mechanism.

4F 242

F-4: Quantum Dots (Area 9)
(15:10-16:25)
Chairs: T. Fujisawa (Tokyo Tech.)
A. Dzurak (Univ. of New South Wales)

15:10 F-4-1 (Invited)
Spin-based Quantum Information Processing in Silicon
A. S. Dzurak, Univ. of New South Wales (Australia)
We review electron spin qubits in silicon based on both dopant atoms and gate-defined quantum dots. Single-shot readout of an electron spin in Si was demonstrated using implanted P donors tunnel-coupled to a Si SET. Readout fidelity was > 90% and spin lifetime T1 ~ 6 s. Measure-ments of valley splitting and spin filling in Si MOS quan-tum dots will also be discussed.

15:40 F-4-2
Simulation study of charge modulation in coupled quantum dots in silicon
T. Kambara[1], T. Kodera[1,2], G. Yamahata[1], K. Uchida[1] and S. Oda[1,2], [1]Tokyo Tech and [2]Univ. of Tokyo (Japan)
We have investigated the number of electrons in Si DQD by simulation with various applied voltages of the top gate and side gates. With optimum gates bias, a few-electron DQD is formed.

15:55 F-4-3
Preparation of SOI-based Double Quantum Dots Structure Defined by Geometry and Electrostatically
M. A. Sulthoni, T. Kodera, K. Uchida and S. Oda, Tokyo Tech (Japan)
We studied two aspects of the fabrication of silicon DQD structure. 3D numerical simulation is used to find optimum structure of such device, and fabrication using electron beam lithography is optimized experimentally.

16:10 F-4-4
Single Electron Transistors (SETs) for Reducing Source/Drain Resistance and MOS Current
J. E. LEE, W. B. Shim, J. G. Yun, K. C. Kang, J. H. Lee, H. Shin and B. G. Park, Seoul National Univ. (Korea)
Since a Metal-Oxide-Semiconductor (MOS) was developed, the scaling down of devices has been the most effective method for the improvement of device performance. However, as the scaling down of devices reaches sub-micron region, it reveals problems such as the short channel effect and power consumption.

Thursday, September 23

4F 243

G-4: Advanced Analog Circuits (Area 5)
(15:10-16:25)
Chairs: T. Hirose (Kobe Univ.)
T. Koide (Hiroshima Univ.)

15:10 G-4-1
A Gate-drain Coupling Distributed Amplifier in 90-nm CMOS Technology
C. Y. Hsiao, W. B. Y. Wang, T. Y. Su, Y. C. Wu and S. S. H. Hsu, National Tsing Hua Univ. (Taiwan)
This paper proposed a distributed amplifier in 90-nm CMOS technology, using the gate-drain transformer coupling and pattern ground folded layout method to achieve high gain-bandwidth of 137.2 GHz and minimized chip size of 0.97x0.42 mm2.

15:30 G-4-2
A 60dB SFDR Low-Noise Amplifier with Variable Bandwidth for Neural Recoding Systems
K. Sueishi[1], T. Yoshida[1], A. Iwata[2], K. Matsushita[3], M. Hirata[3] and T. Suzuki[4], [1]Hiroshima Univ., [2]A-R-Tech Corp., [3]Osaka Univ. and [4]Univ. of Tokyo (Japan)
Recently, a brain machine interface (BMI) /brain computer interface (BCI) has been researched in order to restore communication function for the severely disabled people due to amyotrophic lateral sclerosis, spinal injury, brain stroke etc. Especially, Electrocorticograms (EcoG) is attracting attention as a key signal to realize these systems.

15:50 G-4-3
Temperature Compensated Nano-Ampere CMOS Current Reference Circuit Using Small Offset Voltage
Y. Osaki, T. Hirose, N. Kuroki and M. Numa, Kobe Univ. (Japan)
We developed a low-power current reference circuit with little temperature dependence for micro-power LSIs in a 0.35-μm standard CMOS process.

16:10 G-4-4 (Late News)
Low-voltage Power Supply Regulator for Sub-threshold-operated CMOS Digital LSIs
K. Ueno, H. Shimada, T. Asai and Y. Amemiya, Hokkaido Univ. (Japan)
Our regulator accepted a battery voltage (1-3.3V) and produced a minimum supply voltage (0.5-1.2V) for operating subthreshold logic circuits at a speed determined by a CR reference, regardless of PVT variations.

4F 244

H-4: Carbon Interconnect (Area 2)
(15:10-16:20)
Chairs: M. Nihei (AIST)
M. Matsuura (Renesas Electronics Corp.)

15:10 H-4-1 (Invited)
Thermal Transport in Graphene and Few-Layer Graphene: Applications in Thermal Management and Interconnects
A. A. Balandin, Univ. of California, Riverside (USA)
In this talk I will review the results of our experimental and theoretical investigation of thermal conduction in graphene and few-layer graphene. Graphene applications in interconnects, thermal management and 3D electronics will be discussed.

15:40 H-4-2
Plasma Discharge Condition Dependence of the Crystallographic Quality of Networked Nanographite Grown by the Photoemission-Assisted Plasma-Enhanced CVD
S. Ogawa[1,2], T. Kaga[1], Y. Ohtomo[1], M. Sato[2,3], M. Nihei[2,3] and Y. Takakuwa, [1]Tohoku Univ., [2]CREST-JST and [3]Fujitsu Ltd. (Japan)
In the photoemission-assisted plasma CVD, the crystallographic quality of networked graphite is improved with decreasing the plasma voltage. The considerable reasons are the decrease of growth rate, and the decrease of ion collision to the substrate.

16:00 H-4-3
Carbon Nanotube Growth for Vias and Interconnects
J. Robertson[1], C. S. Esconjauregui[1], B. C. Bayer[1], F. Yan[1], G. Zhong[1], J. Dijon[2] and H. Okuna[2], [1]Cambridge Univ. and [2]CEA (UK)
We achieve nanotube growth densities of 2E12 to 5E12 cm-2 by particular catalyst pre-treatments, for use in Vias and interconnects, the highest achieved to date.

4F 245

I-4: Silicon Carbide Devices (Area 6)
(15:10-16:25)
Chairs: R. Hattori (Mitsubishi Electric Corp.)
T. Hashizume (Hokkaido Univ.)

15:10 I-4-1 (Invited)
SiC Power devices – Recent progress and upcoming challenges
P. Friedrichs, SiCED Electronics Development GmbH & Co.KG (Germany)
The contribution will comment on the role of SiC power semiconductor devices in industrial electronics with a focus on high power densities and efficiency. Device concepts with their pro's and cons will be discussed. After an outlook into the future of high voltage components a discussion about short time applications for SiC devices will be given.

15:40 I-4-2
Recombination Model at Perimeter of Stacking Faults in 4H-SiC pin Diode with Forward Voltage Drift
K. Nakayama[1,3], Y. Sugawara[1], H. Tsuchida[2], C. Kimura[3] and H. Aoki[3], [1]The Kansai Electric Power Co., Inc., [2]Central Research Inst. Of Electric Power Industry and [3]Osaka Univ. (Japan)
The relation between the forward and the reverse recovery characteristics of the pin diode with the forward voltage drift was investigated. The recombination model at perimeter of the stacking faults was proposed and it was revealed that the hole lifetime of pin diode shortened by the recombination at perimeter of the stacking faults.

15:55 I-4-3
Influence of inserting AlN between AlSiON and 4H-SiC interface for the MIS structure on SiC
N. Komatsu, T. Satoh, M. Honjo, T. Futatuki, C. Kimura and H. Aoki, Osaka Univ. (Japan)
An interfacial roughness is suppressed by deposition of AlN on SiC. It is half of interfacial roughness between SiC and thermal oxide. Electrical property is developed by the crystallization of AlN.

16:10 I-4-4 (Late News)
Behavior of in-grown Stacking Faults in 4H-SiC Epitaxial Layer Through Annealing Process
R. Hattori, K. Hamano, J. Moritani, K. Sato and T. Oomori, Mitsubishi Electric Corp. (Japan)
We investigated the behavior of SFs in 4Hn-SiC epi-taxial layer during annealing process with PL topographic imaging inspection. As a conclusion, Single Shockley SFs could be completery recovered by the activation annealing process and other SFs still remain after the process.

4F 246

J-4: Graphene's Electrical Properties (Area 13)
(15:10-16:25)
Chairs: K. Maehashi (Osaka Univ.)
K. Nishiguchi (NTT Basic Res. Labs.)

15:10 J-4-1 (Invited)
DOS Bottleneck for Contact Resistance in Graphene FETs
K Nagashio, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)
The contact resistance between graphene and metal is crucially important for achieving potentially high performance of graphene from both physics and practical viewpoints. This paper discusses the metal/graphene contact properties by separating from the intrinsic conduction of graphene.

15:40 J-4-2
Graphene layers dependent vibrational property of metal-graphene heterostructures
S. Entani[1], S. Sakai[1], Y. Matsumoto[1], H. Naramoto[1], T. Hao[1], K. Takanashi[1,2] and Y. Maeda[1,3], [1]JAEA, [2]Tohoku Univ. and [3]Kyoto Univ. (Japan)
Influence of the formation of graphene with various metals on its vibrational properties was studied by micro-Raman spectroscopy.It was revealed that the interface interactions are dramatically different between single layer and multilayer graphenes, which will provide a clue to comprehensive understanding of graphene-based devices.

15:55 J-4-3
Observation of bandgap in epitaxial bilayer graphene field effect transistors
S. Tanabe, Y. Sekine, H. Kageshima, M. Nagase and H. Hibino, NTT Corp. (Japan)
Epitaxial bilayer graphene was grown on SiC. Electronic properties of the graphene were studied in a field effect transistor configuration. As a result, bandgap was observed in the transistor.

16:10 J-4-4
Bridging Growth and Electrical Properties of Single Carbon Nanowall
T. Kanda[1], H. Mikuni[1], K. Yamakawa[2], H. Kondo[1], M. Hiramatsu[3], M. Sekine[1] and M. Hori[1], [1]Nagoya Univ., [2]Katagiri Engineering Co., Ltd. and [3]Meijo Univ. (Japan)
Carbon nanowalls are two-dimensional carbon nanomaterials consisting of stacked graphene sheets. In this study, we fabricated a single bridging carbon nanowall and measured the electrical property.

2F 222

K-4: Next Generation Solar Cells (Area 14)
(15:10-16:25)
Chairs: C. A. Kaufmann (Helmhe. Its Zentrum Berlin)
K. Nishioka (Univ. of Miyazaki)

15:10 K-4-1
Optical and Photoelectrical Characterizations of Wide-gap Nanocrystalline Silicon Layers
R. Mentek, B. Gelloz, M. Kawabata and N. Koshida, Tokyo Univ. of Agri. And Tech. (Japan)
Nanocrystalline silicon fabricated by electrochemical etching is under investigation as a new material for wide-gap solar cells. Interesting properties such as band-gap widening and photo-conduction will be presented during this conference.

15:25 K-4-2
Carrier Transfer Simulation on Si/SiC interface in Quantum Dot Solar Cells
S. Hirose, I. Yamashita, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
In this study, we analyzed the carrier transfer on Si-QD/SiC interface by using the quantum chemical calculation and carrier transfer simulation to analyze the influence of interface defect on conversion efficency.

15:40 K-4-3
Development of Multi-Scale Simulation Method for Dye-Sensitized Solar Cells Including Effect of Photoelectrode Material Interface
M. Onodera, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
Dye-Sensitized Solar Cells (DSSCs) are regarded as next-generation solar cells. We have developed a multi-scale DSSC simulator. We developed the calculation part for the effect of the photoelectrode material interface and improved our DSSC simulator.

15:55 K-4-4 (Late News)
Crystalline Silicon Solar Cells Used with Al and Au Metals
T. Sameshima, K. Kogure and M. Hasumi, Tokyo Univ. of Agri. And Tech. (Japan)
We propose a simple crystalline silicon solar cell using Al and Au metals to cause an internal built-in potential in silicon because of their difference of the work functions. No PN junction is necessary. We also used 1.5 nm SiO2 layer for surface passivation. Solar cell characteristics were experimentally demonstrated well.

2F 223

Thursday, September 23

1F 211

A-4: Organic Memory and Related Materials (Area 10)

1F 212

B-4: Process Integration (Area 1)

1F 213

C-4: Tr & SRAM Variabilities (Area 3)

2F 221

D-4: Photonic Crystal Devices (Area 7)

4F 241

E-4: Flash Memory Ⅲ (Area 4)

4F 242

F-4: Quantum Dots (Area 9)

Coffee Break (2F Forum)

1F 211 — A-5: Organic Electronics and Device Physics (Area 10)

(16:50-18:05)
Chairs: K. Fujita (Kyushu Univ.)
H. Usui (Tokyo Univ. of Agri. & Tech.)

16:50 A-5-1
Surface Manipulation of Precursor Carbazole Dendron Polymer Thin Films by Conducting-AFM Nanolithography
A. Baba[1], R. Oyanagi[1], T. Mashima[1], Y. Ohdaira[1], K. Shinbo[1], K. Kato[1], F. Kaneko[1], G. Jiang[2] and R. Advincula[2], [1]Niigata Univ. and [2]Univ. of Houston (Japan)
In this study, conducting AFM nanolithography was used to manipulate the surface morphology of carbazole precursor dendron polymer thin films. Bias voltages were locally applied to the sample by using conducting AFM. We have successfully obtained the locally cross-linked conju-gated polymer due to the polymerization (Cross-linking) and the doping of the polycarbazole.

17:05 A-5-2
Computational Study of Electronic States around Defects in Organic Semiconductors
T. Shimada[1], M. Ohtomo[2], T. Yanase[2] and T. Hasegawa[2], [1]Hokkaido Univ. and [2]Tokyo Univ. (Japan)
We evaluated the electronic states around defects in organic semiconductor crystals. It was found that the thermal fluctuation conceals shallow trap levels originating from defects at high temperature but the trap levels suddenly become active at lower temperatures.

17:20 A-5-3
Preparation of a Hybrid Sensor of Surface Plasmon Resonance and Quartz Crystal Microbalance by Using Imprinted Grating Structure
K. Shinbo, K. Kuroki, Y. Tesuma, Y. Ohdaira, A. Baba, K. Kato and F. Kaneko, Niigata Univ. (Japan)
A hybrid sensor of QCM and SPR methods was prepared and its fundamental property was investigated. Grating structure of CD-R was imprinted on the QCM electrode, and the QCM and SPR property were observed simultaneously.

1F 212 — B-5: Advanced Gate Dielectrics (Area 1)

(16:50-18:10)
Chairs: S. Miyazaki (Nagoya Univ.)
K. Shiraishi (Univ. of Tsukuba)

16:50 B-5-1
Asymmetric Gate-oxide Thickness Four-terminal FinFETs Fabricated using Low-Temperature and Atomically Flat interface Neutral-Beam Oxidation Process
A. Wada[1], K. Endo[2], M. Masahara[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]AIST (Japan)
Flexibly Vth-controllable symmetric and asymmetric Tox 4T-FinFETs with low-temperature neutral beam oxidation process have been successfully fabricated. These results demonstrate the great potential of NBO process for fabricating three dimensional 4T-FinFETs.

17:10 B-5-2
Mobility Degradation and Interface Dipole Formation in Direct-Contact HfO_2/Si MOSFETs
N. Miyata, H. Ishii, T. Itatani and T. Yasuda, AIST (Japan)
The effects of dipoles induced at direct-contact HfO_2/Si interfaces on MOSFTE characteristics was systematically investigated. Mobility degradation was observed in the direct-contact devices, which was attributed to high-k remote scattering rather than the dipole scattering.

17:30 B-5-3
Robust Ultra-violet (UV) Analysis Technique for Band Diagram Extraction of Al/HfGdO/SiO_2/p-Si Structure with Different Hf/Gd Dual-sputtered Ratio
P. C. Chou[1], J. C. Wang[1], C. S. Lai[1], J. Y. Lin[1], W. C. Chang[1], K. T. Chen[1], Y. C. Chung[1], Y. H. Lin[1], I. T. Wang[1], C. I. Wu[2] and P. S. Wang[2], [1]Chang Gung Univ. and [2]National Taiwan Univ. (Taiwan)
In this paper, we for the first time extract the energy band structure of HfGdO gate dielectric layer by using U-V analysis techniques. We successfully obtain the parameters such as energy band gap, valence band, electron affinity, Schottky barrier height, and electron effective mass of the HfGdO films.

1F 213 — C-5: Si Nanowire Technology (Area 3)

(16:50-18:10)
Chairs: N. Mori (Osaka Univ.)
F. L. Yang (National Nano Device Labs.)

16:50 C-5-1
Fully Quantum Study of Silicon Devices with Scattering Based on Wigner Monte Carlo Approach
S. Koba, R. Aoyagi and H. Tsuchiya, Kobe Univ. (Japan)
In this study, we have developed a fully quantum Monte Carlo simulator based on the Wigner transport formalism, and discussed quantum and dissipative transport in Si nanoscale devices.

17:10 C-5-2
Ultra-Thin (4nm) Gate-All-Around CMOS devices with High-*k*/Metal for Low Power Multimedia Applications
J. L. Huguenin[1,2], S. Monfray[1], G. Bidal[1], S. Denorme[1], P. Perreau[3,1], N. Loubet[1], Y. Campidelli[1], M. P. Samson[3,1], C. Arvet[3,1], K. Benotmane[3], F. Leverd[1], P. Gouraud[1], B. Le-Gratiet[1], C. De-Buttet[3,1], L. Pinzelli[1], R. Beneyton[1], S. Barnola[3], T. Morel[1], A. Halimaoui[1], F. Boeuf[1], G. Ghibaudo[2] and T. Skotnicki[1], [1]STMicroelectronics, [2]IMEP and [3]CEA-LETI (France)
We present the successfull integration of high-k/metal self-aligned planar Gate-All-Around with channel thickness down to 4nm. Our devices present state-of-the-art performances and excellent subthreshold characteristics thanks to its surrounding gate.

17:30 C-5-3
Heavily-Doped Poly-Si Gate and Epi-First Source/Drain Extension Technique in Strained Si Nanowire MOSFETs with Reduced Papasitic Resistance
Y. Nakabayashi[1], M. Saitoh[1], T. Ishihara[1], T. Numata[1], K. Uchida[2] and J. Koga[1], [1]Toshiba Corp. and [2]Tokyo Inst. of Tech. (Japan)
Parasitic resistance reduction and current drive enhancement were achieved in nanowire filed-effect-transistors with Epi-first process and compressive stress induced by heavily-doped poly-Si gate. 20% current drive enhancement was obtained compared to conventional process. Heavily-doped poly-Si gate process is additive to the tensile stress liner.

2F 221 — D-5: Quantum Dot (Area 7)

(16:50-18:05)
Chairs: S. Saito (Hitachi, Ltd.)
Y. Ishikawa (Univ. of Tokyo)

16:50 D-5-1
Light emission from a strongly coupled single quantum dot-photonic crystal nanobeam cavity system
R. Ohta, Y. Ota, M. Nomura, N. Kumagai, S. Ishida, S. Iwamoto and Y. Arakawa, Univ. of Tokyo (Japan)
InGaAs single quantum dot-photonic crystal nanobeam cavity coupled system is fabricated and clear cavity QED effect is observed for the first time. PL spectra measured at various detunings show the strong coupling signature at 4K.

17:05 D-5-2
Excited State Bilayer Quantum Dot Lasers at 1.3µm
M. A. Majid[1], D. T. D. Childs, H. Shahid, K. Kennedy, R. Airey, R. A. Hogg, E. Clarke[2], P. Spencer and R. Murray, [1]Univ. of Sheffield and [2]Imperial College (UK)
We report the realization of excited state bilayer QD lasers in the 1.31µm region,offering the opportunity for ultra-high modulation bandwidths. The extension of QD ground-state operating wavelengths to 1.45µm, spans the O and E-band.

17:20 D-5-3
A tunnel injection structure for speeding up carrier dynamics in InAs/GaAs quantum dots using a GaNAs quantum-well injector
C. Y. Jin[1], S. Ohta, M. Hopkinson[2], O. Kojima[1], T. Kita and O. Wada, [1]Kobe Univ. and [2]Univ. of Sheffield (Japan)
A tunnel injection structure has been employed to speeding up carrier dynamics in InAs/GaAs quantum-dots (QD) with a GaAsN quantum well (QW) as a carrier injector. The carrier capture time from the GaAsN QW to QD ground states has been evaluated by time-resolved photoluminescence.

4F 241 — E-5: Flash Memory Ⅳ (Area 4)

(16:50-17:30)
Chairs: E. Yang (eMemory Technology Inc.)
Y. Sasago (Hitachi, Ltd.)

16:50 E-5-1
Investigation of Threshold Voltage Disturbance Caused by Programmed Adjacent Cell in Virtual Source/Drain NAND Flash Memory Device
W. Kim, D. W. Kwon, J. H. Ji, J. H. Lee and B. G. Park, Seoul National Univ. (Korea)
In this paper, we investigate and minimize the threshold voltage disturbance caused by programmed adjacent cell in VSD NAND flash memory device, through the device simulation and measurement data of fabricated arch-shape devices.

17:10 E-5-2
Band Energy Engineered Metal Nanodots Nonvolatile Memory to Achieve Long Retention Characteristics
T. Hiraki, Y. Pei, T. Kojima, J. C. Bea, H. Kino, M. Koyanagi and T. Tanaka, Tohoku Univ. (Japan)
We investigated band energy engineering of metal nanodots memories. We achieved long retention characteristics with tungsten/cobalt double stacked nanodots memory. This result was based on the difference of work-function between tungsten and cobalt.

4F 242 — F-5: New Functional MOS Structures (Area 9)

(16:50-18:05)
Chairs: Y. Takahashi (Hokkaido Univ.)
Y. Uraoka (NAIST)

16:50 F-5-1
Three Dimensional Floating Gate Memory with Multi-layered Nanodot Array Formed by Bio-LBL
K. Ohara[1], B. Zheng[1,2], M. Uenuma[1,2], I. Yamashita[1,2] and Y. Uraoka[1,2], [1]NAIST and [2]CREST-JST (Japan)
I proposed the nanodot-type floating gate memories with multi-layered nanodot layers. Multi-layered nanodot arrays were achieved by Bio-Layer-By-Layer (Bio-LBL) method. Enlargement of memory window of memory was observed by stacking nanodot arrays.

17:05 F-5-2
Switching voltage reduction of resistance switching memory using Si/CaF_2/CdF_2 quantum-well structures
M. Watanabe, Y. Nakashouji and K. Tsuchiya, Tokyo Tech (Japan)
Novel resistance switching diode using Si/CaF2/CdF2/CaF2/Si double heterostructure tunneling barriers and one quantum-well structure. Resistance switching voltage has been successfully reduced around 1V using doping control of a Si barrier layer, where 2.5 - 4V was required when using non-doped Si barrier layer.

17:20 F-5-3
Time dependent analysis of the applied voltage operation for ensuring 10-year lifetime with SiN MOSFET noise source device
M. Matsumoto, T. Tanamoto, S. Yasuda, R. Ohba and S. Fujita, Toshiba Corp. (Japan)
We have theoretically evaluated long-term change in device characteristics of SiN MOSFET from device measurement data on short-term change. It has been found that, to improve the endurance, it is necessary to preclude electron trapping at deep levels by shortening.

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4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-4: Advanced Analog Circuits (Area 5)	H-4: Carbon Interconnect (Area 2)	I-4: Silicon Carbide Devices (Area 6)	J-4: Graphene's Electrical Properties (Area 13)	K-4: Next Generation Solar Cells (Area 14)	

Coffee Break (2F Forum)

G-5: Integrated MEMS/Bio Sensors (Area 5 & 11) — 4F 243

(16:50-18:05)
Chairs: H. Toshiyoshi (Univ. of Tokyo)
K. Sawada (Toyohashi Univ. of Tech.)

16:50 G-5-1 (Invited)
Integrated CMOS-MEMS Technology and its Application.
K. Machida and H. Morimura, [1]NTT AT and [2]NTT Microsystem Integration Laboratories (Japan)
The paper describes the integrated CMOS-MEMS technology and its applications. We discuss the features of the technology. MEMS fingerprint sensor and Low-voltage RF CMOS-MEMS switch are demonstrated as the applications.

17:20 G-5-2
Polarization Analyzing Image Sensor with Monolithically Embedded Polarizer using 65nm CMOS Process
S. Shishido, T. Noda, K. Sasagawa, T. Tokuda and J. Ohta, NAIST (Japan)
The polarization analyzing sensor is expected to be a solution for analyses of optically active compounds. We designed a polarization analyzing image sensor using 65nm CMOS process. By this sensor, polarization characteristics are successfully measured.

17:35 G-5-3
Design and Fabrication of Smart All-in-one Chip for Electrochemical Measurement
T. Yamazaki[1,2], T. Ikeda[1], M. Ishida[1,3] and K. Sawada[1,3], [1]Toyohashi Univ. of Tech., [2]HIOKI E.E. E. Corp. and [3]JST-CREST (Japan)
An electro-chemical sensor chip with a signal input circuit, a potentiostat and sensor electrodes incorporated was designed and fabricated for the first time. Cyclic voltammetry was demonstrated to acquire electrochemical signals using well-studied ferricyanide solution.

H-5: Cu/Low-k Integration (Area 2) — 4F 244

(16:50-18:00)
Chairs: S. Matsumoto (Panasonic Corp.)
T. Hasegawa (Sony Corp.)

16:50 H-5-1 (Invited)
Advanced Organic Polymers for the Aggressive Scaling of Low-k Materials
M. Pantouvaki[1], L. Zhao[2], C. Huffman[1], N. Heylen[1], Y. Ono[3], M. Nakajima[3], K. Nakatani[3], G. P. Beyer[1] and M. R. Baklanov[1], [1]IMEC, [2]Intel Corp. and [3]Sumitomo Bikelite Co., Ltd. (Belgium)
In this paper the scalability of an organic polymer of k-value of 2.2 is studied in single damascene structures with dielectric spacings ranging from 75 to 30 nm, both with and without Cu diffusion barriers.

17:20 H-5-2
DMOTMDS/MTMOS Multi-Stacked SiOCH films for Super-Low-k and Sufficient Modulus Formed by Damage-free Neutral Beam Enhanced CVD
T. Sasaki[1], S. Yasuhara[1], T. Shimayama[2], K. Tajima[2], H. Yano[2], S. Kadomura[2], M. Yoshimaru[2], N. Matsunaga[2] and S. Samukawa[1], [1]Tohoku Univ. and [2]STARC (Japan)
Multi-stacked film was successfully fabricated by depositing lower k-value and higher modulus layers alternately. By optimizing multi-stacked film, we could obtain a super low-k film with k-value of 1.8 and sufficient modulus of 7Gpa simultaneously.

17:40 H-5-3
Improvement of Variability and Reliability in Low-k/Cu Interconnects by Selectivity Control in Dry-Etching Process
I. Kume, M. Ueki, N. Inoue, J. Kawahara, N. Ikarashi, N. Furutake, S. Saitoh and Y. Hayashi, Renesas Electronics Corp. (Japan)
As dimension of the LSI scales down, precise control of the patterning profile in low-k films becomes a key to keep high reliability and small variability in Cu dual damascene interconnects. Carbon-rich MPS-SiOCH film, along with control of the etching gas, achieved highly selective RIE processes for small variability and high reliability.

I-5: Oxide Devices (Area 6) — 4F 245

(16:50-17:50)
Chairs: S. Sasa (Osaka Inst. of Tech.)
T. Hashizume (Hokkaido Univ.)

16:50 I-5-1
High-Mobility a-IGZO Thin-Film Transistor Using Ta_2O_5 Gate Dielectric
C. J. Chiu, S. P. Chang, C. Y. Lu and S. J. Chang, National Cheng Kung Univ. (Taiwan)
In this paper, we have reported the high performance of an amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor with a high-k dielectric layer on a glass substrate.

17:05 I-5-2
ZnO thin film fabricated by plasma assisted atomic layer deposition
Y. Kawamura[1] and Y. Uraoka[1,2], [1]NAIST and [2]CREST-JST (Japan)
In this study, we fabricated ZnO thin-films using plasma-assisted ALD to improve the performance. Excellent properties were obtained. The effects of plasma condition on film properties were also investigated.

17:20 I-5-3
The Unique Phenomenon in the Amorphous In_2O_3-Ga_2O_3-ZnO TFTs Degradation under the Dynamic Stress
M. Fujii[1], J. S. Jung[2], J. Y. Kwon[2] and Y. Uraoka[1,3], [1]NAIST, [2]Samsung Advanced Inst. of Tech. and [3]CREST-JST (Japan)
We investigated the degradation of a-IGZO TFTs caused by the AC stress. We found that the S value change under the AC stress and this degradation caused by the Negatively-charged Donor like traps.

J-5: Graphene Devices(Area 13) — 4F 246

(16:50-18:05)
Chairs: K. Ishibashi (RIKEN)
S. Sato (AIST)

16:50 J-5-1
Label-Free Immunosensors Based on Aptamer-Modified Graphene Field-Effect Transistors
Y. Ohno, K. Maehashi and K. Matsumoto, Osaka Univ. (Japan)
Aptamer-modified G-FETs were successfully fabricated for label-free immunosensors. IgE aptamers can be immobilized on the graphene surface using linker, which was confirmed by AFM and electrical characteristics. The aptamer-modified G-FETs were electrically detected only target IgE molecules.

17:05 J-5-2
Performance Evaluation of Graphene Nanoribbon Heterojunction Tunneling Field Effect Transistors with various Source/Drain Doping Concentration and Heterojunction structure
H. Da[1], K. T. Lam[1], S. K. Chin[2], G. S. Samudra[1], Y. C. Yeo[1] and G. Liang[1], [1]National Univ. of Singapore and [2]Institute of High Performance Computing (Singapore)
The influence of doping concentration and geometrical parameters on the current-voltage characteristics of HJ GNR TFETs has been theoretically investigated by performing Dirac NEGF approach. It is shown that ION as well as SS can be enhanced by controlling the doping concentration and geometrical parameters.

17:20 J-5-3
Impact of Surface Treatment of SiO_2/Si Substrate on Mechanically Exfoliated Graphene
T. Yamashita, J. Fujita, K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)
The interaction between graphene and SiO_2 surface is critical to improve the mobility as well as the size of graphene. We study the effect of O_2 plasma treatment for SiO_2 surface on the interaction.

K-5: Compound Semiconductor Solar Cells (Area 14) — 2F 222

(16:50-18:05)
Chairs: A. Yamada (Tokyo Tech)
T. Minemoto (Ritsumeikan Univ.)

16:50 K-5-1 (Invited)
Flexible Cu(In,Ga)Se_2 Thin Film Solar Cells and Challenges for Low Temperature Growth
C. A. Kaufmann, R. Caballero, T. Rissom, T. Eisenbarth, T. Unold, R. Klenk and H. W. Schock, Helmholtz Zentrum Berlin für Materialien und Energie (Germany)
Flexible Cu(In,Ga)Se2 (CIGSe) thin film solar cells attract growing interest. Due to light weight, robustness and low cost they are expected to increase the range of terrestrial and space applications. The talk focuses on the fabrication of CIGSe at low process temperatures and the challenges related to this approach.

17:20 K-5-2
First principles calculations of defect formation in In-free photovoltaic semiconductors Cu_2ZnSnS_4 and $Cu_2ZnSnSe_4$
T. Maeda, S. Nakamura and T. Wada, Ryukoku Univ. (Japan)
We calculate the vacancy formation energy in Cu2ZnSnSe4 (CZTSe), and Cu2ZnSnSe4 (CZTS) by first-principles calculation. We compare the defect formation in In-free photovoltaic semiconductors CZTSe and CZTS with that of CuInSe2.

17:35 K-5-3
Kinetics of strain relaxation in lattice-mismatched $In_xGa_{1-x}As$/GaAs heteroepitaxy
T. Sasaki[1], H. Suzuki[2], M. Takahasi[3], S. Fujikawa, I. Kamiya[1], Y. Ohshita and M. Yamaguchi, [1]Toyota Tech. Inst., [2]Univ. of Miyazaki and [3]JAEA (Japan)
In situ X-ray reciprocal space mapping during lattice-mismatched In0.08Ga0.92As/GaAs(001) growth and growth interruption is performed to investigate the extent to which the strain relaxation process is kinetically limited.

1F 211

A-5: Organic Electronics and Device Physics (Area 10)

17:35 A-5-4 (Late News)
Nonvolatile memory thin film transistors using triple polymeric dielectric layers
Y. C. Chen[1], C. Y. Huang[2], C. Y. Cheng[1], H. C. Yu[1], Y. K. Su[1] and T. H. Chang[1], [1]National Cheng Kung Univ. and [2]National Taitung Univ. (Taiwan)
The nonvolatile memory OTFTs with triple dielectric layers have been demonstrated. In our device configuration, the memory effect originates from the charges stored in the interfaces between the dielectric layers and in the -OH groups inside the polymer dielectrics. The transistors have a switchable channel current and long retention time.

17:50 A-5-5 (Late News)
Passivation Effect of Diamond Like Carbon Films for Organic Light-Emitting Diodes
H. Butou, H. Okada and S. Naka, Univ. of Toyama (Japan)
We have studied OLEDs with double-layered inorganic/ DLC as a passivation films. By adding the MoO3 as passivation layer for reducing plasma damage, identical durability that compared to the glass encapsulation was observed.

1F 212

B-5: Advanced Gate Dielectrics (Area 1)

17:50 B-5-4
Stability origin of metastable higher-k phase HfO_2 at room temperature
Y. Nakajima, K. Kita, T. Nishimura, K. Nagashio and A. Toriumi, Univ. of Tokyo (Japan)
The stability origin of the metastable higher-k phase HfO2, and a plausible mechanism of Si-cap PDA to obtain that phase were investigated.

1F 213

C-5: Si Nanowire Technology (Area 3)

17:50 C-5-4
Low GIDL and Its Physical Origins in Si Nanowire Transistors
K. Zaitsu, M. Saitoh, Y. Nakabayashi, T. Ishihara and T. Numata, Toshiba Corp. (Japan)
Gate-induced drain leakage (GIDL) in Si nanowire transistors fabricated on SOI substrates is systematically studied. GIDL current is drastically reduced in nanowire FETs with the nanowire width of around 10 nm, which realizes extremely small off-current devices.

2F 221

D-5: Quantum Dot (Area 7)

17:35 D-5-4 (Late News)
Stimulated Emission in Silicon Fin Light-Emitting Diode
S. Saito[1,3], K. Tani[1,3], T. Takahama[1], M. Takahashi[1], E. Nomoto[1], Y. Matsuoka[1], J. Yamamoto[2,3], Y. Suwa[1], D. Hisamoto[1], S. Kimura[1], H. Arimoto[1,3], T. Sugawara[1], M. Aoki[1], K. Torii[1] and T. Ido[1,3], [1]Hitachi, Ltd., Central Res. Lab., [2]Hitachi Advanced Res. Lab. and [3]PECST (Japan)
We have proposed a Si fin light-emitting diode to realize multiple quantum wells fabricated by Si technologies. The experimental results demonstrate the excellent transport characteristics and efficient electroluminescence in the infrared regime.

17:50 D-5-5 (Late News)
Effects of tunneling barrier width on the electrical characteristic in Si-QD LEDs
T. Y. Kim[1,3], N. M. Park[1], C. J. Choi[2], C. Huh[1], C. G. Ahn[1], G. Y. Sung[1], I. K. You[1] and M. Suemitsu[3], [1]Electronics and Telecommunications Res. Inst., [2]Univ. of Chonbuk and [3]Tohoku Univ. (Korea)
In this work, we investigated the impacts of nitride source on the electrical properties of the Si-QD LEDs. Two nitrogen sources, nitrogen (N2) and ammonia (NH3), have been compared for the PECVD growth of the silicon nitride film, while silane (SiH4) has been commonly used as the silicon source.

4F 241

E-5: Flash Memory Ⅳ (Area 4)

4F 242

F-5: New Functional MOS Structures (Area 9)

17:35 F-5-4
Strong Stark effect of electroluminescence in thin SOI MOSFETs
J. Noborisaka, K. Nishiguchi, Y. Ono, H. Kageshima and A. Fujiwara, NTT Corp. (Japan)
We report electroluminescence from thin SOI MOSFETs when electrons are injected into a thin SOI layer. We observed a large Stark shift of up to approximately 50 meV by applying an electric field normal to the thin SOI layer. Stark effect indicates that quantum confinement in the Si/SiO2 system plays an important role in light emission.

17:50 F-5-5
Drive Current Enhancement with Invasive Source in Double Gate Tunneling Field-Effect Transistors
Y. Yang, P. F. Guo, G. Q. Han, C. L. Zhan, L. Fan and Y. C. Yeo, National Univ. of Singapore (Singapore)
We studied the dependence of TFET performance on source design using a 2D TCAD simulation tool. Use of an invasive source with an optimized shape could be used to realize an increased tunneling region, giving a higher Ion. Applying the invasive source in Ge-source Si-body TFET can further enhance the device performance.

Rump Session (Sanjo Conference Hall)

Rump Sessions (18:30-20:00)

Session A (1st Floor)
"Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?"
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

Session B (Basement Floor)
"Silicon Solar Cells -Their key technologies and future prospects-"
Organizer: T. Fukui, (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech) , A. Masuda (AIST)

Thursday, September 23

4F 243	4F 244	4F 245	4F 246	2F 222	2F 223
G-5: Integrated MEMS/Bio Sensors (Area 5 & 11)	**H-5: Cu/Low-k Integration (Area 2)**	**I-5: Oxide Devices (Area 6)**	**J-5: Graphene Devices(Area 13)**	**K-5: Compound Semiconductor Solar Cells (Area 14)**	
17:50 G-5-4 **Amperometric Electrochemical Sensor Array for On-Chip Simultaneous Imaging: Circuit and Microelectrode Design Considerations** *J. Hasegawa, S. Uno and K. Nakazato, Nagoya Univ. (Japan)* We introduce amperometric sensor circuit array for rapid and simultaneous electrochemical imaging, and also propose a novel microelectrode structure to reduce the time to reach the steady-state current, which is verified by computer simulation.		**17:35 I-5-4** **Novel Passivation Layer for Improvement of Reliability In Amorphous Indium Gallium Zinc Oxide Thin Film Transistors (TFTs)** *S. H. Choi, Y. W. Lee, J. Y. Kwon and M. K. Han, Seoul National Univ. (Korea)* We have proposed and fabricated the a-IGZO TFTs with novel passivation layer consisting of sub-layers with different substrate temperatures. And we have verified that the proposed device could improve bias-illumination stability and enhance the electrical characteristics of a-IGZO TFTs.	**17:35 J-5-4** **Graphene based transversal-gated field effect transistor due to band gap modulation** *S. B. Kumar, T. Fujita and G. Liang, National Univ. of Singapore (Singapore)* We explore a transversal-gated-FET in which an asymmetric electrochemical potential is applied. This potential causes a reduction in the band gap of the AGNR, thus resulting in larger current flow across the device. The device performance is improved by introducing vacancies at the top edge. **17:50 J-5-5 (Late News)** **Effect of Oxidation-induced Tensile Strain on Gate-all-Around Silicon Nanowire Based Single-electron Transistor Fabricated using Optical Lithography** *Y. Sun[1,2], Rusli[1] and N. Singh[2], [1]Nanyang Tech. Univ. and [2]Inst. of Microelectronics (Singapore)* Room temperature silicon nanowire-based single electron transistor was fabricated using optical lithography. Coulomb oscillation is weakened for SiNWs of shorter length, attributed to the lowering of the tunneling barriers due to reduced oxidation-induced tensile strain.	**17:50 K-5-4** **Numerical Analysis of a Solar Cell with a Tensile-Strained Ge as a Novel Narrow Band Gap Absorber** *Y. Hoshina, M. Shimizu, A. Yamada and M. Konagai, Tokyo Tech (Japan)* The solar cell performances of the InGaAs /tensile-strained Ge/ InGaAs double-hetero structure are numerically demonstrated as a thin, low-cost, and lattice-adjustable narrow band gap absorber in future multijunction solar cells.	

Rump Session (Sanjo Conference Hall)

Rump Sessions (18:30-20:00)

Session A (1st Floor)
“Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?”
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

Session B (Basement Floor)
“Silicon Solar Cells -Their key technologies and future prospects-”
Organizer: T. Fukui, (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech) , A. Masuda (AIST)