



Advance Program Part II LATE NEWS PAPERS

Wednesday, October 7

Oral Session

2F Heisei <Naka> Area 1

17:30 B-2-5L Polarized Raman study of mechanical stress distribution in W/TiN metal gate MOSFETs
T. Tada¹, V. Poborchii¹, T. Matsuki², J. Yugami² and T. Kanayama¹, ¹MIRAI-AIST and ²Selete (Japan)

17:45 B-2-6L In Situ Si Wafer Surface Temperature Measurement during Flash Lamp Annealing
Y. Yamada¹, T. Aoyama², H. Chino³, K. Hiraka³, J. Ishii¹, S. Kadoya³, S. Kato², H. Kiyama⁴, H. Kondo⁴, T. Kuroiwa⁴, K. Matsuo⁴, T. Owada⁵, T. Shimizu³ and T. Yokomori⁵, ¹AIST, ²Semiconductor Leading Edge Tech. Inc., ³Chino Corp., ⁴Dainippon Screen Manufac. Co. Ltd. and ⁵Ushio Inc. (Japan)

4F Hirose <Nishi> Area 4

17:50 G-2-6L SONOS-Type Nonvolatile Memory Formed on Epitaxial-Ge Layer on Si Substrate
J. R. Wu, M. L. Wu, L. L. Chen, Y. S. Lin and Y. H. Wu, National Tsing Hua Univ. (Taiwan)

18:05 G-2-7L A 1.2V Operation 2.43 Times Higher Power Efficiency Adaptive Charge Pump Circuit with Optimized V_{TH} at Each Pump Stage for Ferroelectric (Fe)-NAND Flash Memories
S. Noda¹, T. Hatanaka¹, M. Takahashi², S. Sakai² and K. Takeuchi¹, ¹Univ. of Tokyo and ²AIST (Japan)

2F Heisei <Nishi> Area 5

18:00 C-2-6L A 14GHz AC-Coupled Clock Distribution using Single LC-VCO and Distributed Phase Interpolators
K. Niitsu¹, V. V. Kulkarni¹, K. Shinmo², H. Ishikuro¹ and T. Kuroda¹, ¹Keio Univ. and ²Samsung Electronics Co. Ltd. (Japan)

6F Hagi Area 6

18:00 J-2-7L High-electron-mobility InAs thin layers down to ~ 100 nm obtained by epitaxial lift-off and normal/inverted van der Waals bonding on flexible substrates
H. Takita, M. Akabori and T. Suzuki, JAIST (Japan)

16:30 E-4-3L High Voltage AlGaIn/GaN HEMTs Employing Surface Treatment by Deposition and Removal of Silicon Dioxide Layer
Y. H. Choi, S. J. Kim, Y. S. Kim, M. K. Kim, O. Seok and M. K. Han, Seoul National Univ. (Korea)

3F Keyaki Area 8

17:45 E-5-2L Effect of drain bias stress on the stability of nanocrystalline silicon thin film transistor with various channel length
S. J. Kim, S. G. Park, S. B. Ji and M. K. Han, Seoul National Univ. (Korea)

18:00 E-5-3L Multilayer Epitaxial Lateral Overgrowth of Light Emitting Diode with Anisotropically Etched GaN/sapphire Interface.

M. H. Lo¹, P. M. Tu¹, C. H. Wang¹, H. C. Kuo¹, S. C. Wang¹, H. W. Zan¹, C. Y. Chang¹, S. C. Hsu², Y. J. Cheng² and S. C. Huang³, ¹National Chiao Tung Univ., ²Res. Center for Applied Sci., Academia Sinica and ³Advanced Optoelectronic Technology Inc. (Taiwan)

18:15 E-5-4L InP Ring-shaped Quantum-dot Molecules Grown by Droplet Molecular Beam Epitaxy
W. Jevasuwan, P. Boonpeng, S. Panyakeow and S. Ratanathamphan, Chulalongkorn Univ. (Thailand)

6F Aoi Area 9

18:30 K-5-5L Local Measurements of Photothermal Signals on Polycrystalline Silicon Materials by Dual Sampling Method in Atomic Force Microscopy
K. Hara and T. Takahashi, Univ. of Tokyo (Japan)

4F Hirose <Higashi> Area 10

14:00 F-3-4L Highly Reliable Nano-gap Electrodes for Single Molecule Evaluation
K. Tsutsui, H. Takagi, M. Morita, M. Tokuda, Y. Ito and Y. Wada, Toyo Univ (Japan)

14:15 F-3-5L Fabrication of Electrophoretic Display Driven by Membrane Switch Array
K. Senda^{1,2} and H. Usui², ¹Sumitomo Precision Co., Ltd. and ²Univ. of Tokyo Atricul. & Technol. (Japan)

6F Kaede Area 11

18:30 I-5-5L Deterioration of mechanical characteristics of micro-cantilevers by plasma induced damage
M. Tomura, Y. Yoshida, T. Ono, C. H. Huang and S. Samukawa, Tohoku Univ. (Japan)

3F Keyaki Area 14

16:45 E-4-4L Substantial Reduction of Power Loss in a 14kVA SiC-Inverter
S. Nakata, S. Kinouchi, T. Kitamura, H. Sumitani, M. Imaizumi, T. Takami, T. Oi and T. Oomori, Mitsubishi Electric Corp. (Japan)

6F Kiri Area 8

17:45 H-2-6L Epitaxy of Graphene on Si substrates toward Three-Dimensional Graphene Devices
H. Fukidome¹, Y. Miyamoto¹, H. Handa^{1,2}, R. Takahashi¹, K. Imaizumi¹ and M. Suemitsu, ¹Tohoku Univ. and ²CREST-JST (Japan)

18:00 H-2-7L Micro/nanospheres from polysilsequioxane containing UVB-absorbing group
P. Kidsaneepoiboon and S. P. Wanichwecharunguang, Chulalongkorn Univ. (Thailand)

6F Aoi Area 9

17:45 K-2-8L Enhancement of Electroluminescent Refrigeration by Inserting Carrier Blocking Layers
K. C. Lee and S. T. Yen, National Chiao Tung Univ. (Taiwan)

18:00 K-2-9L Nanogap size control by room-temperature annealing
T. Hayashi and K. Muraki, NTT Corp. (Japan)

4F Hirose <Higashi> Area 10

18:00 F-2-8L Electric double layer gate FETs based on silicon
T. Yanase¹, T. Shimada¹ and T. Hasegawa^{1,2}, ¹Univ. of Tokyo and ²CREST-JST (Japan)

Thursday, October 8

POSTER SESSION (10:30-12:00, 2F Heisei <Naka & Nishi>)

P-10, Area10:Organic Materials Science, Device Physics, and Applications

P-10-26L Fabrication of Solution-Processed TIPS-Pentacene TFTs with Poly(4-vinylphenol) Bank Layer by using Ink-Jet Printing
S. M. Kim¹, M. J. Kim¹, S. R. Park¹, G. S. Ryu³, J. S. Park² and C. K. Song¹, ¹Dept. of Electronics Eng., ²Dept. of Textile Eng. and ³Media Device Lab., Dong-A Univ. (Korea)

Oral Session

2F Heisei <Higashi> Area 1

14:25 A-3-5L Stress variability control by defects suppression of SiGe Source/Drain using novel SiGe epitaxial growth technique
M. Fukuda, Y. Shimamune, M. Nakamura, K. Tanahashi, T. Miyashita, M. Nishikawa, N. Tamura, T. Mori, Y. Nara and M. Kase, Fujitsu Microelectronics Ltd. (Japan)

4F Hirose <Higashi> Area 2

13:15 F-3-1L Effect of Electrode Contacts on Transport in Carbon Nanofiber Interconnects
H. Yabutani¹, T. Yamada¹, T. Saito² and C. Y. Yang¹, ¹Santa Clara Univ. and ²Hitachi High-Technologies Corp. (U.S.A.)

13:30 F-3-2L Mechanism of electromigration and spontaneous formation of single electron transistors at ultrasmall copper nano-junctions
S. Sakata¹, A. Umeno¹, K. Yoshida¹ and K. Hirakawa^{1,2}, ¹Univ. of Tokyo and ²CREST-JST (Japan)

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3F Keyaki Area 14

17:30 E-5-1L Defect-free Isolation on High-Thermal-Conductivity SOI Substrates for Complementary BiCMOS Technology
K. Van Wichelen¹, P. Ong¹, A. Moussa¹, D. Radisic¹, K. Devriendt¹, S. Halder¹, K. Kenis¹, W. Lee¹, B. Vandeveldt¹, C. Soonekindt¹, S. A. Hadi¹, T. Smet¹, S. Van Huylenbroeck¹, S. Decoutere¹, M. Seacrist², M. Ries², V. Drobny³ and R. Wise³, ¹IMEC, ²MEMC and ³Texas Instruments (Belgium)

Friday, October 9

Oral Session

2F Heisei <Nishi> Area 3

10:20 C-6-5L Separation of Interface and Bulk traps in Advanced High-k Gate Dielectric MOSFETs from a Low-Leakage Charge Pumping Technique
E. R. Hsieh¹, Y. H. Chu¹, G. D. Lee¹, S. S. Chung¹, W. M. Lin², C. W. Yang², Y. S. Hsieh², L. W. Cheng², C. T. Tsai² and G. H. Ma², ¹National Chiao Tung Univ. and ²UMC (Taiwan)

2F Heisei <Nishi> Area 3

14:35 C-8-5L Random-Dopant-Induced Static Noise Margin Fluctuation and Suppression in 16-nm-Gate CMOS SRAM Cell
T. Y. Li¹, C. H. Hwang¹ and Y. Li^{1,2}, ¹National Chiao Tung Univ. and ²National Nano Device Labs. (Taiwan)

14:50 C-8-6L A Novel Compact-Model of Quasi-Ballistic Nanowire MOSFETs
K. Natori, Tokyo Inst. Tech. (Japan)

6F Kaede Area 7

16:45 I-9-6L 2 x 2 Thermo-optic Silicon Oxynitride Optical Switch Incorporating the Cascaded Multimode Interference Waveguides
R. W. Chuang^{1,2}, M. T. Hsu¹ and Z. L. Liao¹, ¹National Cheng Kung Univ. and ²National Nano Device Labs. (Taiwan)

4F Hirose <Nishi> Area 9

17:00 G-9-6L Charge transport in single and few layer graphene devices
M. F. Craciun¹, S. Russo^{1,2}, M. Yamamoto¹, J. B. Oostinga^{2,3}, A. Morpurgo³ and S. Tarucha^{1,4}, ¹Univ. of Tokyo, ²Delft Univ. of Tech., ³Univ. of Geneva and ⁴Quantum Spin Information Project, International Cooperative Research Project (Japan)

4F Hirose <Higashi> Area 10

12:00 F-7-6L Characterization of All Printed Single-Wall Carbon Nanotube based Thin-Film Transistor on Plastic Foils using Displacement Current Measurement
M. Jung^{1,2}, K. Jung², S. Y. Lim², K. Lee¹, A. Leonard³, J. M. Tour³, Y. Majima^{1,4} and G. Cho¹, ¹National Sunchon Univ., ²Paru Co. Ltd., ³Rice Univ. and ⁴Tokyo Institute of Tech. (Korea)

13:45 F-3-3L Evaluation of Ferromagnetic Thin Film Noise Suppressor Applied to On-Chip Transmission Lines
S. Muroga, Y. Endo, M. Suzuki, T. Inagaki, Y. Mitsuzuka and M. Yamaguchi, Tohoku Univ. (Japan)

3F Keyaki Area 3

13:15 E-3-1L A Compact Space and Efficient Drain Current Design for Multi-Pillar Vertical MOSFETs
K. Sakui and T. Endoh, Tohoku Univ. (Japan)

13:30 E-3-2L Exploration of Device Design Space to Meet Circuit Speed Targeting 22nm and Beyond
L. Wei¹, F. Boeuf², D. Antoniadis³, T. Skotnicki² and H. S. Philip Wong¹, ¹Stanford Univ., ²STMicroelectronics and ³Massachusetts Inst. of Tech. (USA)

13:45 E-3-3L Variability-Tolerant CMOS Gates Using Functional MOSFETs with Resistive Switching Devices
S. Yamamoto and S. Sugahara, Tokyo Tech. (Japan)

14:00 E-3-4L Characteristic Sensitivity of Multi-Gate and Multi-Fin MOSFETs to Random Dopant Fluctuation and Implication for Digital Circuits
H. W. Cheng¹, C. H. Hwang¹ and Y. Li^{1,2}, ¹National Chiao Tung Univ. and ²National Nano Device Labs. (Taiwan)

6F Kaede Area 5

17:30 I-5-1L Above-CMOS Inductor for Rapid Prototyping of Mixed-Signal SoCs
Y. Omiya, K. Kotani and T. Ito, Tohoku Univ. (Japan)

17:45 I-5-2L Highly-reliable One-chip Signal Processor LSI for One Angular-rate and Two Acceleration Sensor using Dual DSPs
H. Iwasawa¹, M. Matsumoto¹, T. Nakamura¹, S. Asano¹, M. Hayashi² and Y. Kobayashi¹, ¹Hitachi, Ltd. and ²Hitachi Automotive Systems, Ltd. (Japan)

18:00 I-5-3L A New Differential-amplifier-based Offset-Cancellation Sense Amplifier (DOCSA) for High-speed SRAMs in Scaled-down CMOS Technology
H. Ikeda, K. Takeda, M. Nomura and Y. Hayashi, NEC Electronics Corp. (Japan)

18:15 I-5-4L A Continuous-Time Common-Mode Feedback Circuit for High-Gain, Wide-Output-Range Fully-Differential OTAs
T. Konishi, K. Inazu and S. Masui, Tohoku Univ. (Japan)

3F Keyaki Area 6

16:00 E-4-1L Monte Carlo Analysis of Optical Pulse Response of Plasmon-Resonant Terahertz Emitter
K. Kubota¹, E. Sano¹, Y. M. Mezzani² and T. Otsuji², ¹Hokkaido Univ. and ²Tohoku Univ. (Japan)

16:15 E-4-2L Excellent stability of GaN-on-Si HEMTs with 5 μm gate-drain spacing tested in off-state at a record drain voltage of 200 V and 200°C
D. Marcon^{1,2}, M. Van Hove¹, D. Visalli^{1,2}, J. Derluyn¹, J. Das¹, F. Medjdoub¹, S. Degroote¹, M. Leys¹, K. Cheng¹, R. Mertens, M. Germain¹ and G. Borghs^{1,2}, ¹IMEC and ²Katholieke Universiteit Leuven (Belgium)

4F Hirose <Higashi> Area 10

16:45 F-9-5L Air stable organic semiconductors towards flexible organic field-effect transistors
W. Takashima, T. Nagase, S. Nagamatsu, T. Moriguchi, T. Okauchi, K. Mizoguchi, S. Hayase and K. Kaneto, Kyushu Inst. Of Tech. (Japan)

17:00 F-9-6L Electrical Bistabilities of Organic Bistable Device utilizing Hyperbranched Polymer and Gold Nanoparticle composite
H. Ichikawa¹, K. Yasui², M. Ozawa² and K. Fujita¹, ¹Kyushu Univ. and ²Nissan Chemical Industries, Ltd. (Japan)

6F Hagi Area 11

10:15 J-6-6L RFID sensor chips with anticollision algorithm for simultaneous detection of multiple DNA target
Y. Yazawa, T. Oonishi, K. Watanabe, R. Nemoto and A. Shiratori, Hitachi, Ltd., (Japan)

6F Hagi Area 11

17:00 J-9-6L Light-Addressable Potentiometric Sensor with Fluorine Terminated Hafnium Oxide for Sodium Detection
H. Y. Chen, C. E. Lue and C. S. Lai, Chang Gung Univ. (Taiwan)

6F Aoi Area 12

16:45 K-9-4L Observation of Spin Relaxation in InGaAs/AlAsSb Quantum Wells
S. Izumi¹, S. Gozu², T. Mozume², Y. Saeki¹, T. Nukui¹ and A. Takeuchi¹, ¹Waseda Univ. and ²AIST (Japan)

3F Keyaki Area 13

16:45 E-9-5L Silicon Thin Film with Si Nanopillar Surface Decoration for Solar Cell Application
S. M. Wong^{1,2}, H. Y. Yu^{1,2}, J. S. Li^{1,2}, G. Zhang², G. Q. Lo² and D. L. Kwong², ¹Nanyang Tech. Univ. and ²Inst. of Microelectronics (Singapore)

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UPDATED INFORMATION AND CORRECTION

Wednesday, October 7

Oral Session
2F Heisei <Naka> Area 1
17:00 B-2-4 -> 17:10 B-2-4

New Criteria for Suppressing Extrinsic Defect Generation in Ultra Thin SiON Gate Insulator (EOT <1.4nm) for Advanced CMOSFETs
S. Shimamoto1, H. Kawashima2, T. Kikuchi1, Y. Yamaguchi2 and A. Hiraiwa2, 1Hitachi, Ltd. and 2Renesas Tech. Corp. (Japan)

2F Heisei <Higashi> Area3

October 8, 16:00 A-4-1 -> October 7, 15:40 A-1-7 (Invited)
The Tunnel Source n-MOSFET: A Novel Asymmetric Device for Low Power Applications
N. Venkatagirish, A. Tura, R. Jhaveri, H. Y. Chang and J. Woo, UCLA (USA)

Thursday, October 8

Poster Session
6F Aoi Area9

October 9, 16:45 G-9-5 -> October 8, 8:45 P-9-18
Anisotropic Transport in Epitaxial Graphene Transistor on Vicinal SiC Substrate
S. Odaka1,2,3, H. Miyazaki1,3, A. Kanda3,4, K. Morita5, S. Tanaka5, Y. Miyata6, H. Kataura6, K. Tsukagoshi1,3,6 and Y. Aoyagi3,7, 1NIMS, 2Tokyo Tech, 3CREST-JST, 4Univ. of Tsukuba, 5Kyushu Univ., 6AIST and 7Ritsumeikan Univ. (Japan)

Oral Session
2F Heisei <Higashi> Area3

A-4-2 -> A-4-1
Multiple-Gate Tunneling Field Effect Transistors with sub-60mV/dec Subthreshold Slope
D. Leonelli1,2, A. Vandooren1, R. Rooyackers1, A. S. Verhulst1,2, S. De Gendt1,2, M. M. Heyns1,2 and G. Groeseneken1,2, 1IMEC and 2Katholieke Univ. Leuven (Belgium)
A-4-3 -> A-4-2
Novel Source Heterojunction Structures with Relaxed-/Strained-Layers for Quasi-Ballistic CMOS Transistors using Ion Implantation Induced Relaxation Technique of Strained-Substrates
T. Mizuno1,2, N. Mizoguchi1, K. Tanimoto1, T. Yamauchi1, T. Tezuka3 and T. Sameshima4, 1Kanagawa Univ., 2MIRAINRC, 3MIRAI-Toshiba and 4Tokyo Univ. of Agri. and Tech. (Japan)

Friday, October 9

Oral Session
4F Hirose <Nishi> Area9

15:30 G-9-1
AFM nanolithography of graphene
L. Weng, L. Zhang, Y. P. Chen, and L. Rokhinson, Purdue Univ. (USA)

17:00 G9-6 -> 16:45 G-5
Self-Excitation of Terahertz Plasma Oscillations in Optically Pumped Graphene
V. Ryzhii1,3, M. Ryzhii1,3, A. Satou1,3, E. M. Amine2 and T. Otsuji2,3, 1Univ. of Aizu, 2Tohoku Univ. and 3CREST-JST (Japan)

RUMP SESSIONS

Session A (4F Hirose-Higashi)
Moderator: M. Hane (NEC Corp., Japan)
-> Y. Miyamoto (Tokyo Tech, Japan)
Panelist: S. Okazaki (EUVA)
T. Endoh (Tohoku Univ.)
S. Tanaka (Tohoku Univ.)
T. Kozawa (Osaka Univ.)
T. Uchiyama (NEC Electronics Corp.)

Session B (4F Hirose-Nishi)
Moderator: M. Ishiko (Toyota Central R&D Labs., Inc, Japan)
-> Y. Yoshida (AIST, Japan)
Panelist: T. Motohiro (Toyota Central R&D Labs. Inc.)
" What We Can Expect from Solar Cells "
S. Sugihara (Shonan Inst. of Tech.)
" Possibility of Practical Solar Car? - Dankichi and Sunflower - "
S. Uchida (RCAST, Univ. of Tokyo)
" Thin, Light-Weight Flexible Dye Sensitized Solar Cells "
S. Yoshikawa (Sharp Corp.)
" Solar Cells for Mobile Phones "

PROGRAM COMMITTEE

[14] Power Electronics
Member: A. Masuda (NAIST) -> A. Masuda (AIST)

Session Chair

- A-3 I. Yamamoto (NEC Corp.) -> I. Yamamoto (NEC Electronics Corp.)
B-4 I. Yamamoto (NEC Corp.) -> I. Yamamoto (NEC Electronics Corp.)
A-4 Y. Yeo (National University of Singapore) -> H. Wakabayashi (Sony Corp.)
F-5 S. F. Horng (National Tsing Hua Univ.) -> K. Kato (Niigata Univ.)

- H-7 N. Iwamura (Fuji Electric Device Tech. Co., Ltd.) -> Philip A. Mawby (Univ of Warwick)
E-8 Y. Ohno (Nagoya Univ.) -> K. Maehashi (Osaka Univ.)
J-8 M. Niwano (Tohoku Univ.) -> A. Hirano (Tohoku Univ.)
P-3 A. Azuma (Toshiba Corp.) -> S. Inumiya (Toshiba America Electronic Components Inc.)
P-3 M. Hane (NEC Electronics America) -> H. Wakabayashi (Sony Corp.)
P-7 M. Sugawara (Fujitsu Labs. Ltd.) -> H. Yamada (Tohoku Univ.)
P-13 J. Motohisa (Hokkaido Univ.) -> K. Ishibashi (RIKEN)

Session Time

Table with 3 columns: Session Area, Session Title, and Time slot. Includes sessions like 2F Heisei<Higashi> A-1 13:30-16:00, etc.

Session Title

- A-1 SOI/GOI and Channel Engineering -> A-1 SOI/GOI and Channel Engineering
A-3 Source/Drain Engineering -> A3 Source/Drain Engineering
B-4 Hihg-k/Metal Gate I -> B-4 High-k/Metal Gate I
B-5 Hihg-k/Metal Gate I -> B-5 High-k/Metal Gate II

Withdrawn

- P-4-13
P-12-5
I-8-3
P-8-1
P-10-10
P-9-12
P-1-6

SSDM 2009 Time Table

Large table with columns for session areas (2F Heisei, 3F Sakura, 4F Hirose, 5F Keyaki, 6F Kiril, 6F Kaede, 6F Hagl, 6F Aoi) and rows for time slots (10:00-12:00, 13:00-15:45, 16:00-18:00, 19:00-21:00, 8:45-10:30, 10:30-12:00, 13:05-14:40, 15:00-15:45 plenary, 9:00-10:30, 10:35-12:15, 13:15-15:05, 15:20-17:10).