

2009 International Conference on Solid State Devices and Materials
=Short Course=
From Basic Theory to Newest Application in MOS Devices

- Date:** October 6th (Tue), 2009
- Location:** Lecture room, 2nd building, 5F, Institute of Fluid Science, Tohoku University 2-1-1, Katahira, Aoba-ku, Sendai, Miyagi, 980-8577, Japan
- Registration fee:** General: ¥15,000, Student: ¥3,000
(Attendee of SSDM 2009 Workshop: General: ¥20,000, Student: ¥5,000)
- Capacity:** 100
- Registration:** Participants are required to register online at the conference web site <http://www.ssdm.jp>, in which the forms for short course will be available from the beginning of June, 2009 to September 24th, 2009. After September 24th, please register onsite.

※All lectures are given in English.

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Organizers

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Over sixty years has past after the invention of transistor by Shockley. This invention has brought about highly advanced information society which has never been expected. Miniaturization of the semiconductor device has progressed steadily until now, however, many researchers points out their limit recently. MOS (Metal-Oxide-Semiconductor) transistors have played important role in various devices such as logic or memory and their high performance have been pursued extensively. In recent years, new materials such as high-k film or strain silicon have been introduced, however, their important role will not be replaced. In this short course, MOS transistors are lectured in various view points from basic theory to newest application for beginners such as students or younger researchers.

Program

11 : 00-12 : 00 Advanced LSI Technology - Operation Principles of Scaled MOS Transistors-

Prof. T. Hiramoto, University of Tokyo

The driving force of the performance improvements in recent MOS transistors is not only the further device scaling but also the introduction of new materials and new structures. This lecture covers basic operation principles of a long-channel MOS transistors, various short channel effects including threshold voltage roll-off and DIBL, and new booster technologies for performance improvements. The future prospects of ultimate MOS devices are also mentioned.

(12 : 00-13 : 00 Lunch)

13 : 00-14 : 00 Gate Stack Technology -From thin gate oxide to High-k gate dielectric-

Dr. M. Niwa, Panasonic Corporation

The continuous downscaling of MOSFETs requires a corresponding reduction of the gate dielectric thickness. And due to the reduction in thickness, direct tunneling current through gate dielectrics has become a critical issue. To ease off this vertical scaling, high-k dielectrics have been introduced by reducing the gate leakage current, hence allows increased scaling of the gate dielectric thickness.

In this course, history of the gate stack study from thin gate SiO₂ to high-k gate dielectric including corresponding gate electrode will be traced and the present situation and future prospects for the advanced gate stack will be discussed.

14 : 00-15 : 00 Interconnect Technology

Prof. K. Ueno, Shibaura Institute of Technology

Interconnect technology has become more critical in LSI performance, yield, and reliability with LSI scaling. At the same time, interconnect scaling continue to be a big challenge for improvement. In this short course, overview of interconnect technology will be provided. Basic processes, integration schemes, and reliability issues for Cu/low-k interconnect will be reviewed. We will discuss challenges in sub-100nm Cu interconnect such as resistivity increase and reliability degradation, as well as their potential solutions. We will also discuss emerging interconnect technologies including 3D interconnect, nano-carbon interconnect, and optical interconnect, which will potentially break-through the limit of Cu/low-k interconnect.

(15 : 00-15 : 20 Break)

15 : 20-16 : 20 Analysis Technique of LSI device

Prof. S. Miyazaki, Hiroshima University

For the sophistication of semiconductor process modules, characterization and diagnostics in material processing play a leading role. With progressive device scaling, in-depth analysis of ultrathin films, very shallow regions including interfaces has been increasingly important. Among many surface sensitive measurements including electron spectroscopies, photoemission techniques are quite powerful to get a better understanding of chemical and electronic structures of surfaces, ultrathin films and interfaces. In this talk, comprehensive yet concise commentaries on how useful information photoemission techniques provide us will be given based on some case studies.

16 : 20-17 : 20 Nano Device Design by Theoretical Approach

Prof. K. Shiraishi, University of Tsukuba

Recent Si-nano-technology requires the use of new materials to continue significant downscaling which leads to higher computational speed, larger memory size and lower power consumption. The knowledge of new materials surely enriches our lives, since our modern society relies on the technologies developed in modern histories. In particular, Si nano-technology gives us great knowledge which leads to the new finding in nano-science due to its precise control of sizes and shapes of various materials based on the highly developed fabrication techniques.

In this lecture, we will show the new scientific findings based on computational science which gives great insight to modern semiconductor technologies.