Plenary Session
15:00-15:45 2F Heisei
Chair: S. Chung, *National Chiao Tung Univ.*

15:00 PL-2-1
Long term strategy for mitigating climate change
Y. Kaya, *RITE,* Japan

Area 1: Advanced Gate Stack / Si Processing & Material Science

A-3: Source/Drain Engineering
13:05-14:40 2F Heisei <Higashi>
Chair: H. Fukutome (Fujitsu Microelectronics Ltd.)
I. Yamamoto (NEC Corp.)

13:05 A-3-1
Carbon Incorporation into Substitutional Silicon Site by Molecular Carbon Ion Implantation and Recrystallization Annealing for Stress Technique in nMOSFETs
H. Itokawa, K. Miyano, Y. Oshima, I. Mizushima and K. Suguro, *Toshiba Corp. (Japan)*

13:25 A-3-2
Influence of Carbon in in-situ Carbon Doped SiGe (SiGe:C) Films on Si (001) Substrates on Epitaxial Growth Characteristics
H. Oomae[1], H. Itokawa[2], I. Mizushima[2], S. Nakamura[3] and N. Uchitomi[1], *[1]Nagaoka Univ. of Tech., [2]Toshiba Corp. and [3]Aoyama Gakuin Univ. (Japan)*

13:45 A-3-3
Carbon Profile Engineering for Silicon-Carbon Source/Drain Stressor Formed by Carbon Ion Implantation and Solid Phase Epitaxy
Q. Zhou[1], S. M. Koh[1], Z. Y. Zhao[2], T. Toh[2], H. Maynard[2], N. Variam[2], T. Henry[2], Y. Erokhin[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Varian Semiconductor (Singapore)*

14:05 A-3-4
Contribution of Carbon to Activation and Diffusion of Boron in Silicon
H. Itokawa[1], Y. Agatsuma[2], N. Aoki[1], N. Uchitomi[2] and I. Mizushima[1], *[1]Toshiba Corp. and [2]Nagaoka Univ. of Tech. (Japan)*

15:00-15:45 Plenary Session

Area 1: Advanced Gate Stack / Si Processing & Material Science

B-4: High-k/Metal Gate I
16:00-17:30 2F Heisei <Naka>
Chair: I. Yamamoto (NEC Corp.)
Y. Nara (Fujitsu Microelectronics Ltd.)

16:00 B-4-1 (Invited)
Development of high-k / Metal Gate CMOS Technology in Selete
K. Ikeda, J. Yugami, T. Aoyama and Y. Ohji, *Selete (Japan)*

16:30 B-4-2
Gate Leakage Advantage of LaO Incorporation for V_t Tuning in High-k nMOSFETs over Metal Gate WF Control
M. Kadoshima[1], S. Sakashita[1], T. Kawahara[1], M. Inoue[1], M. Mizutani[1], Y. Nishida[1], A. Shimizu[1], Y. Takeshima[1], S. Yamanari[1], M. Anma[1], R. Mitsuhash[2], Y. Satoh[2], S. Matsuyama[2], A. Tsudumitani[2], Y. Okuno[2], H. Umeda[1], J. Yugami[1], H. Yoshimura[1] and H. Miyatake[1], *[1]Renesas Tech. Corp. and [2]Panasonic Corp. (Japan)*

16:50 B-4-3
Influence of Post Cap-layer Deposition Annealing Temperature on MgO Diffusion in High-k/IFL Stacks
T. Morooka, T. Matsuki, T. Nabatame, J. Yugami, K. Ikeda and Y. Ohji, *Selete (Japan)*

17:10 B-4-4
Bottom-La Inserted HfSiON Gate Dielectrics with

MOCVD HfCN Metal Gate Electrode Realizing High Mobility and Reliability Improvement
S. Inumiya, A. Kaneko, K. Nagatomo, M. Goto, K. Tatsumura, I. Hirano, S. Kawanaka, A. Azuma, K. Nakajima, T. Aoyama, K. Eguchi, A. Nishiyama, Y. Toyoshima and Y. Tsunashima, *Toshiba Corp.(Japan)*

17:30-17:40 Break

Area 1: Advanced Gate Stack / Si Processing & Material Science

B-5: High-k/Metal Gate II
17:40-19:00 2F Heisei <Naka>
Chair: J. Yugami (Selete)
H. Umeda (Renesas Tech. Corp.)

17:40 B-5-1
Channel Strain Analysis in High Performance Damascene-gate pMOSFETs by High Spatial Resolution Raman Spectroscopy
M. Takei[1], D. Kosemura[1], K. Nagata[1], H. Akamatsu[1], S. Mayuzumi[1,2], S. Yamakawa[2], H. Wakabayashi[2] and A. Ogura[1], *[1]Meiji Univ. and [2]Sony Corp. (Japan)*

18:00 B-5-2
Effect of Post Cap-Layer Deposition Annealing Temperature and TiN Thickness on SMDH CMOS Process using TiN Hard Mask
H. Shinohara, A. Katakami, T. Watanabe, M. Hayashi, S. Kamiyama, Y. Sugita, T. Matsuki, T. Eimori, J. Yugami, K. Ikeda and Y. Ohji, *Selete (Japan)*

18:20 B-5-3
Improvement of Interfacial Characteristics and Reliability in Poly/SiON Gate Stack by Catalytic Effect of Hafnium Incorporation Technique
T. Shimizu, Y. Arayashiki, S. Inumiya, K. Nakajima, T. Aoyama and K. Eguchi, *Toshiba Corp. (Japan)*

18:40 B-5-4
Influence of Gate Electrode Stress on Channel Stress and

Device Performance in Gate-First W/TiN Gate MOSFETs
T. Matsuki, J. Yugami, T. Eimori, Y. Nara and K. Ikeda, *Selete (Japan)*

Area 2: Characterization and Materials Engineering for Interconnect Integration

D-4: Scaled-down Cu Metallization
16:00-17:10 3F Sakura
Chair: S. Matsumoto (Panasonic Corp.)
T. Hasegawa (Sony Corp.)

16:00 D-4-1 (Invited)
Patterning & Metallization Options for Advanced Contact Module Integration
S. Demuynck, *IMEC (Belgium)*

16:30 D-4-2
Effect of Via-Profile on the Via Reliability in Scaled-down Low-k/Cu Interconnects
I. Kume, N. Inoue, S. Saito, N. Furutake, J. Kawahara and Y. Hayashi, *NEC Electronics Corp. (Japan)*

16:50 D-4-3
On the Reliability of Cu Contacts for the 32nm Technology Node and beyond
T. Kauerauf, S. Demuynck, G. Butera, J. Bogan, Zs. Tökei and G. Groeseneken, *IMEC (Belgium)*

17:10-17:30 Break

Area 2: Characterization and Materials Engineering for Interconnect Integration

D-5: Characterization and Reliability for Metallization
17:30-18:40 3F Sakura
Chair: G. Beyer (IMEC)
M. Kodera (Toshiba Corp.)

17:30 D-5-1 (Invited)
High-Resolution and Thermodynamic Analysis of Interconnect Metals and Diffusion Barriers
R. Sinclair, *Stanford Univ. (USA)*

18:00 D-5-2
Rutherford Backscattering Spectrometry Analysis of Growth of Ti-Rich Layer Formed at Cu(Ti)/Low-k Interfaces
K. Kohama[1], K. Ito[1], K. Mori[2], K. Maekawa[2], Y. Shirai[1] and M. Murakami[3], *[1]Kyoto Univ., [2]Renesas Tech. Corp. and [3]The Ritsumeikan Trust (Japan)*

18:20 D-5-3
A Comparison of Lifetime Improvements in Electromigration between Ti Barrier Metal and CVD Co Capping
Y. Kakuhara and S. Yokogawa, *NEC Electronics Corp. (Japan)*

Area 3: CMOS Devices /Device Physics

A-4: Novel Device Structure and Physics
16:30-17:10 2F Heisei <Higashi>
Chair: D. Hisamoto (Hitachi, Ltd.)
Y. Yeo (National Univ. of Singapore)

16:30 A-4-1
Multiple-Gate Tunneling Field Effect Transistors with sub-60mV/dec Subthreshold Slope
D. Leonelli[1,2], A. Vandooren[1], R. Rooyackers[1], A. S. Verhulst[1,2], S. De Gendt[1,2], M. M. Heyns[1,2] and G. Groeseneken[1,2], *[1]IMEC and [2]Katholieke Univ. Leuven (Belgium)*

16:50 A-4-2
Novel Source Heterojunction Structures with Relaxed-/Strained-Layers for Quasi-Ballistic CMOS Transistors using Ion Implantation Induced Relaxation Technique of Strained-Substrates
T. Mizuno[1,2], N. Mizoguchi[1], K. Tanimoto[1], T. Yamauchi[1], T. Tezuka[3] and T. Sameshima[4], *[1]Kanagawa Univ., [2]MIRAI-NIRC, [3]MIRAI-Toshiba and [4]Tokyo Univ. of Agri. and Tech. (Japan)*

17:10-17:30 Break

Area 3: CMOS Devices /Device Physics

A-5: New Device Technologies
17:30-18:50 2F Heisei <Higashi>
Chair: K. Horita (Renesas Tech. Corp.)
S. Hayashi (Panasonic Corp.)

17:30 A-5-1
NiSi metal S/D transistors with ultimaltely low Schottky barrier by sulfur Implantation After Silicidation Process
Y. Nishi and A. Kinoshita, *Toshiba Corp. (Japan)*

17:50 A-5-2
A New Diamond-like Carbon (DLC) Ultra-High Stress Liner Technology for Direct Deposition on P-Channel Field-Effect Transistors
B. Liu[1], M. C. Yang[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Data Storage Inst. (Singapore)*

18:10 A-5-3
Investigation on Enhanced Impact Ionizaion in Uniaxially Strained Si MOSFET
S. Adachi and T. Asano, *Kyushu Univ. (Japan)*

18:30 A-5-4
Influence of Carrier Transit Delay on CMOS Switching Performance
D. Hori[1], M. Miyake[1], N. Sadachika[1], H. J. Mattausch[1], M. Miura-Mattausch[1], T. Iizuka[2], T. Hoshida[2], K. Matsuzawa[2], Y. Sahara[2] and T. Tsukada[2], *[1]Hiroshima Univ. and [2]STARC (Japan)*

Area 4: Advanced Memory Technology

G-3: Flash Memory II
13:15-14:35 4F Hirose <Nishi>
Chair: R. Shen (eMemory Tech. Inc.)
Y. Shimamoto (Hitachi, Ltd.)

13:15 G-3-1
Direct Measurement of Back-Tunneling Current during

Program/Erase Operation of MONOS Memories and Its Dependence on Gate Work Function
J. Fujiki, S. Fujii, N. Yasuda and K. Muraoka, *Toshiba Corp. (Japan)*

13:35 G-3-2
Thickness Effect on Read Window in a Two-Bit Nitrided-based Trapping Storage Cell
G. D. Lee, C. H. Cheng, S. H. Ku, C. H. Liu, S. H. Kuo, C. H. Lee, S. W. Huang, N. K. Zous, M. S. Chen, W. P. Lu, K. C. Chen and C. Y. Lu, *Macronix Int'l Co., Ltd. (Taiwan)*

13:55 G-3-3
Engineering of Si-rich Nitride Charge-Trapping Layer for Highly Reliable MONOS Type NAND Flash Memory with MLC Operation
R. Fujitsuka, K. Sekine, A. Sekihara, A. Fukumoto, J. Fujita, F. Aiso and Y. Ozawa, *Toshiba Corp. (Japan)*

14:15 G-3-4
Thermally Robust Nanocrystal Memory with Co Bio-nanodot Self-assembled Monolayer as a Charge Trap Medium on Ultrathin $LaAlO_3$ Layer
S. Jung[1], K. Ohara[2], Y. Uraoka[2], T. Fuyuki[2], I. Yamashita[2] and H. Hwang[1], *[1]Gwangju Inst. of Sci. and Tech. and [2]NAIST (Korea)*

15:00-15:45 Plenary Session

Area 4: Advanced Memory Technology

G-4: Flash Memory III
16:00-17:20 4F Hirose <Nishi>
Chair: Y. C. Chen (Macronix Int'l Co., Ltd.)
R. Shen (eMemory Tech. Inc.)

16:00 G-4-1
Depletion-type Cell-Transistor of 23 nm Cell Size on Partial SOI Substrate for NAND Flash Memory
M. Mizukami[1], K. Nishihara[2], H. Ishida[2], F. Aiso[2], T. Iguchi[2], D. Ichinose[2], A. Fukumoto[2], N. Aoki[2],

M. Kondo[2], T. Izumida[2], H. Tanimoto[2], T. Enda[2], T. Suzuki[2], I. Mizushima[2] and F. Arai[2], *[1]Toshiba R&D Center and [2]Toshiba Advanced Micro-electronics Center (Japan)*

16:20 G-4-2
The Operation Scheme and Process Optimization in TLC(Triple Level Cell) NAND Flash Characteristics
J. Yang, M. Park, S. Jung, S. Park, S. Cho, J. An, J. Lee, S. Cho, H. Lee, M. K. Cho, K. O. Ahn, K. Jin and Y. Koh, *Hynix Semiconductor Inc. (Korea)*

16:40 G-4-3
The Influence of Mechanical Stress on Data Retention in Advanced NAND Flash
S. W. Seo, H. Oh, Y. Yang, S. M. Yi, S. Y. Kim, P. Kim, D. K. Lee, H. Yang, H. Lee, M. K. Cho, K. O. Ahn and Y. Koh, *Hynix Semiconductor Inc. (Korea)*

17:00 G-4-4
A New Differential Logic-Compatible Multiple-Time Programmable (MTP) Memory Cell
Y. H. Tsai, H. L. Yang, W. J. Lin, C. J. Lin and Y. C. King, *National Tsing Hua Univ. (Taiwan)*

17:20-17:30 Break

Area 4: Advanced Memory Technology

G-5: PRAM
17:30-18:20 4F Hirose <Nishi>
Chair: M. Moniwa (Renesas Tech. Corp.)
Y. C. Chen (Macronix Int'l Co., Ltd.)

17:30 G-5-1 (Invited)
Current Status and Future Challenge of PRAM
Y. H. Shih, *Macronix Int'l Co., Ltd. (Taiwan)*

18:00 G-5-2
Elevated-Confined Phase Change RAM cells
H. K. Lee[1], L. P. Shi[1], R. Zhao[1], H. X. Yang[1], K. G. Lim[1], J. M. Li[1] and T. C. Chong[1,2], *[1]A*STAR and [2]National Univ. of Singapore (Singapore)*

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

J-3: SiC and Diamond Devices
13:15-14:45 6F Hagi
Chair: R. Hattori (Mitsubishi Electric Corp.)
T. Tanaka (Panasonic Corp.)

13:15 J-3-1 (Invited)
SiC Power MOSFETs and Diodes for Next Generation
J. W. Palmour, A. Agarwal, R. Callanan and J. Richmond, *Cree, Inc. (USA)*

13:45 J-3-2
Improvement of Interface Properties by NH_3 Pretreatment for 4H-SiC(000-1) MOS Structure
Y. Iwasaki, H. Yano, T. Hatayama, Y. Uraoka and T. Fuyuki, *NAIST (Japan)*

14:00 J-3-3
Very Smooth SiO_2/SiC Interface Formed by Supercritical Water Oxidation of Low Temperature
T. Futatsuki[1,2], T. Oe[2], H. Aoki[1], N. Komatsu[1], C. Kimura[1] and T. Sugino[1], *[1]Osaka Univ. and [2]Organo Corp. (Japan)*

14:15 J-3-4
Interface Properties of C-face 4H-SiC Metal-Oxide-Semiconductor Structures Prepared by Direct Oxidation in Nitric Oxide
D. Okamoto, H. Yano, Y. Oshiro, T. Hatayama, Y. Uraoka and T. Fuyuki, *NAIST (Japan)*

14:30 J-3-5
High-temperature Operation of Boron-implanted Diamond FETs
K. Ueda, Y. Yamauchi and M. Kasu, *NTT Basic Res. Labs. (Japan)*

15:00-15:45 Plenary Session

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

J-4: High-frequency Devices
16:00-17:15 6F Hagi
Chair: S. Yamahata (NTT Corp.)
K. S. Seo (Seoul National Univ.)

16:00 J-4-1
A 20-Gb/s Pulse Generator with 4.9-ps FWHM using 75-nm InP-based HEMTs
Y. Nakasha[1], Y. Kawano[1], T. Suzuki[1], T. Ohki[2], T. Takahashi[1], K. Makiyama[1] and N. Hara[1], *[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd. (Japan)*

16:15 J-4-2
Ultra-Fast Optical Response by InAlAs/InAs/InGaAs Pseudomorphic High Electron Mobility Transistors
H. Taguchi, Y. Oishi, T. Ando, K. Uchimura, M. Mochiduki, M. Enomoto, T. Iida and Y. Takanashi, *Tokyo Univ. of Sci. (Japan)*

16:30 J-4-3
0.25-μm-Emitter InP HBTs with a Passivation Ledge Structure
N. Kashio, K. Kurishima, Y. K. Fukai, M. Ida and S. Yamahata, *NTT Corp. (Japan)*

16:45 J-4-4
$In_{0.49}GaP/Al_{0.45}GaAs/In_{0.22}GaAs/Al_{0.22}GaAs$ Barrier Enhancement-mode Pseudo-morphic High Electron Mobility Transistor with an Enhanced Gate Forward Turn-on Voltage
J. Sung, J. Kim, K. Jang and K. S. Seo, *Seoul National Univ. (Korea)*

17:00 J-4-5
RF Small Signal Characterization of Active Transmission Lines Load by InGaAs/AlAs Resonant Tunneling Diodes
K. Kasahara, T. Ohe, M. Mori and K. Maezawa, *Univ. of Toyama (Japan)*

17:15-17:30 Break

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

J-5: Graphen and Oxide Devices
17:30-18:45 6F Hagi
Chair: K. Maezawa (Univ. of Toyama)
Y. Ohno (Univ. of Tokushima)

17:30 J-5-1
Extraction of Drain Current and Effective Mobility in Epitaxial Graphene Channel FETs on Silicon Substrates
H. C. Kang[1], R. Olac-vaw[1], H. Karasawa[1], Y. Miyamoto[1], H. Handa[1], T. Suemitsu[1,2], H. Fukidome[1,2], M. Suemitsu[1,2] and T. Otsuji[1,2], *[1]Tohoku Univ. and [2]CREST-JST (Japan)*

17:45 J-5-2
Enhancement-mode MOCVD Grown ZnO TFTs on Glass Substrates using N_2O Plasma Treatment
K. Remashan, Y. S. Choi, S. J. Park and J. H. Jang, *Gwangju Inst. of Sci. and Tech. (Korea)*

18:00 J-5-3
Effect of Post Thermal Annealing of ZnO-TFTs by Atomic Layer Deposition
Y. Kawamura[1] and Y. Uraoka[1,2], *[1]NAIST and [2]CREST-JST (Japan)*

18:15 J-5-4
Low Voltage Operation of Inverted Staggered Amorphous Indium Gallium Zinc Oxide Thin Film Transistor with Al_2O_3 High-k Dielectric Material
Y. G. Yoon and J. H. Jang, *Gwangju Inst. of Sci. and Tech. (Korea)*

18:30 J-5-5
Characteristics of Transparent ZnO Based Thin Film Transistors with High-k Dielectric Gd_2O_3 Gate Insulators Fabricated at Room Temperature
J. R. Tsai, C. S. Li, J. N. Chen, C. J. Tseng, P. H. Chien, W. S. Feng and K. C. Liu, *Chang Gung Univ. (Taiwan)*

Area 7: Photonic Devices and Device Physics

I-3: LED I
13:15-14:45 6F Kaede
Chair: M. Gotoda (Mitsubishi Electric Corp.)
H. Yamada (Tohoku Univ.)

13:30 I-3-2
Divergent Far-Field Pattern from GaN-based Film-Transferred Photonic Crystal Light-Emitting Diodes
C. F. Lai[1], H. C. Kuo[1], C. H. Chao[2], H. H. Yeh[1], C. E. Lee[1], C. Y. Huang[2] and W. Y. Yeh[2], *[1]National Chiao Tung Univ. and [2]Indus. Tech. Res. Inst. (Taiwan)*

13:45 I-3-3
High Performance Angled Light-Emitting Diodes by Laser Micromachining
K. N. Hui[1,2], P. T. Lai[2] and H. W. Choi[2], *[1]State Univ of New Jersey and [2]Univ. of Hong Kong (USA)*

14:00 I-3-4
A Screen Printed Sn-based Dicing-Free Metal Substrate Technology for the Fabrication of Vertical-Structured GaN-based Light-Emitting Diodes
P. R. Wang[1], P. H. Wang[1], H. Y. Kuo[1], K. M. Uang[2], T. M. Chen[2], D. M. Kuo[1] and S. J. Wang[1], *[1]National Cheng Kung Univ. and [2]Wufeng Inst. Of Tech. (Taiwan)*

14:15 I-3-5
Fabrication of High Qualify factor of GaN-based Vertical-cavity Light Emitting Diodes with AlN/GaN and Ta_2O_5/SiO_2 Hybrid Mirrors
S. W. Chen, C. K. Chen, T. T. Kao, C. H. Chen, M. H. Lo, Z. Y. Li, T. C. Lu, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ. (Taiwan)*

14:30 I-3-6
Enhanced Light Output of Vertical-Structured GaN-based LEDs with Surface Roughening using KrF Laser and ZnO Nanorods
W. C. Lee[1], K. M. Uang[2], T. M. Chen[2], D. M. Kuo[1],

P. R. Wang[1], C. R. Tseng[1], C. K. Wu[1] and S. J. Wang[1], *[1]National Cheng Kung Univ. and [2]Wufeng Inst. Of Tech. (Taiwan)*

15:00-15:45 Plenary Session

Area 8: Advanced Material Synthesis and Crystal Growth Technology

H-3: Oxide Materials
13:15-14:45 6F Kiri
Chair: M. Nakada (NEC Corp.)
T. Fukumura (Tohoku Univ.)

13:15 H-3-1 (Invited)
High throughput combinatorial materials Exploration for advanced magneto-electronics
T. Fukumura[1,2], *[1]Tohoku Univ. and [2]PRESTO-JST (Japan)*

13:45 H-3-2
Control of Crystal-growth of VO_2 Films Fabricated by Excimer Laser Assisted Metal Organic Deposition
M. Nishikawa[1], T. Nakajima[2], T. Kumagai[2], T. Okutani[1] and T. Tsuchiya[2], *[1]Yokohama National Univ. and [2]AIST (Japan)*

14:00 H-3-3
Prediction of Crystallization Temperature for HfO_2 Thin Film in High Temperature Annealing Process by Reaction Time Accelerating Molecular Dynamics
K. Nishitani[1,2], H. Yabuhara[1], A. Endou[2], A. Suzuki[2], H. Tsuboi[2], N. Hatakeyama[2], H. Takaba[2], M. Kubo[2] and A. Miyamoto[2], *[1]Toshiba Corp. and [2]Tohoku Univ. (Japan)*

14:15 H-3-4
Electrical and Physical Characteristics of the High-K Gd_2O_3 (Gadolinium) Dielectric Deposited on the Polycrystalline Silicon
J. S. Chiu[1], C. H. Kao[1], H. Chen[2], P. Y. Tsung[1], Y. C. Liao[1], W. S. Liao[1], Y. T. Chung[1], H. C. Fan[1], P. L. Lai[1], C. Y. Huang[1], C. S. Lin[1] and J. M. Dai[1], *[1]Chang Gung Univ. and [2]Chi Nan Univ. (Taiwan)*

14:30 H-3-5
Highly-(001)-Oriented Ferroelectric PZT Thin Films on Glass by CW Green-Laser Crystallization
J. Jiang, S. Kuroki, K. Kotani and T. Ito, *Tohoku Univ. (Japan)*

15:00-15:45 Plenary Session

Area 8: Advanced Material Synthesis and Crystal Growth Technology

H-4: Advanced Nitride Growth and Structures
16:00-17:15 6F Kiri
Chair: Y. Sakuma (NIMS)
T. Iwai (Fujitsu Labs. Ltd.)

16:00 H-4-1 (Invited)
Recent advances in InN-based III-nitrides towards novel nanostructure photonic devices
A. Yoshikawa, Y. Ishitani, S. B. Che, N. Hashimoto, A. Yuki, H. Watanabe and K. Kusakabe, *Chiba Univ. (Japan)*

16:30 H-4-2
Epitaxial overgrowth of GaN Nanorods on Si (111) substrates by rf-plasma-assisted molecular-beam Epitaxy
J. T. Ku, T. H. Yang, J. R. Chang, Y. Y. Wong, W. C. Chou and C. Y. Chang, *National Chiao Tung Univ. (Taiwan)*

16:45 H-4-3
Growth of (10_{-1} 3) semipolar GaN on Si substrate with a CrN interlayer by molecular beam epitaxy
K. W. Liu, T. H. Hsueh, S. J. Young, H. Hung, S. X. Chen, Y. Z. Chen and S. J. Chang, *Nation Cheng Kung Univ. (Taiwan)*

17:00 H-4-4
Growth of Quaternary AlInGaN with Various TMI Molar Rates
S. F. Yu, S. J. Chang and S. P. Chang, *National Cheng Kung Univ. (Taiwan)*

17:15-17:30 Break

Area 8: Advanced Material Synthesis and Crystal Growth Technology

H-5: Advanced Nitride Growth and Structures
17:30-18:45 6F Kiri
Chair: T. Iwai (Fujitsu Labs. Ltd.)
Y. Sakuma (NIMS)

17:45 H-5-2
Growth and Characterization of High Quality a-plane InGaN/GaN Single Quantum Well Structure Grown by Multi-buffer Layer Technique
H. Song[1,2], J. S. Kim[1], E. K. Kim[1], Y. G. Seo[2] and S. M. Hwang[2], *[1]Hanyang Univ. and [2]Korea Electronics Tech. Inst. (Korea)*

18:00 H-5-3
Enhanced Extraction and Efficiency of Blue Light Emitting Diodes Prepared using Two-Step-Etched Patterned Sapphire Substrates
Y. C. Lu[1], S. F. Yu[2], Y. C. S. Wu[3], C. H. Chiang[1], W. C. Hsu[4], S. J. Chang[2] and R. M. Lin[1], *[1]Chang Gung Univ., [2]National Cheng Kung Univ., [3]National Chiao Tung Univ. and [4]Sino-American Silicon Products Inc. (Taiwan)*

18:15 H-5-4
Improvement of the blue LED using patterned sapphire substrates with low threading dislocation densities
S. M. Jeong[1], S. Kissinger[1], Y. H. Ra[1], S. H. Yun[1], D. W. Kim[1], S. J. Lee[2], J. S. Kim[1] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Korea Photonics Tech. Inst. (Korea)*

18:30 H-5-5
Hexagonal AlN (0001) heteroepitaxial growth on cubic diamond (001)
K. Hirama, Y. Taniyasu and M. Kasu, *NTT Corp.(Japan)*

Area 9: Physics and Applications of Novel Functional Materials and Devices

K-3: Electron Spin and Quantum Information
13:15-14:45 6F Aoi
Chair: H. Gotoh (NTT Basic Res. Labs.)
Sven Rogge (Delft Univ. of Tech.)

13:15 K-3-1 (Invited)
Spin Read-Out of Donors in Silicon
M. Brandt, *Munich Univ. of Tech. (Germany)*

13:45 K-3-2
Single-electron Spin Resonance in a g-factor-controlled Semiconductor Quantum Dot
T. Kutsuwa[1], M. Kuwahara[1], K. Ono[2] and H. Kosaka[1,3], *[1]CREST-JST, [2]RIKEN and [3]Tohoku Univ. (Japan)*

14:00 K-3-3
Electron - Nuclear Spin Interaction in Vertical Double Quantum Dot with Different g-factor Layers System
R. Takahashi[1,2], K. Kono[1,2], S. Tarucha[3,4] and K. Ono[1,5], *[1]RIKEN, [2]Tokyo Tech, [3]Univ. of Tokyo, [4]ICORP-JST and [5]CREST-JST (Japan)*

14:15 K-3-4
Robustness of Charge-qubit Cluster States to Double Quantum Point Contact Measurement
T. Tanamoto, *Toshiba Corp. (Japan)*

14:30 K-3-5
Measurement of Electron Spin States in a Semiconductor Quantum well using Tomographic Kerr Rotation
T. Inagaki[1], H. Kosaka[1,2], Y. Rikitake[2,3], H. Imamura[2,4], Y. Mitsumori[1,2] and K. Edamatsu[1], *[1]Tohoku Univ., [2]CREST-JST, [3]Sendai National College of Tech. and [4]AIST (Japan)*

15:00-15:45 Plenary Session

Area 9: Physics and Applications of Novel Functional Materials and Devices

K-4: Nanomechanical Systems
16:00-17:15 6F Aoi
Chair: D. G. Austing (National Res. Council of Canada)
K. Ono (RIKEN)

16:00 K-4-1 (Invited)
Electromechanical Systems for Memory and Logic Devices
I. Mahboob and H. Yamaguchi, *NTT Corp. (Japan)*

16:30 K-4-2
Noise-enhanced Sensing using Micromechanical Nonlinear Resonator
Y. Yoshida and T. Ono, *Tohoku Univ. (Japan)*

16:45 K-4-3
Carrier-induced Dynamic Backaction in GaAs Micromechanical Resonators
H. Okamoto[1], D. Ito[1,2], K. Onomitsu[1], H. Sanada[1], H. Gotoh[1], T. Sogawa[1] and H. Yamaguchi[1,2], *[1]NTT Basic Res. Labs. and [2]Tohoku Univ. (Japan)*

17:00 K-4-4
A Novel Thin-film Transistor with Suspended Nanowire Channels and Side-gated Configuration
C. H. Kuo[1], H. C. Lin[1,2], G. J. Li[1], H. H. Hsu[1], C. J. Su[1] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

17:15-17:30 Break

Area 9: Physics and Applications of Novel Functional Materials and Devices

K-5: Novel Devices and Matarials
17:30-18:30 6F Aoi
Chair: B. G. Park (Seoul National Univ.)
M. Watanabe (Tokyo Tech)

17:30 K-5-1
High hole current density in diamond MOSFETs fabricated on H-terminated IIa-type (111) diamond substrate
K. Tsuge[1], Y. Jingu[1], H. Umezawa[2] and H. Kawarada[1], *[1]Waseda Univ. and [2]AIST (Japan)*

17:45 K-5-2
Performance Comparisons of Ballistic Silicon-Nanowire and Graphene Nanoribbon MOSFETs Considering First-Principles Bandstructure Effects
H. Ando, S. Sawamoto, T. Maegawa, T. Hara, H. Yao, H. Tsuchiya and M. Ogawa, *Kobe Univ. (Japan)*

18:00 K-5-3
Formation of Highly B-doped Source & Drain Layers with TiC Ohmic Contacts for H-terminated Diamond MOSFETs
T. Tsuno[1], Y. Jingu[1], H. Umezawa[2] and H. Kawarada[1], *[1]Waseda Univ. and [2]AIST (Japan)*

18:15 K-5-4
Cross-sectional Low-temperature Scanning Tunneling Spectroscopy of a p-n Junction and an Inversion Layer in InAs
K. Suzuki, K. Kanisawa, K. Onomitsu and K. Muraki, *NTT Basic Res.Labs. (Japan)*

Area 10: Organic Materials Science, Device Physics, and Applications

F-4: Organic Transistor
16:00-17:15 4F Hirose <Higashi>
Chair: S. Aramaki (Mitsubishi Chemical Group Science & Technology Research Center, Inc.)
C. K. Song (Dong-A Univ.)

16:00 F-4-1 (Invited)
Surface-selective deposition for organic transistor
K. Tsukagoshi[1,2,3,4] and T. Minari[1,3,4], *[1]MANA-NIMS, [2]AIST, [3]RIKEN and [4]CREST-JST (Japan)*

16:30 F-4-2
High-Speed Operation of Step-Edge Vertical-Channel Organic Transistors
K. Kudo, T. Takano, H. Yamauchi, M. Iizuka and M. Nakamura, *Chiba Univ. (Japan)*

16:45 F-4-3
Demonstration of a Record High Current-gain Cutoff Frequency (>10 MHz) in Organic Thin-film Transistors
M. Kitamura and Y. Arakawa, *Univ. of Tokyo (Japan)*

17:00 F-4-4
Tuning of Threshold Voltage in Organic Field-effect Transistor by Dipole Monolayer
W. O. Yang, X. Chen, M. Weis, T. Manaka and M. Iwamoto, *Tokyo Tech (Japan)*

17:15-17:30 Break

Area 10: Organic Materials Science, Device Physics, and Applications

F-5: Organic Transistor
17:30-18:30 4F Hirose <Higashi>
Chair: T. Kamata (AIST)
S. F. Horng (National Tsing Hua Univ.)

17:30 F-5-1
Organic Field Effect Transistors from Oriented Pentacene Crystal Fibers
N. Wachi, H. Kubo, J. Nishide, H. Sasabe and O. Karthaus, *Chitose Inst. of Sci. and Tech. (Japan)*

17:45 F-5-2
Temperature Dependence of Electrical Properties of Ambipolar Organic Transistors based on F_{16}CuPc/α6T pn Heterojunction
R. Ye[1], M. Baba[1], K. Ohta[1], T. Suzuki[2] and K. Mori[1], *[1]Iwate Univ. and [2]Iwate Indus. Res. Inst. (Japan)*

18:00 F-5-3
Organic Inverters with Double-gate Organic Thin-film

Transistor using Photosensitive Polymer as the Dielectric Layer
C. C. Wang, W. H. Lee, C. T. Liu and S. H. Hsu, *National Cheng Kung Univ. (Taiwan)*

18:15 F-5-4
Displacement Current and Transfer Curve Simultaneous Measurement in Bottom-Contact Organic Thin-film Transistors
S. Suzuki, T. Suzuki, A. Bhaswara and Y. Majima, *Tokyo Tech (Japan)*

Area 13: Applications of Nanotubes and Nanowires

I-4: Compound Semiconductor Nanowires
16:00-17:15 6F Kaede
Chair: K. Tateno (NTT Basic Res. Labs.)
K. Ishibashi (RIKEN)

16:00 I-4-1 (Invited)
Giant, Level-dependent electron g-factors and Kondo physics in few-electron InSb nanowire quantum dots
H. Xu, *Lund Univ. (Sweden)*

16:30 I-4-2
Fabrication of InAs Nanowire Vertical Surrounding-Gate Field Effect Transistor on Si Substrates
T. Tanaka, K. Tomioka, J. Motohisa, S. Hara and T. Fukui, *Hokkaido Univ. (Japan)*

16:45 I-4-3
Design and Fabrication of BDD-based Reconfigurable Logic Circuit on GaAs Nanowire Network
Y. Shiratori[1], K. Miura[1] and S. Kasai[1,2], *[1]Hokkaido Univ. and [2]PRESTO-JST (Japan)*

17:00 I-4-4
Preparation of NiO/ZnO Nanoheterojunction Arrays and Their Optoelectric Characteristics under UV Light Illumination
W. C. Tsai[1], S. J. Wang[1], J. C. Lin[2], C. R. Tseng[1],

F. S. Tsai[1] and W. I. Hsu[1], *[1]National Cheng Kung Univ. and [2]St. John's Univ. (Taiwan)*

Rump Session

19:00-21:30

Session A (4F Hirose-Higashi)

"Novel Lithography for more Moore/beyond CMOS and More than Moore"

Session B (4F Hirose-Nishi)

"Solar Cells for Electronics : from In-Vehicleto Ubiquitous"