NANOELECTRONIC TECHNOLOGY: CHALLENGES IN THE 21st CENTURY

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OUTLINE

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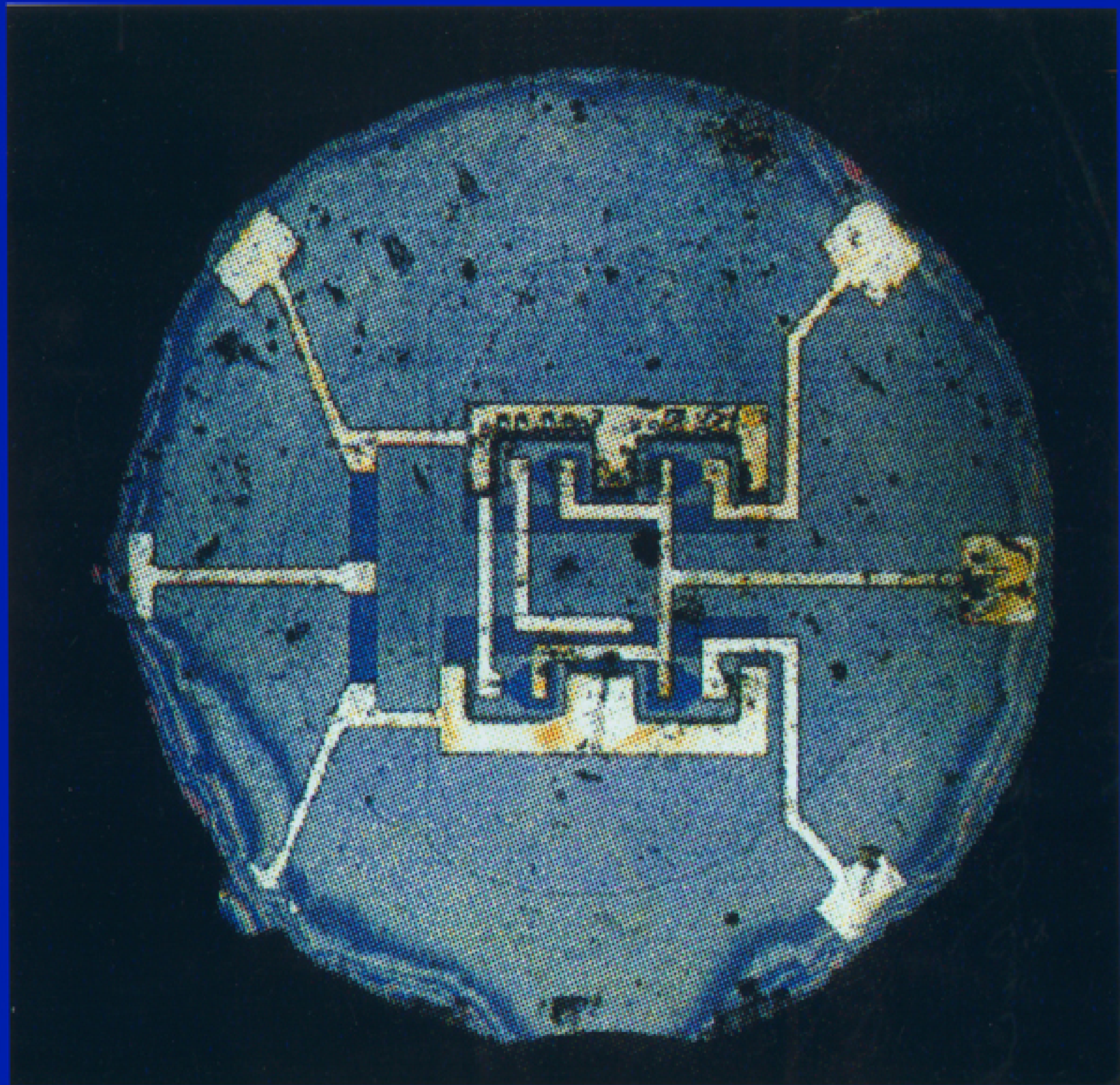
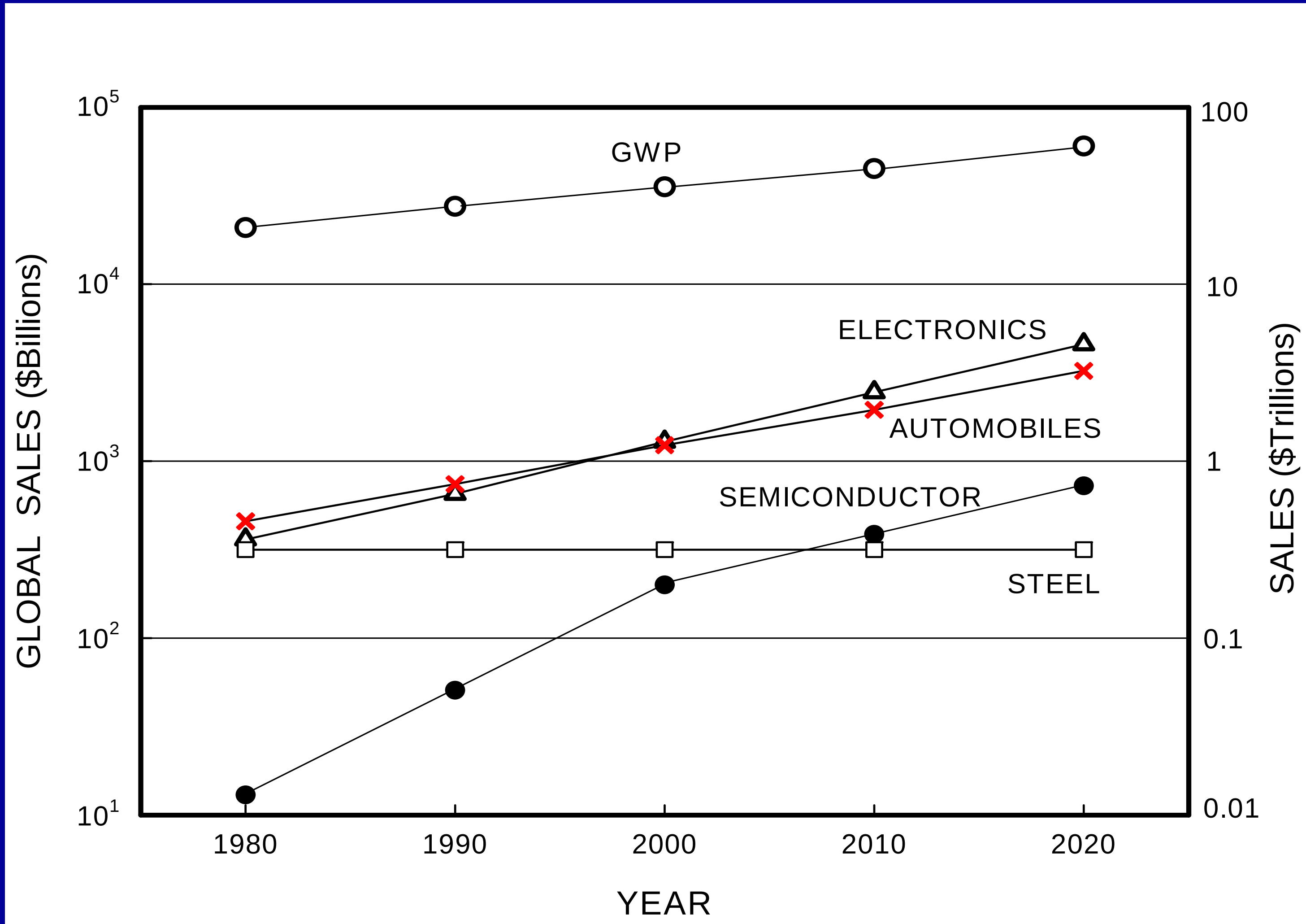
- KEY ACHIEVEMENTS
- MAJOR CHALLENGES
  - WAFER
  - LITHOGRAPHY
  - DEVICE
  - INTERCONNECT
  - ECONOMY
- CONCLUSION

FIRST MONOLITHIC IC BY R. N. NOYCE

(US Patent 2,981,877 filed July 1959, granted 1961)



ELECTRONIC AND SEMICONDUCTOR INDUSTRIES (1980-2020)



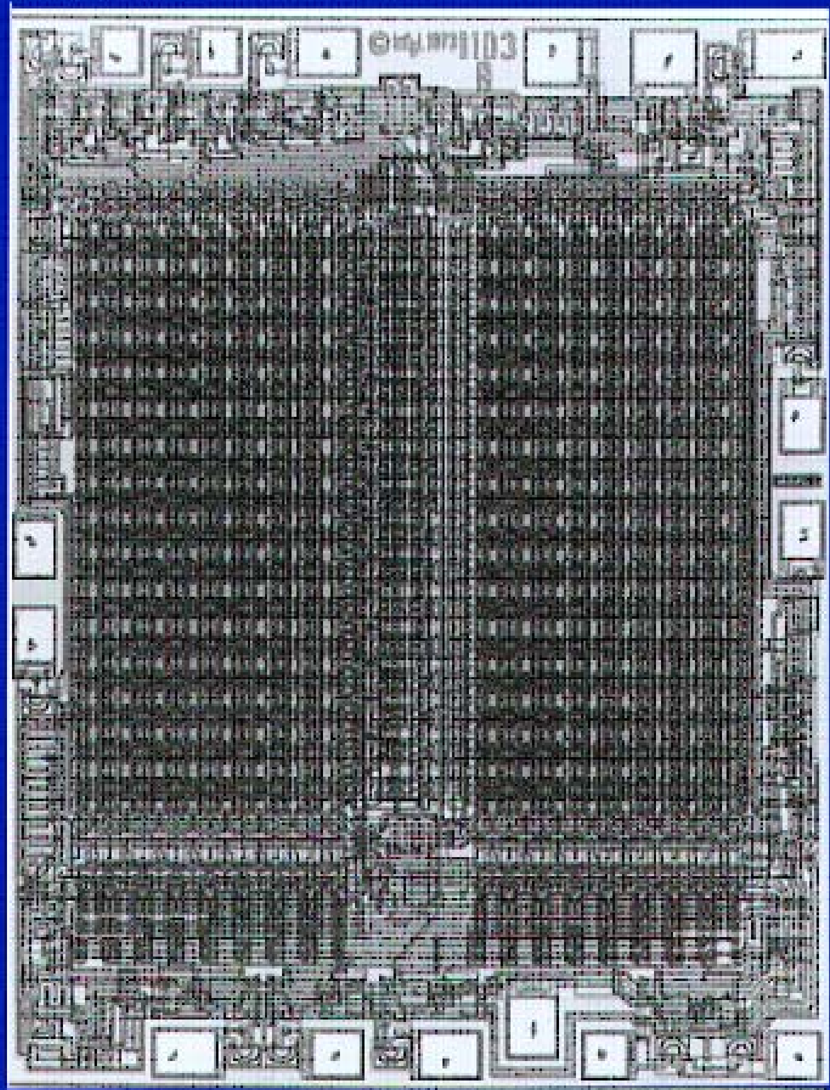
NATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTOR

	Project algorithm for every 3 years	Year 2010
Chip area	1.5X	14 cm^2 DRAM
Min. feature length	30% reduction	50 nm
Components / chip	4X	64 Gb DRAM
On-chip circuit clock	1.5X	50 GHz μP
Cost / transistor	> 50% reduction	10^{-7}
Fab cost	2X	$24 Billions

(Trend projection based on Moore's Law)

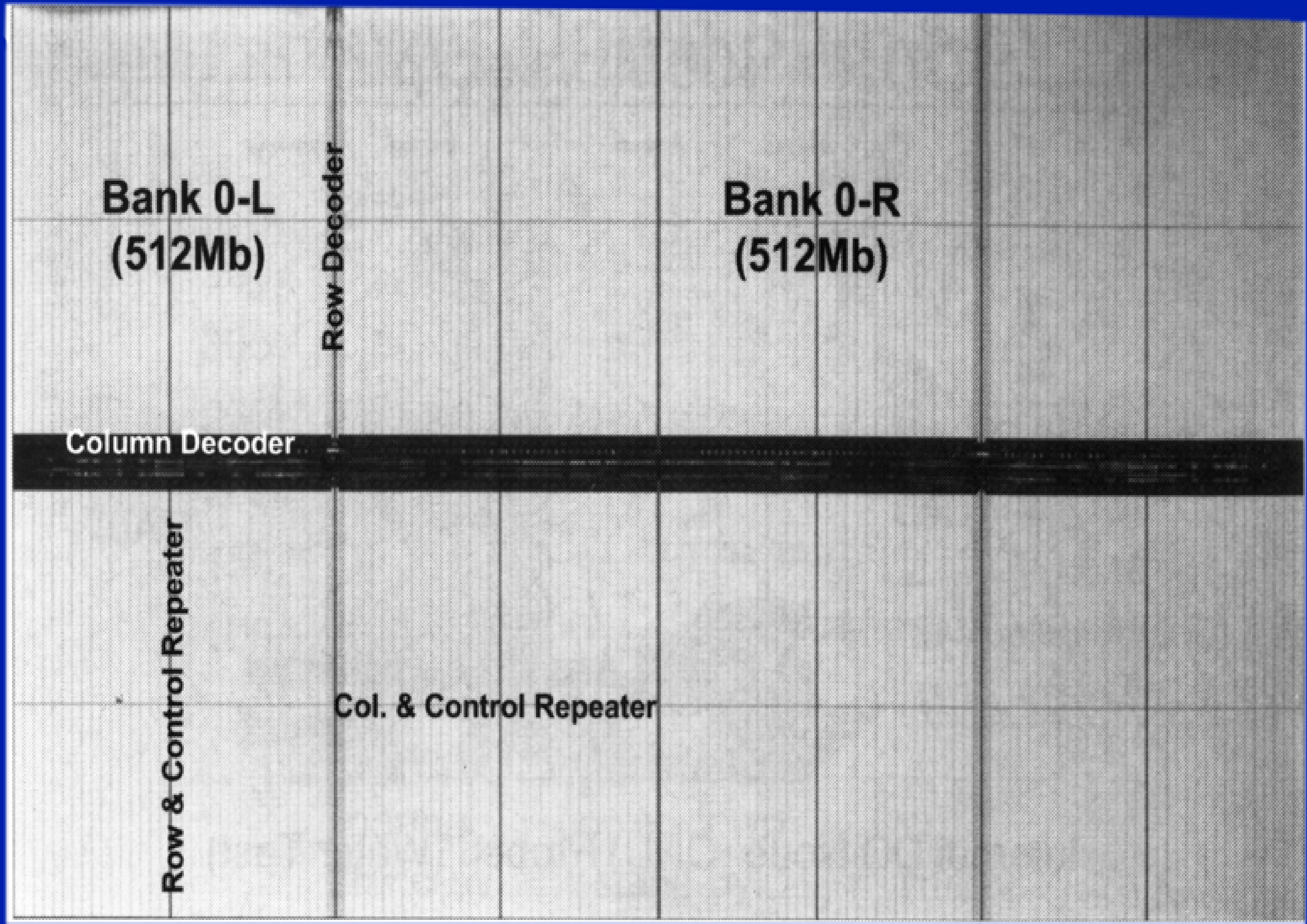
FIRST DRAM (1103 by Intel 1970)

(5 V   8 μm   3 mm^2 2600 μm^2/cell)



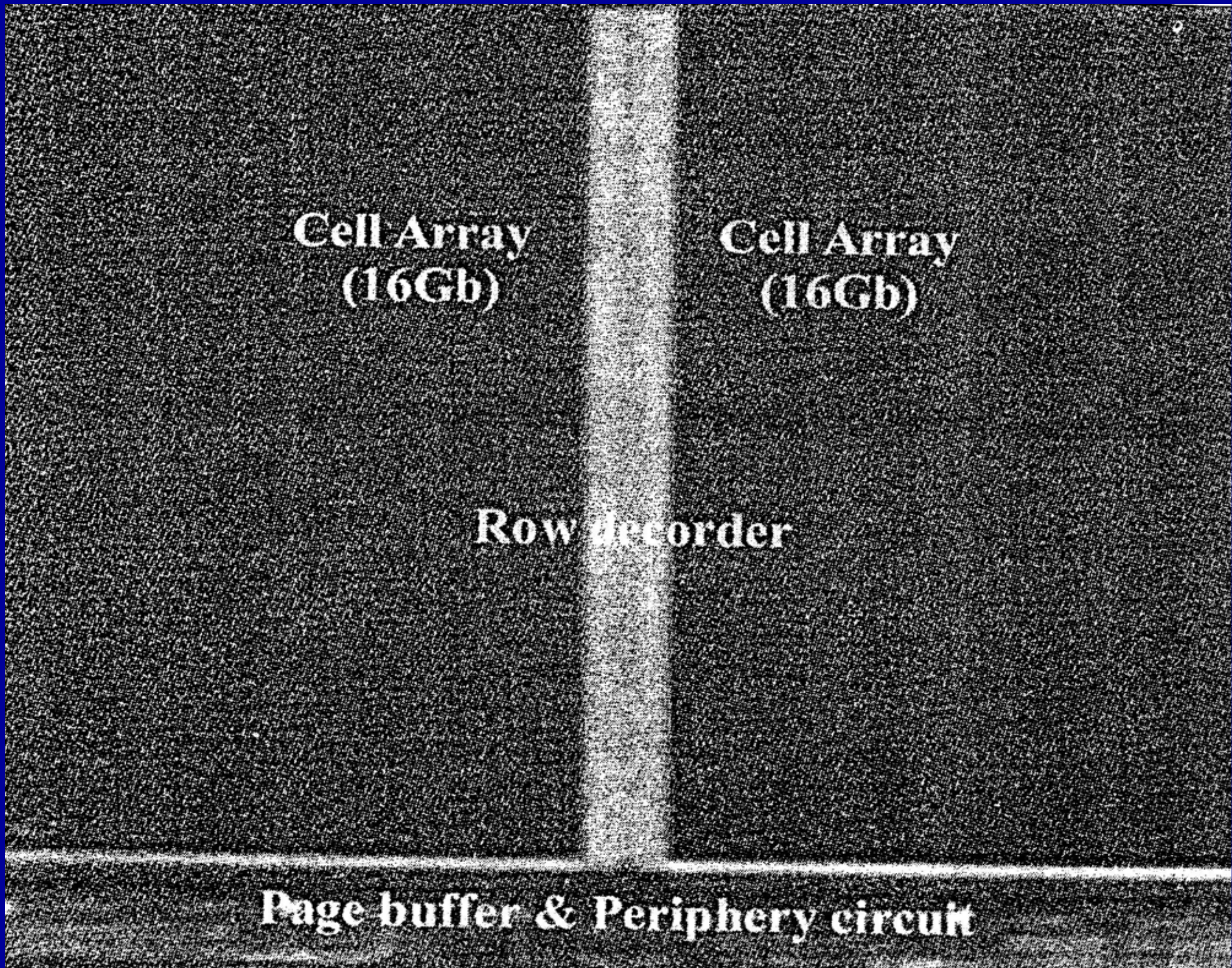
4 Gb DRAM

(1.8 V 0.10 μm 645 mm^2 0.1 μm^2/cell)

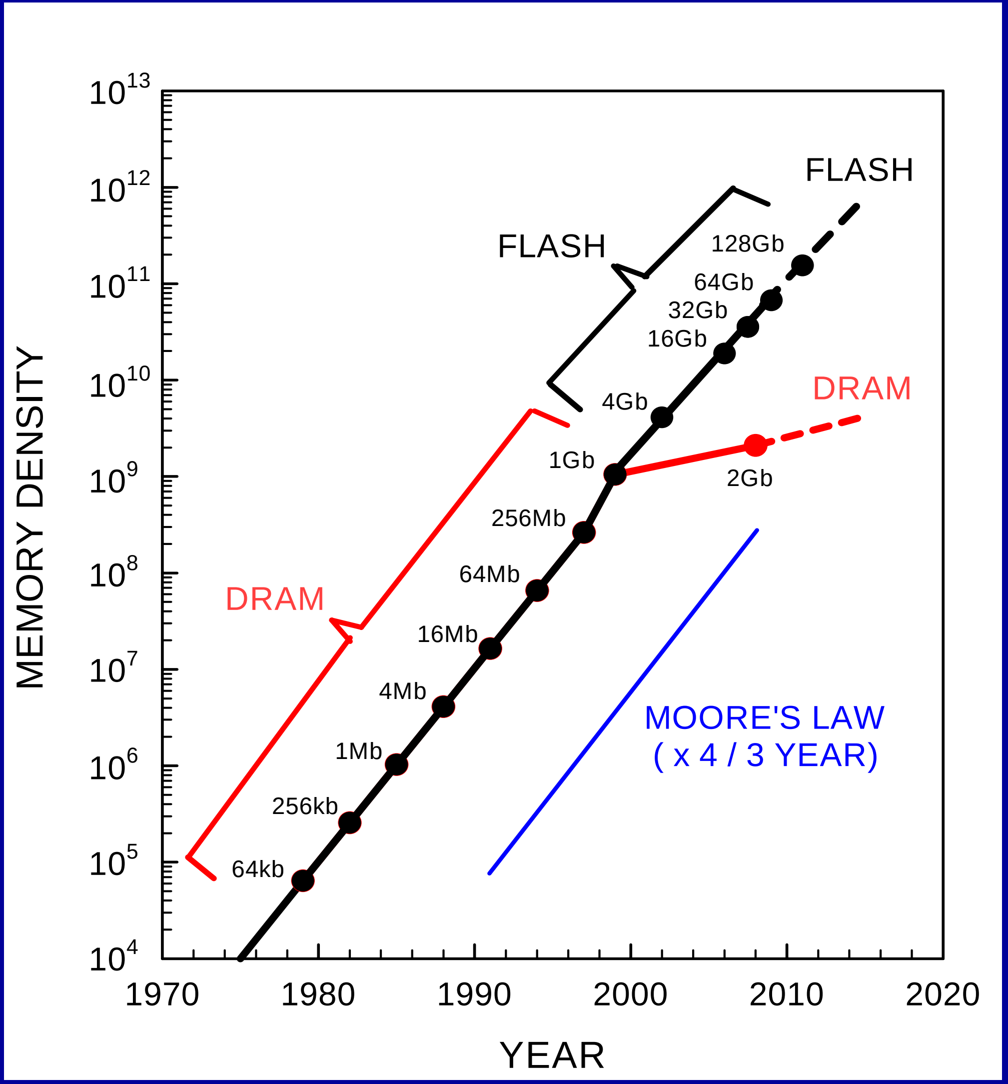


32 Gb FLASH MEMORY

(17 V   40nm   230 mm^2 0.0098μm^2/cell)



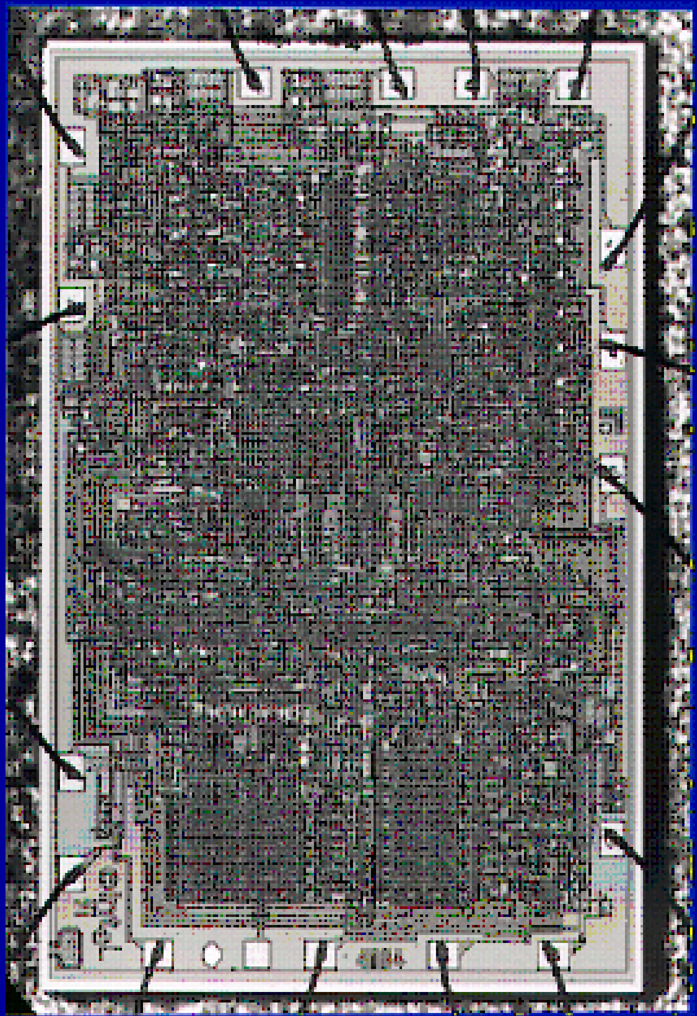
MOORE'S LAW



FLASH
FLASH
DRAM
DRAM
128Gb
64Gb
32Gb
16Gb
4Gb
1Gb
2Gb
256Mb
64Mb
16Mb
4Mb
1Mb
256kb
64kb
MOORE'S LAW
(x 4 / 3 YEAR)
MEMORY DENSITY
YEAR
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
1970
1980
1990
2000
2010
2020

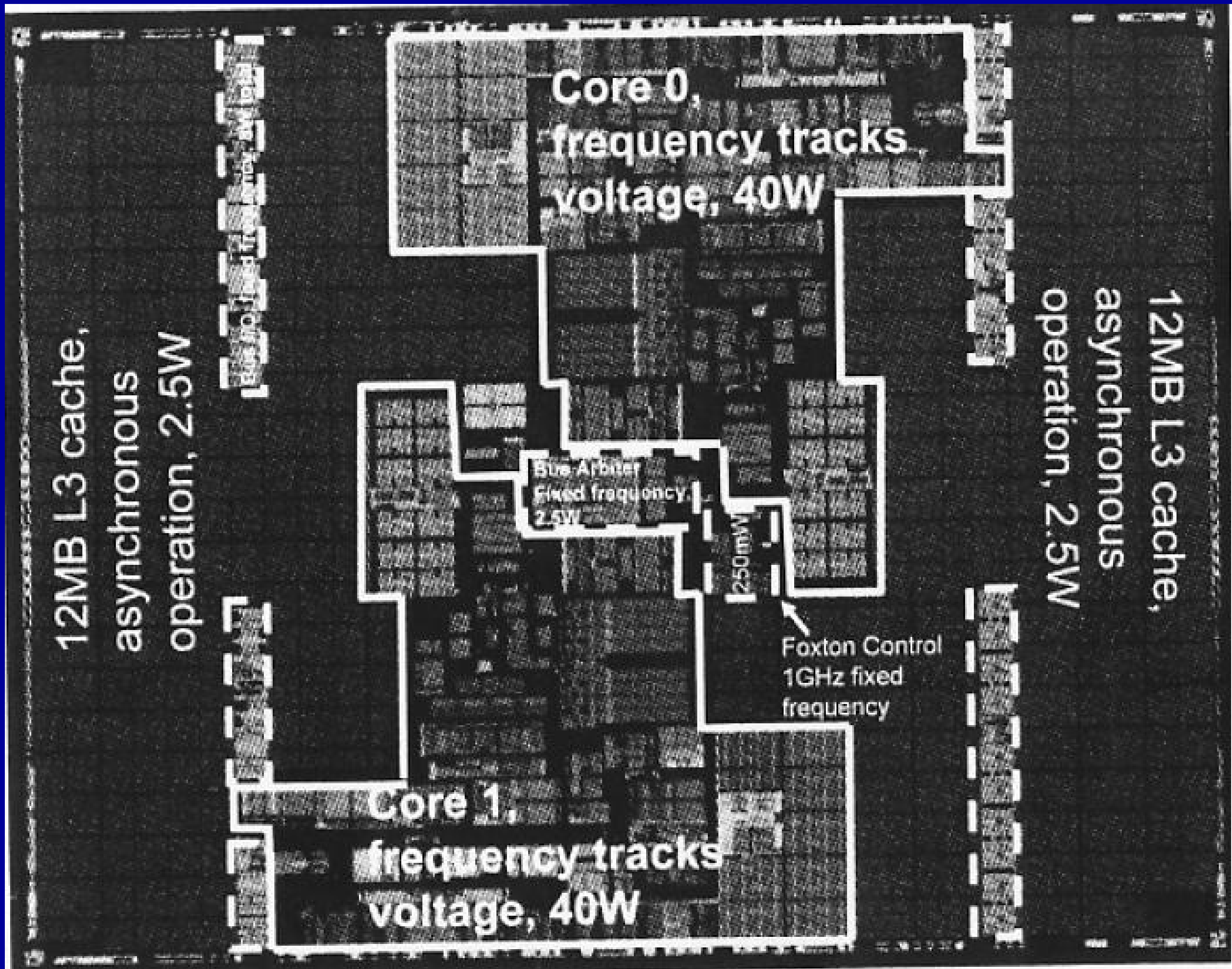
FIRST MICROPROCESSOR (4004 by Intel 1971)

(2300 Transistors 12 mm^2 8μm 750 kHz)

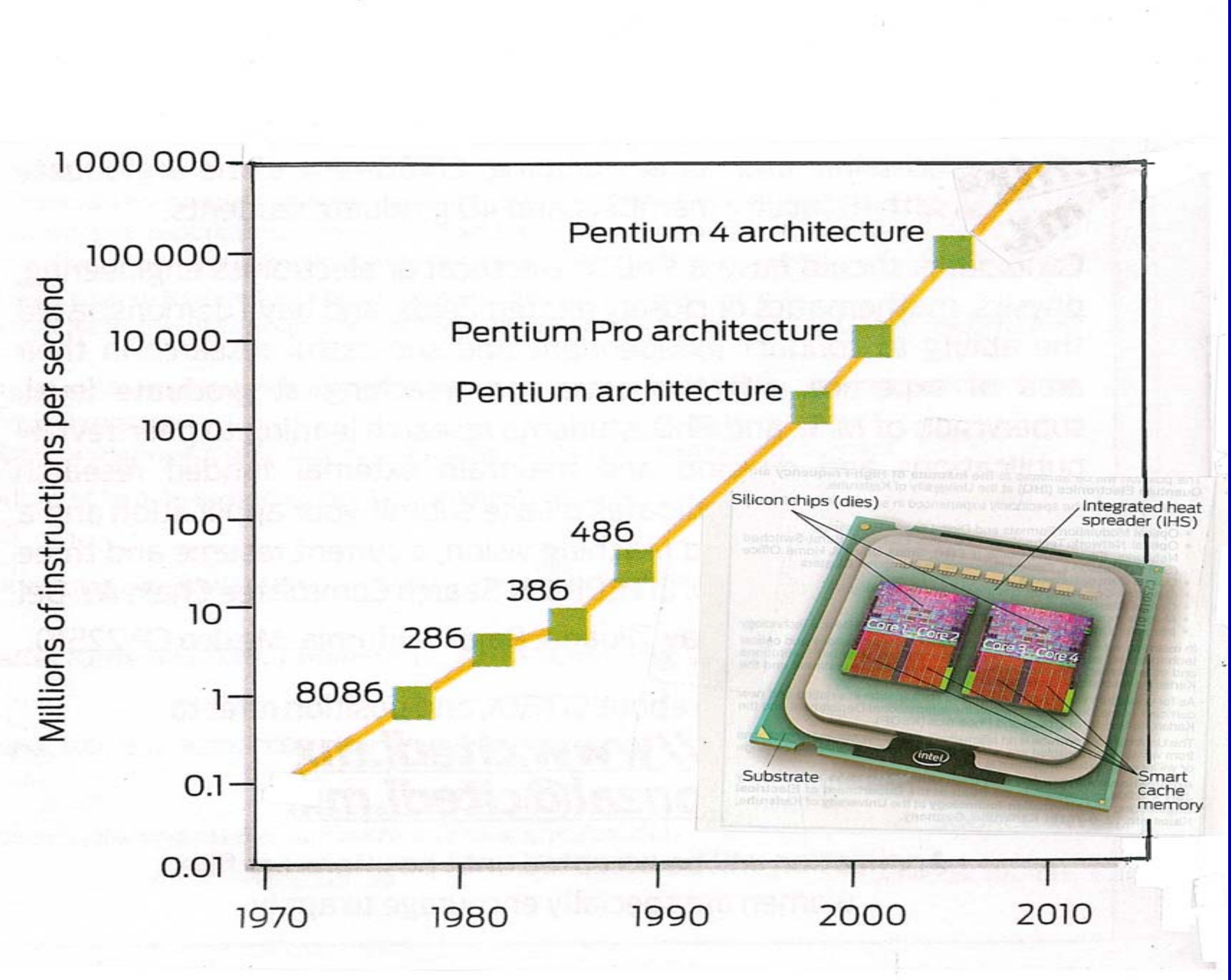


ITANIUM MICROPROCESSOR

(1.72 Billion Transistors 90nm 595 mm2 2 GHz)



CPU PERFORMANCE TREND (1971-2010)



PROGRESS IN MICROELECTRONICS

Year	1959	1970-1971	2008	Ratio
Design Rule (μm)	25		0.045	550 ↓
V_{DD} (V)	5		1.0	5 ↓
Wafer diameter (mm)	25		300	12 ↑
Devices per chip	6		32×10^{9}	5×10^{9} ↑
DRAM density (bit)	–	1k	2G	2×10^{6} ↑
Nonvolatile memory density (bit)	–	2k	32G	16×10^{6} ↑
Microprocessor performance (MIPS)	–	0.1	10^{5}	10^{6} ↑
Transistor shipped / year	10^{7}		5×10^{18}	5×10^{11} ↑
Average transistor price ($)	10		5×10^{-8}	2×10^{8} ↓

MAJOR CHALLENGES

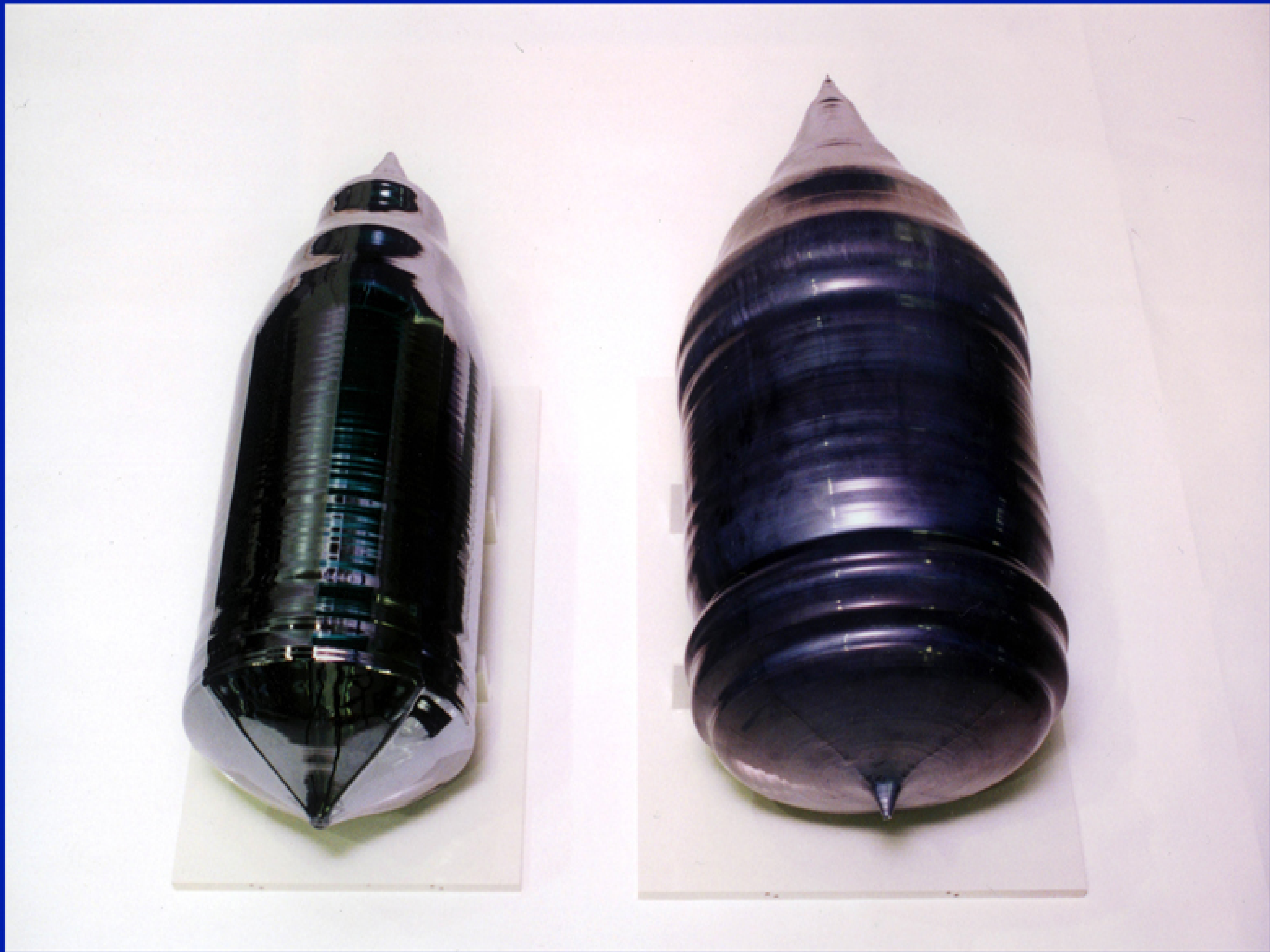
How long can the microelectronic industry maintain it historical rate of performance and cost improvement?

- Super-large-diameter wafer
- Sub-100 nm lithography
- Deca-nano devices
- Interconnect
- Economic considerations

WAFER CHALLENGES

- Difficulties in crystal pulling of large-diameter crystals
  - large crystal weight (> 200 kg for 300 mm wafers)
  - damping of thermal convection for large volume of melt
- Elimination of crystal originated pits (COP)
  - COPs are voids of diameters 10~100 nm
  - 10^5 COPs/cm^3 for 200 mm wafers
  - Elimination of COPs is necessary for 300 mm wafers

SILICON INGOTS
(300 mm and 400 mm)



450 mm SILICON WAFERS

- **Production Cost**

  For Cu/low K 32 nm process, the production cost per unit wafer area is expected to be reduced by 20~25% as compared to 300 mm wafer

- **Initial Production**

  Intel, Samsung, and TSMC are planning their pilot productions around 2010-2012

LITHOGRAPHY CHALLENGES

- Optical Lithography
  - How far can immersion lens and hologram masks extend the 193 nm ArF system?
  - Do we need the EUV system to support sub-25nm technology nodes?
- Nonoptical lithography systems
  - Electron-beam projection lithography (EPL)
  - X-Ray lithography (XRL)
  - Ion-beam projection lithography (IPL)
- Lithography-independent nanotechnology
  - Vertical MOSFET
  - Self-assemble
  - Self-organization

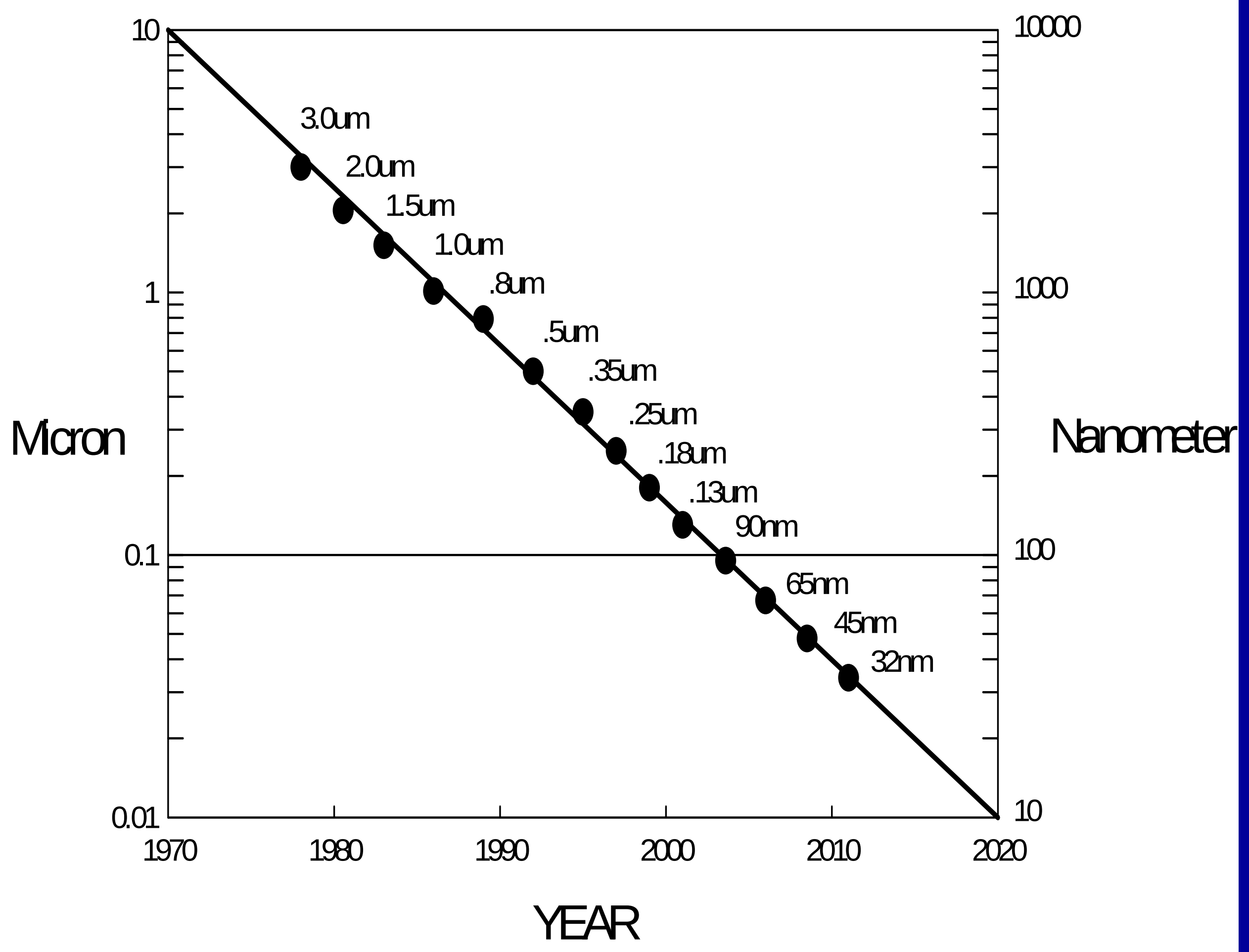
OPTICAL LITHOGRAPHY OPTIONS

- **Water-Based Immersion with Double Patterning**
  - most straight forward extension of 193 nm lithography system, but will double the cost
  - severe impact on tool requirement like overlay
- **Non-Water-Based Immersion**
  - use liquid with refractive index higher than water to increase NA (>1.35)
  - require currently unavailable lens materials
- **Extreme-Ultra-Violet (EUV) System with λ =13.5nm**
  - EUV is the most extendable lithography technology
  - first full-field tools available in 2006
  - additional progress needed on EUV sources, resists, and masks

DEVICE CHALLENGES

- Planar MOSFET Scaling
- MOSFET with Performance Boosters
- Quasi-planar SOI FinFET
- Logic Device Options
- Nonvolatile Semiconductor Memory (NVSM)
- Nonvolatile Memory Options

FEATURE SIZE TREND



MOSFET with PERFORMANCE BOOSTERS

- **Strain / Stress Engineering**

  to alter inter-atomic spacing in the channel region to improve mobility (e.g., SiN overlayer, SiGe or Ge source/drain, Ge stressor, buried SiGe strain-transfer structure)

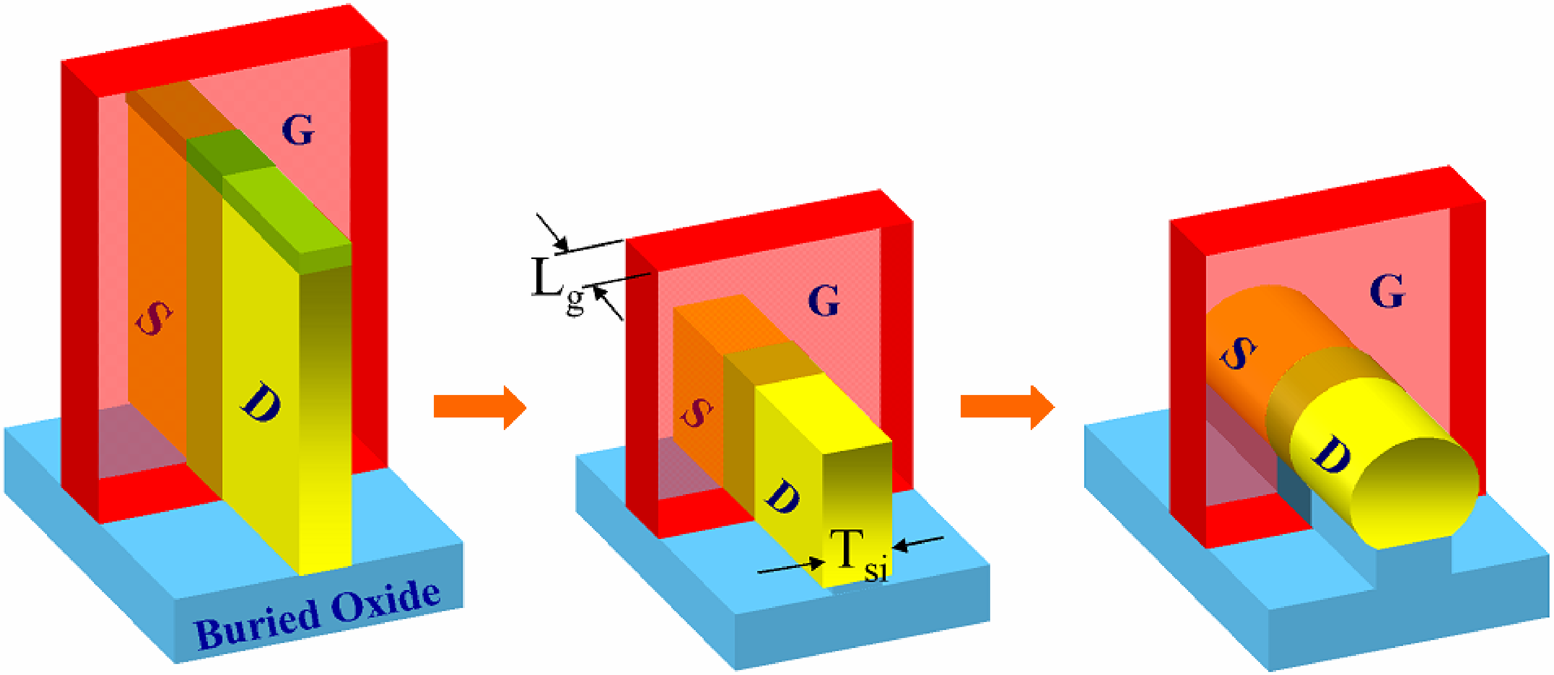
- **Contact Resistance Engineering**

  to reduce series resistance in source and drain regions to improve I_{Dsat} (e.g., metal-semiconductor barrier height adjustment, novel alloy silicides, Schottky-barrier source and drain – $ErSi_2$ for NMOS, PtSi for PMOS)

- **Gate Stack Engineering**

  to eliminate gate depletion effect to increase gate capacitance (e.g., dual metal-gate process, tuning metal-silicide work function)

EVOLUTION OF FinFET

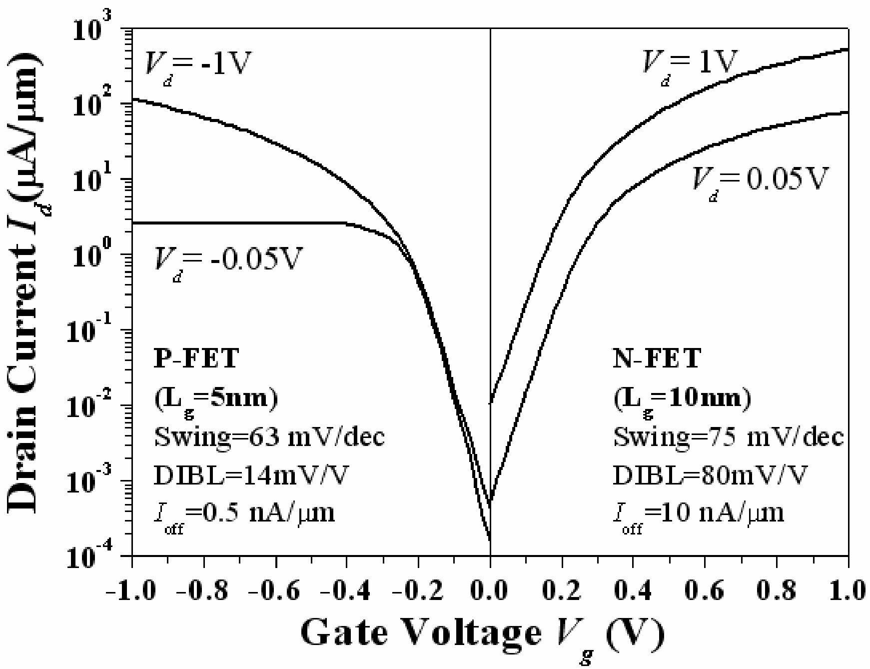


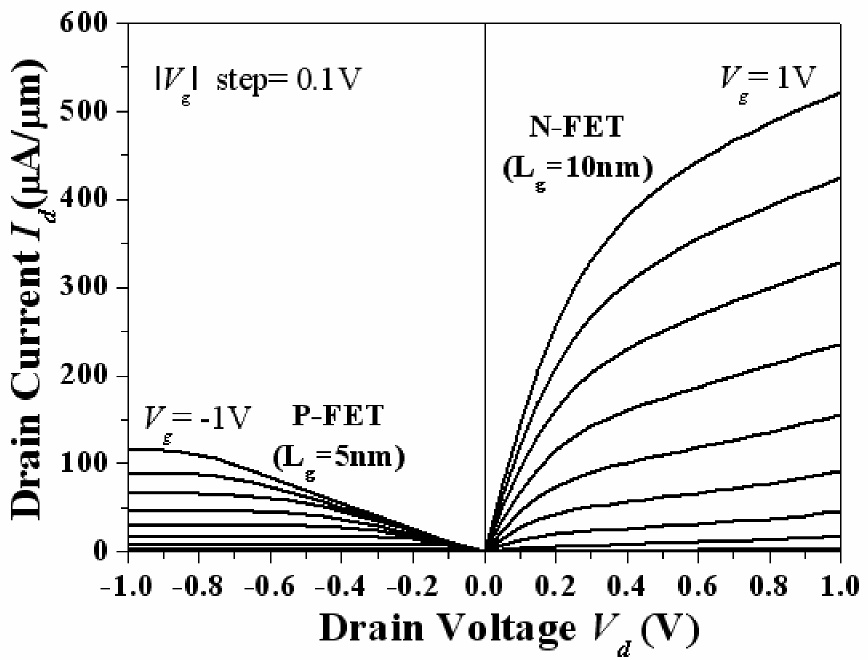
Double-Gate FinFET (T_{si} = $^2/_3$ L_g)

Omega FinFET (T_{si} = L_g)

Nanowire FinFET (T_{si} = $2L_g$)

5 nm P-TYPE/ 10 nm N-TYPE NANOWIRE FinFET





LOGIC DEVICE OPTIONS

- **Carbon Nanotube Field-Effect Transistor (CNFET)**
  - difficulty in contacting small diameter CNTs
  - difficulty in forming nanotubles with desired physical features and orientation
  - difficulty in elimination of ambipolar conduction

- **Molecular Devices**
  - limitation in operating temperature
  - difficulty in making contacts to individual molecules

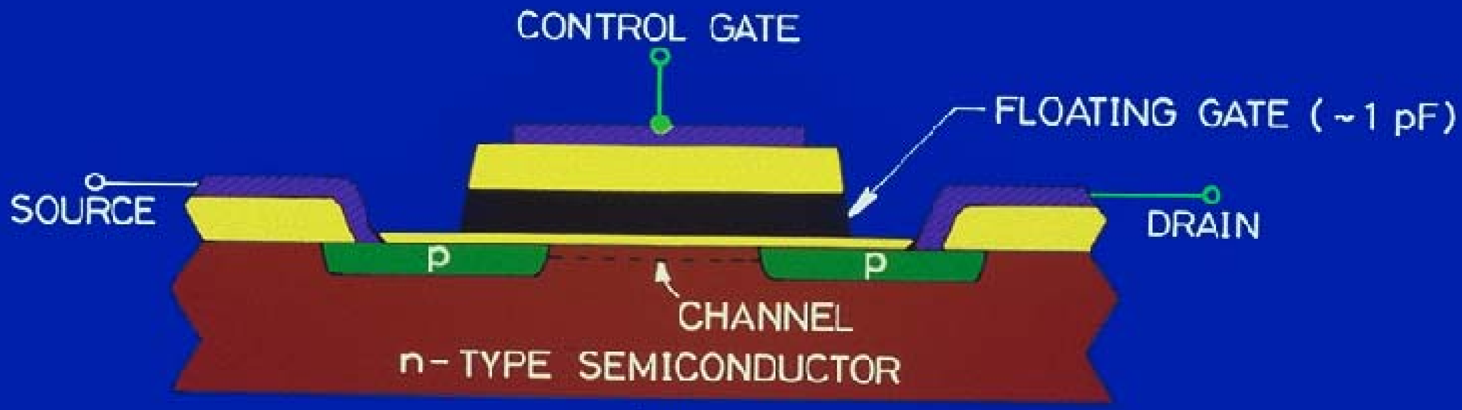
- **Quantum-dot Cellular Automata (Single - Electron Parametron)**
  - limitation in operating temperature
  - sensitivity to random background charge and low speed

- **All above options suffer from parasitic capacitance and resistance which dominate device performances**

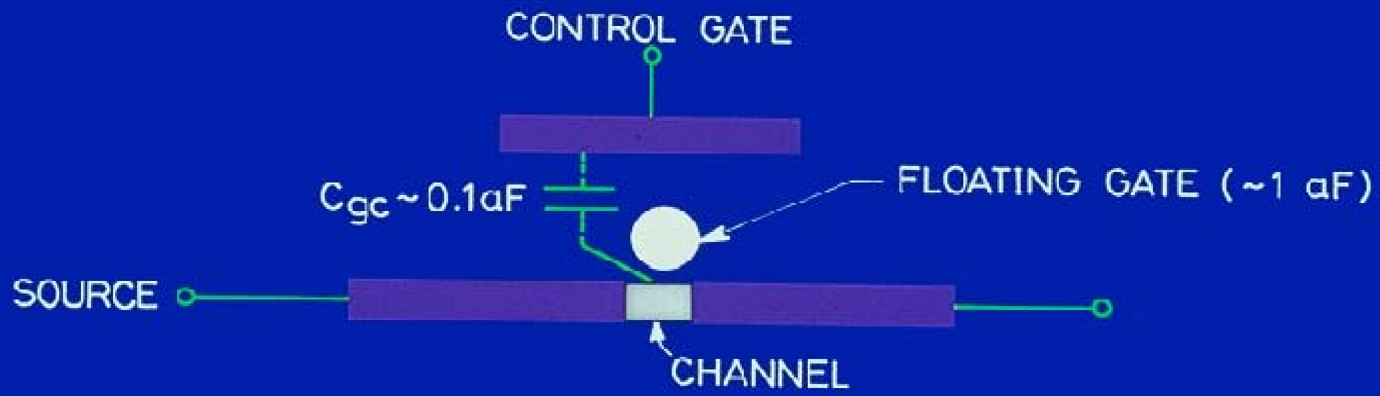
FLOATING-GATE NONVOLATILE SEMICONDUCTOR MEMORY

- The floating-gate nonvolatile semiconductor memory (NVSM) is the most important memory device. NVSM family includes EPROM, EEPROM, and Flash Memory
- There are more NVSM cells produced in the world than any other semiconductor device ($6x10^{18}$ bites in 2007, i.e., more than 800 million bits for every person on earth)
- Flash Memory (NAND) is cheaper than DRAM, and its density is getting close to hard disk drive
- Two limiting cases of floating-gate NVSM:
  - SONOS - when the thickness of the floating gate is reduced to zero, we have an MNOS memory (and its new version, the SONOS)
  - Nano-floating-gate memory – when the length of the floating gate is reduced to 5-10 nm, we have a nanocrystal or nano-floating-gate memory

NONVOLATILE SEMICONDUCTOR MEMORY (NVSM)



(a)



(b)

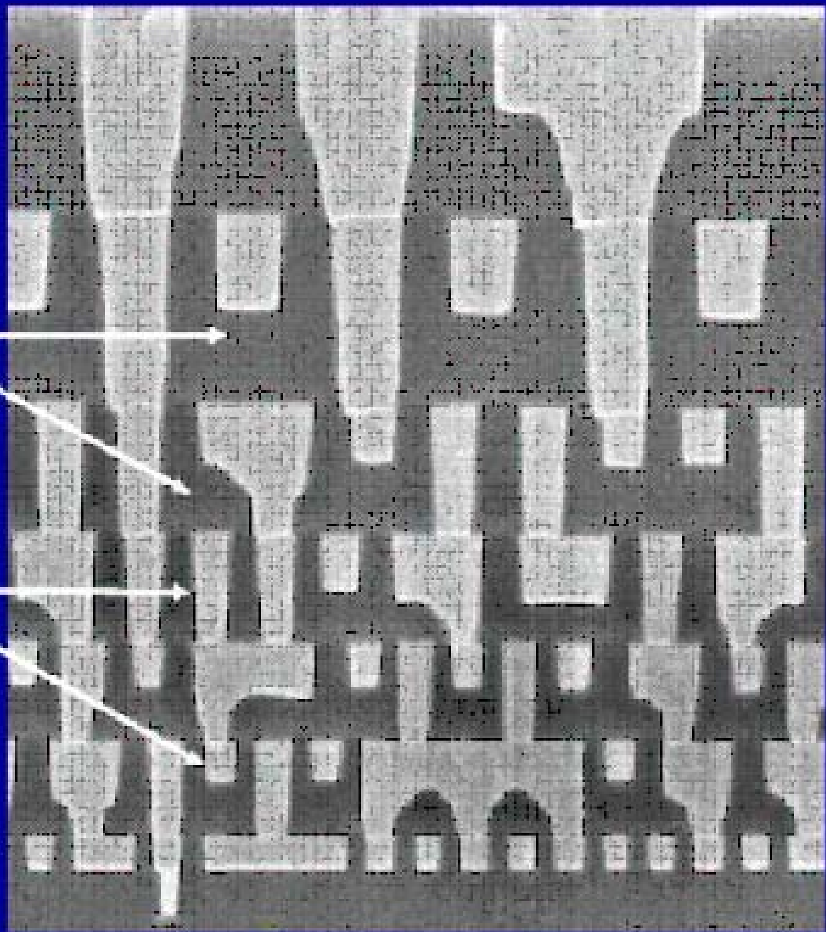
NONVOLATILE MEMORY OPTIONS

- **MRAM** (Magneto-resistive Random Access Memory) : based on tunneling Magneto-resistance effect
- **FeRAM** (Ferroelectric RAM) : based on remanent polarization in perovskite materials
- PCRAM (Phase-change RAM): based on reversible phase conversion between the amorphous and the crystalline state of a chalcogenide glass, which is accomplished by heating and cooling of the glass
- **RRAM** (Resistance RAM) : based on change in resistance with applied electric field
- **Polymer Memory** : based on resistance change of polymer at cross point of metal layers
- **Millipede Memory** : based on concept similar to punch cards, using thermally assisted, rewritable displacement media such as PMMA

INTERCONNECT CHALLENGES

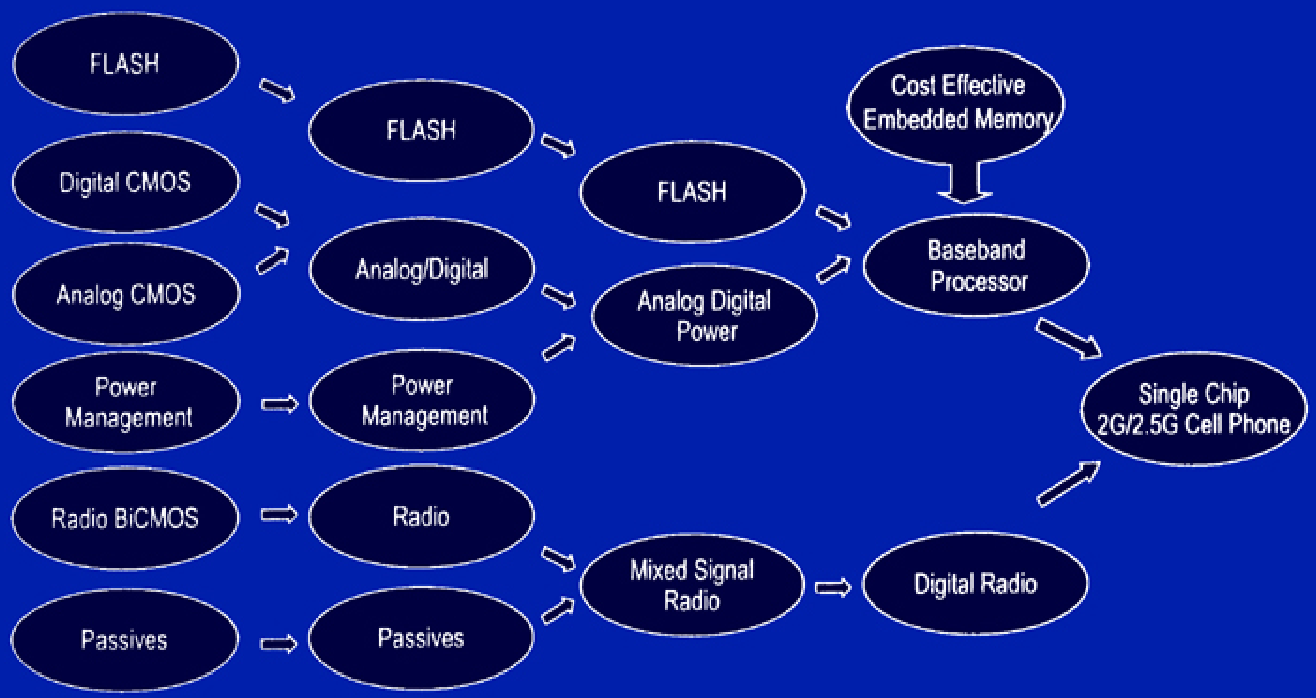
- Low parasitic R and C to improve circuit speed
- Low power dissipation (power~CV^2)
- Scaling limit of multilevel interconnect
- System-on-chip, network-on-chip, superchip to minimize interconnect length
- Interconnect options at sub-25nm regime

45 nm GENERATION INTERCONNECTS



SYSTEM-ON-CHIP INTEGRATION STRATEGY

FOR 3G/4G CELLULAR PHONES



INTERCONNECT OPTIONS At Sub-25nm REGIME

- Metallic Carbon Nanotube (Single Wall or Multi-wall)
  - long mean free path (>1 µm, 100 times of Cu) and low resistivity (5 µΩ–cm)
  - can sustain current density $>10^9$ A/cm^2 (100 times of Cu)
- Conducting Polymer
  - may be useful for molecular electronic
- Metallized DNA
  - may be useful for DNA template for self-assembly
- Metallic Nanowire
  - low resistivity
  - can sustain current density $>10^8$ A/cm^2
- Silicon Microphotonics

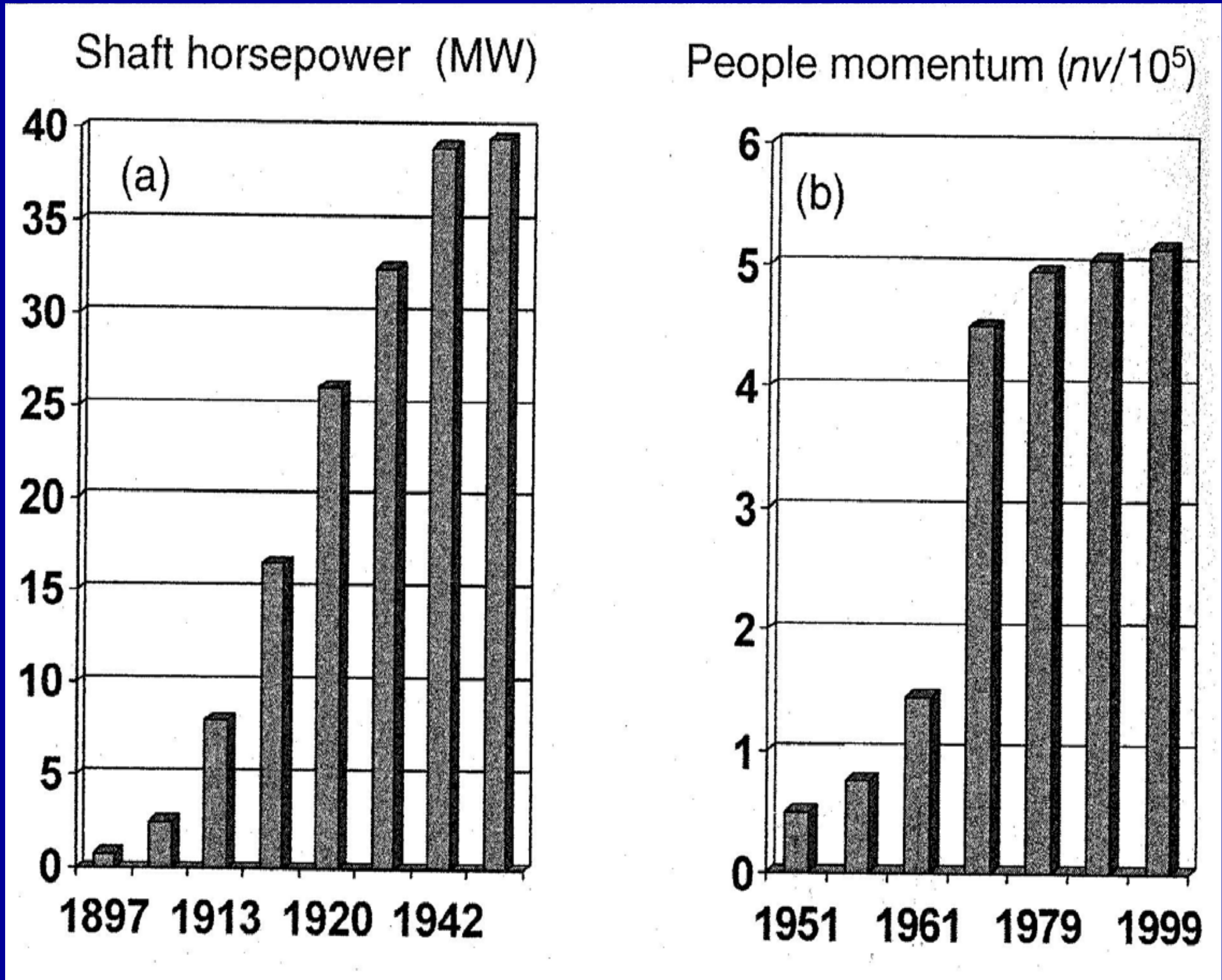
SILICON MICROPHOTONICS
A MAJOR INNOVATION FOR INTERCONNECT

- Photonic components
  - Photon creation, e.g., silicon-erbium LED
  - Photon propagation, e.g., Si/SiO_2 optical fiber, $\bar{n}$ (Si) = 3.5, $\bar{n}$(SiO_2) =1.5
  - Photon detection, e.g., SiGe alloy.
- Advantages
  - Minimizes RC delay
  - Provides precise clock distribution and system synchronization
  - Reduces power dissipation
  - Improves or minimizes cross talk, voltage isolation, impedance matching, and pin inductance

ECONOMIC CHALLENGES

- **Skyrocketing wafer fab cost**
  - **500 time increase since 1975 : $6M (1975), $3B (2005), ~$10B (2020)**
- **Innovative processes needed to lower manufacturing cost**
- **New applications will broaden electronic market**
  - **By 2030, semiconductor industry may reach $1.6 trillions**
  - **By 2030, electronic industry may reach $10 trillions and constitutes 10% of Gross World Product**

METRIC OF PROGRESS
For Marine Turbines and Jet Passenger Aircraft



METRIC OF PROGRESS (CONTINUED)

- For marine turbines: *shaft Horsepower* has been flat since 1942
- For jet passenger aircraft: *people momentum* has been flat since 1979
- But the marine and aircraft industries have diversified. There is a proliferation of types of ship and aircraft, carefully chosen for specific applications. The discriminators now are fuel efficiency, in-cabin or in-flight comfort, and ecological friendliness of the ship or aircraft
- For nanoelectronics: *The Moore's Law*. But the diversification has already begun. For example, the raw computing power is secondary to the range of applications and services that can be provided by a single cellular phone

TOP 30 WORLD MARKETS IN YEAR 2030

	Market	Sales ($ Billions)
*	Portable Data Communications	1260.
*	PC	940.
*	Mobile Phone Service	760.
*	CPU	600.
*	Digital Contents Products	540.
*	Magnetic Memory	500.
*	Electronic Commerce	500.
*	Network Information Service	460.
*	High Density Mag. Memory Mat.	460.
*	Systems-On-Chip	420.
*	Home Medical Equip.	420.
*	Internet	400.
*	CATV	400.
	Intelligent Transportation Syst.	380.
*	Agents Software	360.

Market	Sales ($ Billions)	
Ultra-thin Monitor	340.	*
IC Card	330.	*
Ground-Wave Broadcasting	320.	*
DNA Agricultural Products	320.	
Multi-Purpose Communication Equip.	310.	*
Semiconductor Equip.	300.	*
Electrical Vehicle	300.	
Wall Ultra-thin TV	290.	*
Mobile TV	280.	*
Direct Inject. Vehicle	280.	
ITS Equipment	280.	
DNA Processed Food	270.	
LCD	240.	*
Clone	230.	
Fuel-Cell Car	220.	

* Nanoelectronics related 22 markets : $ 10 trillions.

CONCLUSION

- In the past five decades, microelectronics has been responsible for the rapid growth of the global electronic industry which is now the largest industry in the world (> $ 2 trillions)

- There are many major challenges in nanoelectronics: large wafer, sub-100 nm lithography, deca-nano devices, interconnect, and economic challenges

- Super-large-diameter wafers will be adopted as long as the production cost per unit area can be reduced

- The 193 nm ArF system with immersion lens can support the 45 nm technology node. We may need EUV systems for sub-25nm technology nodes

CONCLUSION (CONTINUED)

- The ultimate logic device will be the MOSFET with performance boosters, and the ultimate memory device will be a nonvolatile memory (possibly a member of the floating-gate family)
- IC performance will be limited by interconnect. For sub-25um ICs, two options are the metallic CNT and the silicon microphotonics
- Low-cost manufacturing processes and broadened electronic applications will support the growth of the nanoelectronics
- The electronic industry will remain to be the largest industry in the world for the next five to ten decades. However, we must develop innovative nanoelectronic technologies to meet the aforementioned challenges