Call for Papers

THE 40TH ANNIVERSARY

2008 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference — September 24–26, 2008
Short Course & Special Events — September 23, 2008
Place — Tsukuba International Congress Center, Japan (EPOCHAL TSUKUBA)

CONFERENCE THEME

"Device and Material Innovations for Novel System Integration"

Paper Deadline—May 8, 2008
Late News Paper Deadline—July 28, 2008

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS
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IEEE Electron Devices Society
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ssdm 2008

Web Site_http://www.ssdm.jp

Call for Papers

2008 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

THE 40th ANNIVERSARY

Conference: September 24-26, 2008
Short Course (in Japanese): September 23, 2008
Special Events: September 23-26, 2008

The 2008 International Conference on Solid State Devices and Materials (SSDM2008) will be held from September 24 to September 26, 2008 at Tsukuba International Congress Center (Tsukuba, Ibaraki, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. This year the SSDM, which is celebrating its 40th anniversary, is organized to have 13 program subcommittees covering circuits and systems, as well as devices and materials. A one-day short course and special events celebrating the 40th anniversary are also scheduled prior to the conference. More information about SSDM 2008 is available online at:

http://www. ssdm.jp

The 40th Anniversary Special Events

1. An extra DVD which includes past 40 years' SSD & SSDM all papers will be distributed for all participants.

2. A hardcover book entitled "40 years of SSDM, Past, Present and Future (Tentative)" will be also distributed for all participants.

3. Panels of past "SSDM Award" will be exhibited during the conference (September 24-26, 2008).

4. A technical seminar on "Research and Development Activities in Science City of Tsukuba" will be organized in the afternoon of September 23, 2008, prior to the conference. All presentations are given in English.

5. A welcome reception will be held in the evening of September 23, 2008, prior to the conference. Both the seminar and the reception are open to all participants without additional fees.

PLENARY SESSIONS

Plenary Speakers:

"CMOS Paradigm Change through Material Integration on a Chip"

M. Hirose (AIST, Japan)

"One Dimensional Electronics: Physics or Technology?"

M. Lundstrom (Purdue Univ., USA)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2008 conference, thirteen program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Gate Stack / Si Processing Science

(Chair: J. Yugami, Renesas Tech. Corp.)

This subcommittee covers all the innovative front-end-of-line process technologies and sciences for advanced silicon-based LSI devices. Not only the gate stack technology but all the new concepts on Si-based front-end process technologies are welcome. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, and metal gate technologies, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow junction formation, novel diffusion/oxidation, and high-precision etching; (3) reliability physics and analysis; and (4) characterization and modeling of a Si process.

Invited Speakers:
"Low Vt Metal-Gate/High-k CMOS from Understanding the Mechanism to Innovative Solution"
A. Chin (National Chiao Tung Univ., Taiwan)
"Stress-Induced Degradation of High-k/Metal Gate Stacks: Identifying "Weak Link" in the Multilayer Dielectric"
G. Bersuker (SEMATECH, USA)
"Material Engineering for High-k/Germanium MISFETs"
K. Kita (Univ. of Tokyo, Japan)
"Dopant and Potential Profiling with Atomic Resolution by Scanning Tunneling Microscopy"
T. Kanayama (MIRAI-ASRC and AIST, Japan)

Area 2

Characterization and Materials Engineering for Interconnect Integration

(Chair: Y. Hayashi, NEC Corp.)

Technologies and sciences that cover a Si back-end-of-line (BEOL) process are discussed, including package technology. Low-k materials have been in practical use; however, they brought new, difficult issues by scaling, especially in reliability and package areas. Innovations and new ideas are needed in the BEOL by introducing new materials with sophisticated characterization as well as novel BEOL process/structures with system integration points of view. Papers are solicited in the following areas: (1) characterization methodology for materials, mechanical and electrical properties in small geometry, metrology and yield improvement; (2) materials, process and packaging technologies for advanced Cu/Low-k interconnect; (3) reliability phenomena and physics, such as EM, SIV, TDDB, and modeling/prediction; (4) passive components for RF or High-speed operations; (5) new structures and materials on future interconnects, such as a 3-D structure, a CNT interconnect, an on-chip optical interconnect, and BEOL-based memory applications, i.e. MRAM, and PRAM.

Invited Speakers:
"High-Frequency Magnetic Shielding Technology for Electronic Devices"
M. Yamaguchi (Tohoku Univ., Japan)

"Aberration Corrected Microscopy and Spectroscopy for Pico-Meter Characterization of Device Materials"

K. Takayanagi (Tokyo Tech., Japn)

"Plasma Physics for Reducing PID in Nano-Structure Patternings"

T. Makabe (Keio Univ., Japan)

"Interconnect and Packaging Technology for CMOS Image Sensors"

J. Gambino (IBM, USA)

"Plastic Material Solutions for Advanced Thin Packages"

H. Tanaka (Sumitomo Bakelite Co., Ltd., Japan)

"Metal Resistivity in Narrow Interconnects Lines"

S. Maitrejean (CEA-LETI, France)

Area 3

CMOS Devices /Device Physics

(Chair: M. Hane, NEC Corp.)

The aim of this area is to discuss advanced silicon device technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel or any high-mobility channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, multi-channels, or nano-wires; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science in conjunction with the increasing variability of device parameters, fluctuations of fabrication parameters or the intrinsic atomistic nature.

Invited Speakers:

"III-V CMOS: Challenges and Opportunities"

J. A. del Alamo (Massachusetts Inst. of Tech., USA)

"Simulation of Material and Strain Engineering of Tunneling Field Effect Transistor with Subthreshold Swing Below 60mV/dec"

G. S. Samudra (National Univ. of Singapore, Singapore)

"Recent Progress in Carbon Nanotube Electronics - Materials, Devices, Circuits, and Modeling"

H. S. Philip Wong (Stanford Univ., USA)

Area 4

Advanced Memory Technology

(Chair: A. Nitayama, Toshiba Corp.)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward ‘‘high speed and high density, broadband and mobile.’’ Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited Speakers:

"Overview and Future Challenge of DRAM Technologies"
G. Jeong (Samsung Electronics Co., Ltd., Korea)

"Impact of Random Telegraph Noise (RTN) on Future Memory"
H. Miki (Hitachi, Ltd., Japan)

"Overview and Future Challenges of 3D Flash Technologies"
H. Aochi (Toshiba Corp., Japan)

"Overview and Future Challenges of Advanced Material for FeRAM"
H. Funakubo (Tokyo Tech., Japan)

"Current Development Status and Future Challenge of Spin Torque Transfer MRAM Technology"
K. Ito (Hitachi, Ltd., Japan)

"Interpretation of Resistive Switching in NiO Thin Films"
I. K. Yoo (Samsung Electronics Co., Ltd., Korea)

Area 5

Advanced Circuits and Systems

(Chair: S. Kawahito, Shizuoka Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following; (1) advanced digital, analog, and mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication circuits; (4) power devices and circuits as well as power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); (7) LSI testing technology; (8) three-dimensional IC technology; (9) MEMS (passive) devices as well as circuits, RF MEMS; (10) sensor devices and circuits; (11) thin film transistors and circuits; and (12) organic devices and circuits.

Invited Speakers:
"Process and Circuit Technologies for MEMS Sensors"
K. Maenaka (Univ. of Hyogo, Japan)
"Low-Power Millimeter-Wave CMOS Pulse Transceiver"
M. Fujishima (Univ. of Tokyo, Japan)
"Nano CMOS Characterization and Device Modeling for Advanced Memory Design"
J. H. Lee (Kyungpook National Univ., Korea)
"The Dynamic-Range Enhancement Technologies for CMOS Image Sensors"
S. Sugawa (Tohoku Univ., Japan)
"Power Device Evolution Challenging to Silicon Material Limit"
A. Nakagawa (Toshiba Corp., Japan)
"Modeling of High Voltage MOSFETs for Device/Circuit Optimization"
M. Miura (Hiroshima Univ., Japan)

Area 6

Compound Semiconductor Circuits, Electron Devices and Device Physics

(Chair: T. Hashizume, Hokkaido Univ.)

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, and other materials. Papers are

solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures; (2) high-voltage or high-temperature electron devices and circuits; (3) microwave and millimeter-wave amplifiers, oscillators, switches, and other ICs; (4) high-speed digital ICs and mixed-signal ICs; (5) theory and physics of electron devices; (6) characterization techniques for devices and ICs; (7) innovative device processing and packaging; (8) reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited Speakers:
"GaN on Silicon RF Devices: Current Status and Future Directions"
I. Kizilyalli (Nitronex Corp., USA)
"GaN HEMTs: Present Status and Future Prospect"
T. Kikkawa[1] and S. Nakajima[2]
([1]Fujitsu Labs. Ltd. and [2]Eudyna Devices Inc., Japan)
"Development of InP/GaAsSb Terahertz Bandwidth DHBTs"
C. R. Bolognesi (Swiss Federal Inst. of Tech., Switzerland)
"Failure Mechanisms of GaN-Based Transistors in On- and Off- State"
E. Zanoni (Univ. of Padova, Italy)

Area 7
Photonic Devices and Device Physics
(Chair: H. Yamada, Tohoku Univ.)

The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs, photodetectors, SOAs, and OEICs; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic crystal materials and novel functional devices; (4) optical switches, modulators, and MEMS; (5) optical wavelength converters, nonlinear optical devices, and all-optical switches; (6) waveguide components, PLCs and integrated photonic circuits; (7) material and device processing and

characterization techniques; (8) hybrid and monolithic integration, packaging and moduling; (9) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (10)linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (11) novel phenomena and applications including slow light, fast light, optical memory, and optoelectronic tweezers, etc.

Invited Speakers:
"Photonic/Electronic Integration for On-Chip Interconnects"
W. Green (IBM, USA)
"High-Performance InAs Quantum-Dot Lasers with Temperature-Stable Lasing Waevlength"
D. Mowbray (Univ. of Sheffield, UK)
"Hybrid AlGaInAs-Silicon Evanescent Racetrack Laser"
A. W. Fang (Univ. of California, Santa Barbara, USA)
"Recent Progress of Self-Organized Quantum Dots for Solar Cell Applications"
Y. Okada (Univ. of Tsukuba, Japan)

Area 8
Advanced Material Synthesis and Crystal Growth Technology

(Chair: A. Yamada, Tokyo Tech.)

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and structures, nitride compounds, CNT, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) nitride-related compound semiconductors; (3) novel synthesis, growth, and fabrication techniques; (4) carbon nanotubes; (5) nanowires and nanoparticles; (6) microscale and nanoscale 3-D structures; (7) characterization of fundamental properties.

Invited Speakers:
"InAs/InP Quantum Dots, Dashes, and Ordered Arrays"
N. Sritirawisarn (Eindhoven Univ. of Tech., Netherlands)
"Metalorganic Vapor Phase Epitaxy of III-Mn-V Epitaxial Thin Films for Spintronics"
B. Wessels (Northwestern Univ., USA)
"Advanced Synthesis for Si and ZnO Nanowires and Their Applications"
D. L. Kwong, S. J. Lee, X. W. Sun, G. Q. Lo, J. D. Ye and S. T. Tam (IME, NTU and NUS, Singapore)
"Low Temperature Epitaxial Growth of Semiconductors on Metal Substrates"
H. Fujioka (Univ. of Tokyo, Japan)

Area 9

Physics and Applications of Novel Functional Materials and Devices

(Chair: T. Fujisawa, NTT Corp.)

This session covers physics, applications and fabrication techniques of novel functional devices and quantum nanostructures. We strongly encourage novel, pioneering, and fundamental research works that would be influential in various solid state devices of various materials (semiconductors, metals, superconductors, magnetic and organic materials, etc.). Specific topics are (1) quantum phenomena in nanostructures; (2) quantum dots and single-electron devices; (3) resonant tunneling devices, (4) solid-state quantum computing and communications; (5) nanometer-scale characterization with spanning probe techniques; (6) nanofabrication techniques and self-organized phenomena; and (7) other novel devices, but are not limited to these subjects.

Invited Speakers:
"Spin Blockade and Lifetime-Enhanced Transport in Si/SiGe Quantum Dots"
M. A. Eriksson (Univ. of Wisconsin-Madison, USA)
"Spin Transport in a Single InAs Quantum Dot Attached to Ferromagnetic Electrodes"
T. Machida (Univ. of Tokyo, Japan)
"Single Artificial Atom Lasing"
J. S. Tsai (NEC Corp., Japan)

"Nanowire Impact Ionization Transistors (I-FETs)"
Y. C. Yeo (National Univ. of Singapore, Singapore)

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Area 10
Organic Materials Science, Device Physics, and Applications

(Chair: T. Kamata, AIST)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9) interfacial phenomena, LC devices, etc.

Invited Speakers:
"To be announced"
B. Batlogg (ETH Zurich, Switzerland)
"Recent Progress in Organic TFT for Active Matrix Display"
S. Lee (Samsung AIT, Korea)
"Material Studies for Organic FET"
T. Tsutsui (Kyushu Univ., Japan)
"A Novel Image Sensor with Organic Photoconductive Films"
S. Aihara (NHK, Japan)

Area 11
Micro/Nano Electromechanical and Bio-Systems (Devices)

(Chair: H. Tabata, Univ. of Tokyo)

This session focuses on micro/nano electromechanical systems(MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices and bio-sensors are

widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems(M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications; (6) molecular imaging and spectroscopy for bio devices.

Invited Speakers:
"Compound Nanoimprint Processes and Their Applications for Functional Nanodevices"
J. Mizuno (Waseda Univ., Japan)
"Bio-Manipulation Based on Microfabricated Structures"
M. Washizu (Univ. of Tokyo, Japan)
"THz-Wave Generation and Applications"
K. Kawase[1,2], T. Shibuya[1,2] and K. Suizu[1]
([1]Nagoya Univ. and [2]RIKEN, Japan)
"FET-Based Biosensor for Detection of Biomolecules"
J. K. Shin (Kyungpook National Univ., Korea)

Area 12
Spintronic Materials and Devices
(Chair: M. Tanaka, Univ. of Tokyo)

This field covers spintronic materials (metals, semiconductors, insulators, hybrid structures, and nanostructures), spin-related phenomena, and device applications. Papers are solicited in the following areas (but are not limited to these areas): (1) ferromagnetic and/or half-metallic materials; (2) hybrid structures and nanostructures in which spin effects are apparent and important; (3) spin-dependent optical and transport phenomena; (4) spin dynamics; (5) spintronics devices

and systems including magnetic tunnel junctions and TMR devices, nonvolatile memory, magnetic sensors, spin-transistors, optical isolators, optical switches etc; (6) quantum information processing using spin states.

Invited Speakers:
"Beyond CMOS and Future Spin Devices"
G. Bourianoff (Intel Corp., USA)
"Spin Injection and Transport in Silicon"
B. T. Jonker (Naval Res. Lab., USA)
"Spin Dynamics and Microwave Related Devices"
H. Kubota (AIST, Japan)
"Magnetic Domain Wall Dynamics in GaMnAs"
F. Matsukura (Tohoku Univ., Japan)
"Spin Transport in III-V Ferromagnetic Semiconductor Heterostructures"
S. Ohya (Univ. of Tokyo, Japan)

Area 13

Applications of Nanotubes and Nanowires

(Chair: K. Matsumoto, Osaka Univ.)

All kinds of applications using nanotubes & nanowires are included in the scope of this sub-committee. Nanotubes & nanowires, e.g., carbon nanotube, BN nanotube, Si nanowire, compound semiconductor nanowire, layered nanowire, etc. are all included. Applications using nanotubes & nanowires in the scope are as follows; 1) Active electronic and optical devices, e.g., FET, HEMT, optical transistor, optical switch, and quantum devices including single electron transistor(SET), SET logics, resonant tunneling devices, quantum computing devices and so on. 2) All kinds of sensors, e.g., bio sensors, gas sensors, pressure sensors, acceleration sensors and so on. 3) Application for passive elements, e.g., wiring & via technology for future LSI and so on. 4) Nanomechanical application, e.g., probe applications for STM/AFM, tweezers, motors, oscillators and so on. 5) Fundamental research related to those applications of nanotube & nanowire, e.g., new growth technology, analysis of growth mechanism, new device fabrication process and so on. 6) New evaluation technology, e.g., TEM, SEM, Raman

scattering, photo luminescence and so on. 7) Theoretical analysis of device physics, new physics in the nanotube & nanowire, e.g., Tomonaga liquid, one dimensional quantum transport and so on.

Invited Speakers:

"Tunable Few Electron Double Dots in InAs Nanowires"

I. Shorubalko, A. Pfund, R Leturcq and K. Ensslin

(ETH, Switzerland)

"Si/SeGe Nanowire Technology Platforms and Device Applications Based on Top-Down Approach"

G. Q. Lo, N. Singh, K. B. Buddaharaju, J. Yu, J. Fu, S. C. Rustagi, N. Balasubramanian and D. L. Kwong

(IME, Singapore)

RUMP SESSIONS

Following two Rump Sessions have been organized on September 25 (Thursday).

Session A

"Can power semiconductor technology contribute to sustainable future?"

Organizer: S. Kimura (Hitachi, Ltd., Japan)
Moderator: I. Omura (Toshiba Corp., Japan)

Semiconductor technology advancement has been represented by the large scale integrated circuit, such as CPUs, in terms of nano-meter gate length, billions of transistors, GHz clock frequency and so on, along with the "Moore's law". These technologies have changed the society with the tremendous spread of the internet, the mobile digital equipments and other convenient so-called "on-line" systems and "ubiquitous" equipment all over the world. We do recognize that the success of semiconductor technology in this field has been brought about the human insatiable demand for convenient lifestyle.

Recent discussions on the global scale environmental issues, however, changed the view point to the semiconductor technology. The total electricity consumption of the world has been increased to 16,695 TWh which has already been equivalent to 32 % of total CO_2 emission. This fact implies that we cannot let the electricity consumption increase as we have done in the past, and the wider spread of the higher quality lifestyle to the world will be realized only by the dramatic improvement of efficiency in electric energy use, i.e. the power semiconductor devices have become the key technology for the sustainable future because they have the potential to improve the efficiency of power supply systems and motor drive systems dramatically.

In this rump session, we will discuss the status quo and prospect of the power semiconductors including new semiconductor materials, which has not been concentrated in SSDM sessions ever, and discuss the contribution of

the advanced Si devices and materials technologies to the future high efficient power semiconductors in contrast to the contribution of the compound semiconductors such as SiC and GaN in power devices and power electronics technologies.

Session B

"Nano-Device and Materials Innovations: What novel systems are you dreaming of?"

Organizers: Y. Horiike (NIMS, Japan)
K. Wada (Univ. of Tokyo, Japan)

Year 2008 celebrates 40th anniversary of SSDM. When we look back 40 years ago, the first Si integrated circuits demonstrated by R. Noyce et al. were just 7 years old. The ICs together with a Boolean Algebra have been a strong foundation of the present advanced information society. However, the progress seems slowing down and something extremely disruptive needs to be implemented to sustain our quality of life. There have been quite a few number of research activities currently being done to innovate devices, materials, and system architectures. In the present rump session, we will set up a table to get you updated with potential candidates - challenges and opportunities. Topics will be solicited, conventional Si and beyond.

SHORT COURSE

Short Course entitled "Progress in Si Technology Booster with Metrology/Evaluation Technique" will be held on Tuesday, September 23. All lectures are given in Japanese.

SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at http://www.ssdm.jp.

Please note that submissions by post will NOT be accepted.

Deadline for Submission is 24:00, May 8, 2008 (Japan time).

The two-page paper must be prepared in English in 8.5- ×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean, etc. fonts cannot be used for either figures or texts. The paper should report original, previously unpublished work, including specific results.

Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

POSTER SESSIONS

Some of the papers will be presented in the Poster Session. All authors of poster presentations are requested to give a short presentation.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed, without opportunity for further revision, in the extended abstracts which will be distributed to conference participants during the conference.

SPECIAL ISSUE in JJAP

Authors of papers accepted for presentation at SSDM 2008 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2009.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

Late News Papers Deadline is 24:00, July 28, 2008 (Japan time).

Notices of acceptance will be e-mailed by mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include plenary sessions, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented in or before 2002.

SSDM Paper Award

Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm_secretariat@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.

An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF).

BANQUET

The conference banquet will be held on the evening of Wednesday, September 24. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

REGISTRATION

Participants are required to register online at the conference web site http://www.ssdm.jp, in which the forms for registration, short course and banquet will be available in the beginning of June, 2008.

The registration and banquet fees are:

	Registration Fee		Short Course (in Japanese)	Banquet
	Before 24:00, Aug. 17 (Japan time)	After 0:00, Aug. 18 (Japan time)		
Regular	¥50,000	¥55,000	¥15,000	¥7,000
Student	¥7,000		¥3,000	¥4,000
Accompanied person				¥4,000

* Fees include tax.

VISA REQUIREMENT

Overseas participants who require a visa should consult the nearest Japanese Embassy. Please note that obtaining a visa may take much longer than you anticipate, and we strongly recommend that you commence the application process as soon as possible. If your visa application requires an invitation to attend the SSDM conference, please contact SSDM Secretariat, ssdm_secretariat@intergroup.co.jp.

LOCATION

SSDM2008 will be held at Tsukuba International Congress Center (EPOCHAL TSUKUBA).

2-20-3 Takezono, Tsukuba, Ibaraki
305-0032, Japan
Phone: +81-29-861-0001
Fax: +81-29-861-1209

Tsukuba International Congress Center has been contributing greatly to the continued development of science and technology, standing as the kernel place for such exchange, where people nearly 2 million have gathered since it was established in 1999. Just 50 km from Tokyo and 40 km from Narita Airport, the congress center is located in Tsukuba, the center of advanced technology, research and development, and the pre-eminent location for conventions.
http://www.epochal.or.jp/index.html

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho, Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2008-gb@or.knt.co.jp

Hotel Accommodations

KNT has blocked rooms at following hotels in Tsukuba for the conference period.
Reservations can be made through the conference website beginning in June.
If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

Hotel Name	**Okura Frontier Hotel Tsukuba**
Room Rates	Single: ¥ 12,000 Twin: ¥ 11,000 (per person, per night)
Hotel Deposit	¥ 20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-1364-1, Azuma Tsukuba-city, Ibaraki 305-0031, Japan
Phone	+81-29-852-1112
Access to Hotel	2 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	6 min. walk

Hotel Name	**Okura Frontier Hotel Tsukuba Epochal**
Room Rates	Single: ¥ 12,000 Twin: ¥ 11,000 (per person, per night)
Hotel Deposit	¥ 20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	2-20-1 Takezono, Tsukuba-city, Ibaraki 305-0032, Japan
Phone	+81-29-860-7700
Access to Hotel	8 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	Next to the site

Hotel Name	**Hotel Grand Shinonome**
Room Rates	Single: ¥ 7,350
Hotel Deposit	¥ 10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	488-1 Onozaki, Tsukuba-city, Ibaraki 305-0034, Japan
Phone	+81-29-856-2211
Access to Hotel	5 min. walk from Tsukuba Sta..
To Conference site	13 min. walk

Hotel Name	**Hotel Route Tsukuba**
Room Rates	Single: ¥ 7,000
Hotel Deposit	¥ 10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	1145-3 Hanamuro, Tsukuba-city, Ibaraki 305-0025, Japan
Phone	+81-29-860-2111
Access to Hotel	20 min. walk (or 5 min. by taxi) from Tsukuba Sta.
To Conference site	30 min. walk (or 10 min. by taxi)

Hotel Name	**Tsukuba Daily Inn**
Room Rates	Single: ¥ 6,930
Hotel Deposit	¥ 10,000
Check-in/out	Check-in:16:00/Check-out:10:00
Address	1-12-4 Sengen, Tsukuba-city, Ibaraki 305-0047, Japan
Phone	+81-29-851-0003
Access to Hotel	30 min. walk (or 7 min. by taxi) from Tsukuba Sta.
To Conference site	15 min. walk (or 3 min. by taxi)

Notes:

All room rates are per person per night including breakfast, 10% service charge, and consumption tax.

Application and Payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website.

The page will be opened in early June and reservations should be made by no later than September 9, 2008 (Japan time).

*Confirmation sheet will be sent by KNT after the application deadline.

Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment.

All payment must be paid only in Japanese yen by one of the following method.

1) Credit Card by Online
(VISA, MasterCard, American Express, Diners Club or JCB only.).
*Please fill in the necessary items in the credit card section of the application form.

2) Bank Transfer:
Sumitomo Mitsui Banking Corp.
Suzuran Branch
SWIFT Code: SMBCJPJT
Account Number: 6103515
Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation

In case of cancellation, a written notification should be sent to KNT to avoid any trouble.

The cancellation charge are:

Up to 14 days before the arrival date--------- No Charge
13 - 7 days before----------10 % of daily room charge
6 - 2 days before----------40 % of daily room charge
Less than 2 days, or no notice given-----100% of daily room charge

Refund

Refunds will be made during or after the conference after deducting bank and/or credit card service charges and the cancellation penalties.

If payment was made by credit card, refund will be made to the same credit card.

If the payment was made by bank transfer, please inform us of your bank account.

*Communication fee of 500 JPY is not refundable.

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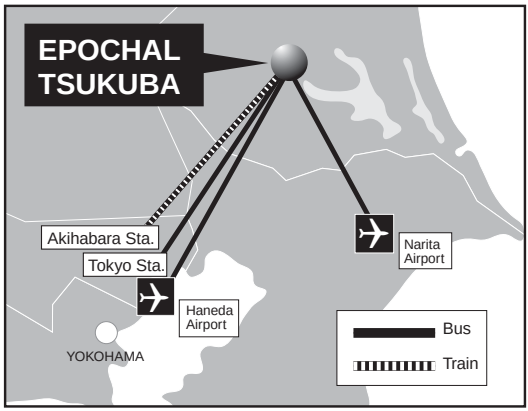

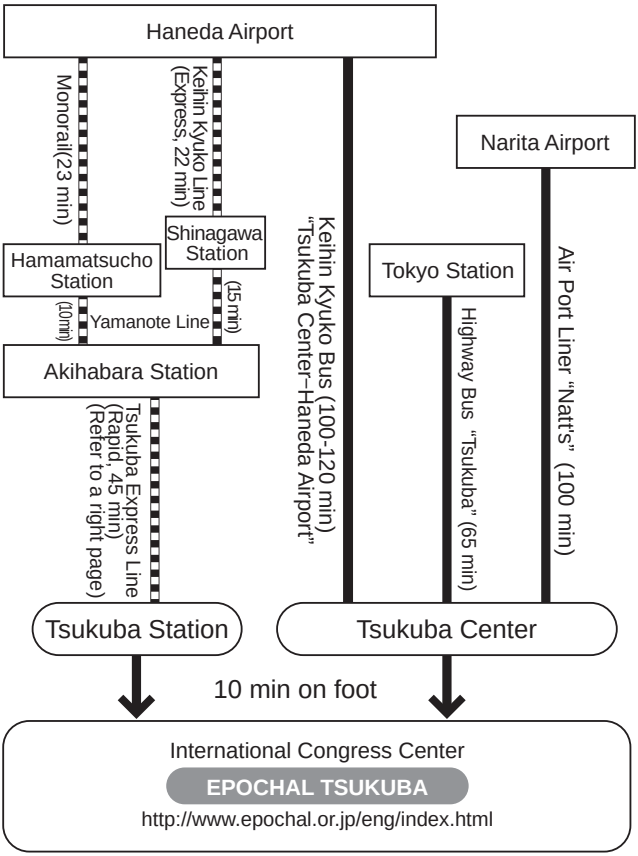

2008 International Conference on
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