Call for Papers

2007 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: September 19-21, 2007
Short Course (in Japanese): September 18, 2007

The 2007 International Conference on Solid State Devices and Materials (SSDM2007) will be held from September 19 to September 21, 2007 at Tsukuba International Congress Center (Tsukuba, Ibaraki, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. For the 2007 conference, 13 program subcommittees have been organized covering circuits and systems, as well as devices and materials. A one-day short course is also scheduled prior to the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM2007 is available online at:

http://www. ssdm.jp

PLENARY SESSIONS

Plenary Speakers:
"New Technology: Silicon Photonics:
Opportunity, Challenges & Applications"
M. Paniccia (Intel, USA)
"Organic Transistors: Towards Ambient Electronics"
T. Someya (The Univ. of Tokyo, Japan)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2007 conference, thirteen program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Gate Stack / Si Processing Science

(Chair: Y. Nara, Selete)

This subcommittee covers all the innovative front-end-of-line process technologies and sciences for advanced silicon-based LSI devices. Not only the gate stack technology but all the new concepts on Si-based front-end process technologies are welcome. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, and metal gate technologies, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow junction formation, novel diffusion/oxidation, and high-precision etching; (3) reliability physics and analysis; and (4) characterization and modeling of a Si process.

Invited Speakers:
"Schottky Barrier and Stability of Metal/high-k Interfaces: Theoretical View"
T. Nakayama (Chiba Univ., Japan)

"Study of Dopant Diffusion and Defect Evolution for Advanced Ultra Shallow Junctions based on an Atomistic Modeling"

T. Noda (Matsushita, IMEC, Belgium)

"Solutions and Challenges for High-k/Metal Gate CMOS"
J. Schaeffer (Freescale, USA)

"NBTI and PBTI in High k/ metal FETs"
S. Zafar (IBM, USA)

Area 2

Characterization and Materials Engineering for Interconnect Integration

(Chair: S. Ogawa, Selete)

Technologies and sciences that cover a Si back-end-of-line process are discussed, including package technology. Low-k materials have been in practical use; however, they brought new, difficult issues with decreasing in size, especially in reliability and package areas, and these areas require different ideas from conventional interconnect in characterization, material, and process/structure technologies. Papers are solicited in the following areas (but are not limited to these areas): (1) characterization methodology for materials, mechanical and electrical properties in small geometry, metrology and yield improvement; (2) materials and process technologies for advanced Cu/Low-k interconnect, including new dielectric and metal formation, planarization, and etching; (3) reliability phenomena and physics, such as EM, SIV, TDDB, and modeling/prediction; (4) Passive components for RF or High-speed operations; (5) packaging for Cu/Low-k chips; (6) new concepts and materials for future interconnects, such as a 3-D structure, a CNT interconnect, and wireless applications. *A special session focused on advanced Cu/Low-k technologies is scheduled to highlight this area through unit processes, characterization, up to reliability.*

Invited speakers will be informed.

Area 3

CMOS Devices / Device Physics

(Chair: K. Shibahara, Hiroshima Univ.)

The aim of this area is to discuss advanced silicon device technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel and SiGe and Ge channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, and double gate FET; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science.

Invited Speakers:

"Progress in Technology Oriented Analytical Modeling of Advanced Quasi Ballistic Ultra Thin Body MOSFETs"

R. Clerc (IMEP, France)

"LSTP/LOP CMOS Process Integration Scheme for 45-32 nm node"

K. Imai (NEC, Japan)

"Impact of RTS on V_{th} Fluctuation (tentative)"

A. S. Spinelli (Politecnico di Milano, Italy)

Area 4

Advanced Memory Technology

(Chair: A. Nitayama, Toshiba)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward ''high speed and high density, broadband and mobile.'' Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited Speakers:
"Current Development Status and Future Challenge of Transition Metal Oxide ReRAM Technologies"
N. Awaya (Sharp, Japan)
"Current Development Status and Future Challenge of 3D Stacked NAND Flash Technologies"
S. M. Jung (Samsung Electronics, Korea)
"Status and Future Challenge of Manufacturable PRAM Technologies"
Y. Matsui (Hitachi, Japan)
"Overview and Future Challenge of Floating Body Cell Technologies"
T. Shino (Toshiba, Japan)

Area 5

Advanced Circuits and Systems

(Chair: H. Kobayashi, Gunma Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following: (1) advanced digital, analog, mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication circuits; (4) power devices and circuits as well as power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); and (7) LSI testing technology; (8) three dimensional IC technology; (9) MEMS (passive) devices as well as circuits, RF MEMS; (10) sensor devices and circuits; (11) thin film transistors and circuits; (12) organic transistors and circuits. A special session focused on RF CMOS devices and circuits is scheduled to highlight this area.

Invited Speakers:
"Accurate Process Sensitivity Models based DFM Flows"
C. Guardiani (PDF Solutions, Italy)
"History of DLP Technology"
P. V. Kessel (Texas Instruments, USA)
"Error Correction and Calibration Technology for RF Circuits and Systems"
A. Matsuzawa (Tokyo Tech., Japan)
"RF CMOS Modeling"
T. Ooguro (Toshiba, Japan)
"RF CMOS Circuits –Overview and Perspective–"
T. Tsukahara (Aizu Univ., Japan)

Area 6

Compound Semiconductor Circuits, Electron Devices and Device Physics

(Chair: M. Kuzuhara, Univ. of Fukui)

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, and other materials. Papers are solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures; (2) high-voltage or high-temperature electron devices and circuits; (3) microwave and millimeter-wave amplifiers, oscillators, switches, and other ICs; (4) high-speed digital ICs and mixed-signal ICs; (5) theory and physics of electron devices; (6) characterization techniques for devices and ICs; (7) innovative device processing and packaging; (8) reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited Speakers:

"Next Generation High-Efficiency RF Transmitter Technology for Basestations"

P. M. Asbeck (UCSD, USA)

"Growth of InAs Channel HEMT Structure on Si Substrate and its Possible Application for Low Power Logic"

E. Y. Chang (National Chiao Tung Univ., Taiwan)

"Microwave Class-F Power Amplifiers Using GaN HEMTs"

K. Honjo (Univ. of Electro-Communications, Japan)

"Parasitic Effects and Reliability Issues on GaN based HEMTs"

G. Meneghesso (Univ. of Padova, Italy)

"GaN HEMT Transistors and MMICs: Technology Status and Applications"

P. Parikh (Cree Santa Barbara, USA)

Area 7

Photonic Devices and Device Physics

(Chair: M. Sugawara, Fujitsu Labs.)

The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs,

photodetectors, SOAs, and OEICs; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic crystal materials and novel functional devices; (4) optical switches, modulators, and MEMS; (5) optical wavelength converters, nonlinear optical devices, and all-optical switches; (6) waveguide components, PLCs and integrated photonic circuits; (7) material and device processing and characterization techniques; (8) hybrid and monolithic integration, packaging and moduling; (9) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (10) linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (11) novel phenomena and applications including slow light, fast light, optical memory, and optoelectronic tweezers, *A special session focused on "Photonic crystals and Si nano-photonics" is scheduled to highlight this area through their concept, design, fabrication processes, and devices.*

Invited Speakers:
"High-speed Quantum-dot Lasers"
P. Bhattacharya (Univ. of Michigan, USA)
"GaN-based High-speed Intersubband Optical Switches"
N. Iizuka and N. Suzuki (Toshiba, Japan)
"MOCVD Growth of Quantum-dot Optical Devices"
K. Kawaguchi (Fujitsu Labs., Japan)
"Quantum Confined Ultra-Thin Silicon Light-Emitting Transistor for On-Chip Optical Interconnection"
S. Saito (Hitachi, Japan)
"Nanophotonic Technologies for PC-SMZ-based All-optical Flip-flop Switch : PC-FF"
Y. Sugimoto[1,2] and K. Asakawa[2]
([1]NIMS, [2]Univ. of Tsukuba, Japan)
"High-speed Wavelength Tunable Lasers"
S. Tsuji (Hitachi, Japan)
Further invited speakers will be added.

Area 8

Advanced Material Synthesis and Crystal Growth Technology

(Chair: H. Yamaguchi, NTT)

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and

structures, nitride compounds, carbon nanotubes, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) nitride-related compound semiconductors; (3) novel synthesis, growth, and fabrication techniques; (4) carbon nanotubes; (5) nanowires and nanoparticles; (6) microscale and nanoscale 3-D structures; (7) characterization of fundamental properties.

Invited Speakers:
"InAs/In(Ga,Al)AsSb Quantum Dot Heterostructures for Photonic Devices"
J. -I. Chyi (NCU, Taiwan)
"Present Status and Future Issues of III-V Semiconductor Nanowires"
K. Hiruma (ASET, Japan)
"Bottom-up Approach for the Nanopatterning of Si(001)"
R. Koch (Johannes Kepler Univ., Austria)
"In Situ X-ray Diffraction during Semiconductor Nanostructure Growth"
M. Takahashi (Japan Atomic Energy Agency, Japan)

Area 9

Physics and Applications of Novel Functional Materials and Devices

(Chair: Y. Takahashi, Hokkaido Univ.)

This session covers applications and physics of novel functional devices and quantum nanostructures that are made mainly by using nanofabrication technology or selforganized phenomena. Papers are solicited in the following areas (but are not limited to these areas): (1) quantum phenomena in nanostructures; (2) quantum dots and single-electron devices; (3) solid-state quantum computing and communications; (4) nanometer-scale characterization, such as SPM and SNOM; (5) other novel devices, such as small superconducting devices, and resonant tunneling devices in nanoscale.

Invited Speakers:
"Nanopatterned Epitaxial Graphene for Nanoelectronics"
W. A. de Heer (Georgia Inst. of Tech., USA)

"CMOS Integration on 3D Nanowires Matrix for VLSI Applications"

T. Ernst (CEA-LETI, France)

"Scanning Gate Measurements at Millikelvin Temperatures: Exceptional Views on Nanostructures"

T. Ihn (ETH Zürich, Switzerland)

Further invited speakers will be added.

Area 10

Organic Materials Science, Device Physics, and Applications

(Chair: T. Kamata, AIST)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors and circuits; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9) interfacial phenomena, LC devices, etc.

Invited Speakers:

"Design of Organic Transistors"

K. Kudo (Chiba Univ., Japan)

"Molecular Device"

T. Lee (GIST, Korea)

"Plastic Dye-sensitized Solar Cells and Solidification with Nano-carbon Materials"

T. Miyasaka (Toin Univ. of Yokohama, Japan)

"Printed Organic TFT for Displays"

R. Street (Xerox, USA)

Area 11

Micro / Nano Electromechanical and Bio-Systems (Devices)

(Chair: H. Tabata, Univ. of Tokyo)

This session focuses on micro/nano electromechanical systems(MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices and bio-sensors are widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and

technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems (M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications.

Invited Speakers:
"Microelectronics for Bio Sensor"
S. Banerjee (Univ. of Texas at Austin, USA)
"Fabrication of 3-dimensional Structure by Nanoimprint Process"
Y. Hirai (Osaka Prefecture Univ., Japan)
"To be announced"
T. Urisu (Inst. of Molecular Science, Japan)
Further invited speakers will be added.

Area 12

Spintronic Materials and Devices

(Chair: M. Tanaka, Univ. of Tokyo)

This field covers spintronic materials (metals, semiconductors, insulators, hybrid structures, and nanostructures), spin-related phenomena, and device applications. Papers are solicited in the following areas (but are not limited to these areas): (1) ferromagnetic and/or half-metallic materials; (2) hybrid structures and nanostructures in which spin effects are apparent and important; (3) spin-dependent optical and transport phenomena; (4) spin dynamics; (5) spintronics devices and systems including magnetic tunnel junctions and TMR devices, nonvolatile memory, magnetic sensors, spin-transistors, optical isolators, optical switches etc; (6) quantum information processing using spin states.

Invited Speakers:
"Spin Transfer Switching in MTJs for MRAM"
Y. Huai (Grandis Inc., USA)
"Giant TMR in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions" (tentative)
S. Ikeda (Tohoku Univ., Japan)

"Giant TMR and Future Nonvolatile Memory"
S. S. P. Parkin (IBM Almaden, USA)
"Structural Study on CoFeB/MgO/CoFeB Magnetic Tunnel Junctions"
K. Tsunekawa (Canon ANELVA, Japan)
Further invited speakers will be added.

Area 13

Applications of Nanotubes and Nanowires

(Chair: K. Matsumoto, Osaka Univ.)

All kinds of applications using nanotubes & nanowires are included in the scope of this sub-committee. Nanotubes & nanowires, e.g., carbon nanotube, BN nanotube, Si nanowire, compound semiconductor nanowire, layered nanowire, etc. are all included. Applications using nanotubes & nanowires in the scope are as follows: (1) active electronic and optical devices, e.g., FET, HEMT, optical transistor, optical switch, and quantum devices including single electron transistor (SET), SET logics, resonant tunneling devices, quantum computing devices and so on; (2) all kinds of sensors, e.g., bio sensors, gas sensors, pressure sensors, acceleration sensors and so on; (3) application for passive elements, e.g., wiring & via technology for future LSI and so on; (4) nanomechanical application, e.g., probe applications for STM/AFM, tweezers, motors, oscillators and so on; (5) fundamental research related to those applications of nanotube & nanowire, e.g., new growth technology, analysis of growth mechanism, new device fabrication process and so on; (6) new evaluation technology, e.g., TEM, SEM, Raman scattering, photo luminescence and so on; (7) theoretical analysis of device physics, new physics in the nanotube & nanowire, e.g., Tomonaga liquid, one dimensional quantum transport and so on.

Invited Speakers:
"Nanowires for Nanoscale Electronics, Biosensors and Energy Applications"
Y. Cui (Stanford Univ., USA)
"Semiconductor Nanowires and their Application to Nanodevices"
T. Fukui (Hokkaido Univ., Japan)
"To be announced"
A. Keshavarzi (Intel, USA)
"Advances in Carbon Nanotube Devices and Circuits"
Y. M. Lin (IBM, USA)
Further invited speakers will be added.