

Call for Papers

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INTERNATIONAL CONFERENCE ON

SOLID STATE
DEVICES AND MATERIALS

**2007 International Conference
on Solid State Devices and Materials (SSDM 2007)**

SECRETARIAT

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Conference **September 19-21, 2007**

Short Course **September 18, 2007**

Place **Tsukuba International Congress Center
(EPOCHAL TSUKUBA)
(TSUKUBA, Ibaraki, Japan)**

Paper Deadline **May 10, 2007**

Online submission through the conference website
is available from the end of March.

Late News Paper Deadline **July 30, 2007**

**Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS**

**Technical-Cosponsored by
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The Institute of Image Information and Television Engineers

Japan Institute of Electronics Packaging



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Web Site : <http://www.ssdm.jp>

Call for Papers

2007 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: September 19-21, 2007
Short Course (in Japanese): September 18, 2007

The 2007 International Conference on Solid State Devices and Materials (SSDM2007) will be held from September 19 to September 21, 2007 at Tsukuba International Congress Center (Tsukuba, Ibaraki, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. For the 2007 conference, 13 program subcommittees have been organized covering circuits and systems, as well as devices and materials. A one-day short course is also scheduled prior to the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM2007 is available online at:

<http://www.ssdm.jp>

PLENARY SESSIONS

Plenary Speakers:

“New Technology: Silicon Photonics:
Opportunity, Challenges & Applications”

M. Paniccia (Intel, USA)

“Organic Transistors: Towards Ambient Electronics”

T. Someya (The Univ. of Tokyo, Japan)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2007 conference, thirteen program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Gate Stack / Si Processing Science

(Chair: Y. Nara, Selete)

This subcommittee covers all the innovative front-end-of-line process technologies and sciences for advanced silicon-based LSI devices. Not only the gate stack technology but all the new concepts on Si-based front-end process technologies are welcome. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, and metal gate technologies, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow junction formation, novel diffusion/oxidation, and high-precision etching; (3) reliability physics and analysis; and (4) characterization and modeling of a Si process.

Invited Speakers:

“Schottky Barrier and Stability of Metal/high-k Interfaces:
Theoretical View”

T. Nakayama (Chiba Univ., Japan)

“Study of Dopant Diffusion and Defect Evolution for Advanced Ultra Shallow Junctions based on an Atomistic Modeling”

T. Noda (Matsushita, IMEC, Belgium)

“Solutions and Challenges for High-k/Metal Gate CMOS”

J. Schaeffer (Freescale, USA)

“NBTI and PBTI in High k/ metal FETs”

S. Zafar (IBM, USA)

Area 2

Characterization and Materials Engineering for Interconnect Integration

(Chair: S. Ogawa, Selete)

Technologies and sciences that cover a Si back-end-of-line process are discussed, including package technology. Low-k materials have been in practical use; however, they brought new, difficult issues with decreasing in size, especially in reliability and package areas, and these areas require different ideas from conventional interconnect in characterization, material, and process/structure technologies. Papers are solicited in the following areas (but are not limited to these areas): (1) characterization methodology for materials, mechanical and electrical properties in small geometry, metrology and yield improvement; (2) materials and process technologies for advanced Cu/Low-k interconnect, including new dielectric and metal formation, planarization, and etching; (3) reliability phenomena and physics, such as EM, SIV, TDDB, and modeling/prediction; (4) Passive components for RF or High-speed operations; (5) packaging for Cu/Low-k chips; (6) new concepts and materials for future interconnects, such as a 3-D structure, a CNT interconnect, and wireless applications. *A special session focused on advanced Cu/Low-k technologies is scheduled to highlight this area through unit processes, characterization, up to reliability.*

Invited speakers will be informed.

Area 3

CMOS Devices / Device Physics

(Chair: K. Shibahara, Hiroshima Univ.)

The aim of this area is to discuss advanced silicon device technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel and SiGe and Ge channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, and double gate FET; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science.

Invited Speakers:

“Progress in Technology Oriented Analytical Modeling of Advanced Quasi Ballistic Ultra Thin Body MOSFETs”

R. Clerc (IMEP, France)

“LSTP/LOP CMOS Process Integration Scheme for 45-32 nm node”

K. Imai (NEC, Japan)

“Impact of RTS on V_{th} Fluctuation (tentative)”

A. S. Spinelli (Politecnico di Milano, Italy)

Area 4

Advanced Memory Technology

(Chair: A. Nitayama, Toshiba)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward “high speed and high density, broadband and mobile.” Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited Speakers:

“Current Development Status and Future Challenge of Transition Metal Oxide ReRAM Technologies”

N. Awaya (Sharp, Japan)

“Current Development Status and Future Challenge of 3D Stacked NAND Flash Technologies”

S. M. Jung (Samsung Electronics, Korea)

“Status and Future Challenge of Manufacturable PRAM Technologies”

Y. Matsui (Hitachi, Japan)

“Overview and Future Challenge of Floating Body Cell Technologies”

T. Shino (Toshiba, Japan)

Area 5

Advanced Circuits and Systems

(Chair: H. Kobayashi, Gunma Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following: (1) advanced digital, analog, mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication circuits; (4) power devices and circuits as well as power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); and (7) LSI testing technology; (8) three dimensional IC technology; (9) MEMS (passive) devices as well as circuits, RF MEMS; (10) sensor devices and circuits; (11) thin film transistors and circuits; (12) organic transistors and circuits. A special session focused on RF CMOS devices and circuits is scheduled to highlight this area.

Invited Speakers:

“Accurate Process Sensitivity Models based DFM Flows”

C. Guardiani (PDF Solutions, Italy)

“History of DLP Technology”

P. V. Kessel (Texas Instruments, USA)

“Error Correction and Calibration Technology for RF Circuits and Systems”

A. Matsuzawa (Tokyo Tech., Japan)

“RF CMOS Modeling”

T. Ooguro (Toshiba, Japan)

“RF CMOS Circuits –Overview and Perspective–”

T. Tsukahara (Aizu Univ., Japan)

Area 6

Compound Semiconductor Circuits, Electron Devices and Device Physics

(Chair: M. Kuzuhara, Univ. of Fukui)

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, and other materials. Papers are solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures; (2) high-voltage or high-temperature electron devices and circuits; (3) microwave and millimeter-wave amplifiers, oscillators, switches, and other ICs; (4) high-speed digital ICs and mixed-signal ICs; (5) theory and physics of electron devices; (6) characterization techniques for devices and ICs; (7) innovative device processing and packaging; (8) reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited Speakers:

“Next Generation High-Efficiency RF Transmitter Technology for Basestations”

P. M. Asbeck (UCSD, USA)

“Growth of InAs Channel HEMT Structure on Si Substrate and its Possible Application for Low Power Logic”

E. Y. Chang (National Chiao Tung Univ., Taiwan)

“Microwave Class-F Power Amplifiers Using GaN HEMTs”

K. Honjo (Univ. of Electro-Communications, Japan)

“Parasitic Effects and Reliability Issues on GaN based HEMTs”

G. Meneghesso (Univ. of Padova, Italy)

“GaN HEMT Transistors and MMICs: Technology Status and Applications”

P. Parikh (Cree Santa Barbara, USA)

Area 7

Photonic Devices and Device Physics

(Chair: M. Sugawara, Fujitsu Labs.)

The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs,

photodetectors, SOAs, and OEICs; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic crystal materials and novel functional devices; (4) optical switches, modulators, and MEMS; (5) optical wavelength converters, nonlinear optical devices, and all-optical switches; (6) waveguide components, PLCs and integrated photonic circuits; (7) material and device processing and characterization techniques; (8) hybrid and monolithic integration, packaging and moduling; (9) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (10) linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (11) novel phenomena and applications including slow light, fast light, optical memory, and optoelectronic tweezers, *A special session focused on "Photonic crystals and Si nano-photonics" is scheduled to highlight this area through their concept, design, fabrication processes, and devices.*

Invited Speakers:

“High-speed Quantum-dot Lasers”

P. Bhattacharya (Univ. of Michigan, USA)

“GaN-based High-speed Intersubband Optical Switches”

N. Iizuka and N. Suzuki (Toshiba, Japan)

“MOCVD Growth of Quantum-dot Optical Devices”

K. Kawaguchi (Fujitsu Labs., Japan)

“Quantum Confined Ultra-Thin Silicon Light-Emitting Transistor for On-Chip Optical Interconnection”

S. Saito (Hitachi, Japan)

“Nanophotonic Technologies for PC-SMZ-based All-optical Flip-flop Switch : PC-FF”

Y. Sugimoto^{1,2} and K. Asakawa²
(¹NIMS, ²Univ. of Tsukuba, Japan)

“High-speed Wavelength Tunable Lasers”

S. Tsuji (Hitachi, Japan)

Further invited speakers will be added.

Area 8

Advanced Material Synthesis and Crystal Growth Technology

(Chair: H. Yamaguchi, NTT)

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and

structures, nitride compounds, carbon nanotubes, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) nitride-related compound semiconductors; (3) novel synthesis, growth, and fabrication techniques; (4) carbon nanotubes; (5) nanowires and nanoparticles; (6) microscale and nanoscale 3-D structures; (7) characterization of fundamental properties.

Invited Speakers:

“InAs/In(Ga,Al)AsSb Quantum Dot Heterostructures for Photonic Devices”

J. -I. Chyi (NCU, Taiwan)

“Present Status and Future Issues of III-V Semiconductor Nanowires”

K. Hiruma (ASET, Japan)

“Bottom-up Approach for the Nanopatterning of Si(001)”

R. Koch (Johannes Kepler Univ., Austria)

“In Situ X-ray Diffraction during Semiconductor Nanostructure Growth”

M. Takahashi (Japan Atomic Energy Agency, Japan)

Area 9

Physics and Applications of Novel Functional Materials and Devices

(Chair: Y. Takahashi, Hokkaido Univ.)

This session covers applications and physics of novel functional devices and quantum nanostructures that are made mainly by using nanofabrication technology or selforganized phenomena. Papers are solicited in the following areas (but are not limited to these areas): (1) quantum phenomena in nanostructures; (2) quantum dots and single-electron devices; (3) solid-state quantum computing and communications; (4) nanometer-scale characterization, such as SPM and SNOM; (5) other novel devices, such as small superconducting devices, and resonant tunneling devices in nanoscale.

Invited Speakers:

“Nanopatterned Epitaxial Graphene for Nanoelectronics”

W. A. de Heer (Georgia Inst. of Tech., USA)

“CMOS Integration on 3D Nanowires Matrix for VLSI Applications”

T. Ernst (CEA-LETI, France)

“Scanning Gate Measurements at Millikelvin Temperatures: Exceptional Views on Nanostructures”

T. Ihn (ETH Zürich, Switzerland)

Further invited speakers will be added.

Area 10

Organic Materials Science, Device Physics, and Applications

(Chair: T. Kamata, AIST)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors and circuits; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9) interfacial phenomena, LC devices, etc.

Invited Speakers:

“Design of Organic Transistors”

K. Kudo (Chiba Univ., Japan)

“Molecular Device”

T. Lee (GIST, Korea)

“Plastic Dye-sensitized Solar Cells and Solidification with Nano-carbon Materials”

T. Miyasaka (Toin Univ. of Yokohama, Japan)

“Printed Organic TFT for Displays”

R. Street (Xerox, USA)

Area 11

Micro / Nano Electromechanical and Bio-Systems (Devices)

(Chair: H. Tabata, Univ. of Tokyo)

This session focuses on micro/nano electromechanical systems (MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices and bio-sensors are widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and

technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems (M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications.

Invited Speakers:

“Microelectronics for Bio Sensor”

S. Banerjee (Univ. of Texas at Austin, USA)

“Fabrication of 3-dimensional Structure by Nanoimprint Process”

Y. Hirai (Osaka Prefecture Univ., Japan)

“To be announced”

T. Urisu (Inst. of Molecular Science, Japan)

Further invited speakers will be added.

Area 12

Spintronic Materials and Devices

(Chair: M. Tanaka, Univ. of Tokyo)

This field covers spintronic materials (metals, semiconductors, insulators, hybrid structures, and nanostructures), spin-related phenomena, and device applications. Papers are solicited in the following areas (but are not limited to these areas): (1) ferromagnetic and/or half-metallic materials; (2) hybrid structures and nanostructures in which spin effects are apparent and important; (3) spin-dependent optical and transport phenomena; (4) spin dynamics; (5) spintronics devices and systems including magnetic tunnel junctions and TMR devices, nonvolatile memory, magnetic sensors, spin-transistors, optical isolators, optical switches etc; (6) quantum information processing using spin states.

Invited Speakers:

“Spin Transfer Switching in MTJs for MRAM”

Y. Huai (Grandis Inc., USA)

“Giant TMR in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions” (tentative)

S. Ikeda (Tohoku Univ., Japan)

“Giant TMR and Future Nonvolatile Memory”

S. S. P. Parkin (IBM Almaden, USA)

“Structural Study on CoFeB/MgO/CoFeB Magnetic Tunnel Junctions”

K. Tsunekawa (Canon ANELVA, Japan)

Further invited speakers will be added.

Area 13

Applications of Nanotubes and Nanowires

(Chair: K. Matsumoto, Osaka Univ.)

All kinds of applications using nanotubes & nanowires are included in the scope of this sub-committee. Nanotubes & nanowires, e.g., carbon nanotube, BN nanotube, Si nanowire, compound semiconductor nanowire, layered nanowire, etc. are all included. Applications using nanotubes & nanowires in the scope are as follows: (1) active electronic and optical devices, e.g., FET, HEMT, optical transistor, optical switch, and quantum devices including single electron transistor (SET), SET logics, resonant tunneling devices, quantum computing devices and so on; (2) all kinds of sensors, e.g., bio sensors, gas sensors, pressure sensors, acceleration sensors and so on; (3) application for passive elements, e.g., wiring & via technology for future LSI and so on; (4) nanomechanical application, e.g., probe applications for STM/AFM, tweezers, motors, oscillators and so on; (5) fundamental research related to those applications of nanotube & nanowire, e.g., new growth technology, analysis of growth mechanism, new device fabrication process and so on; (6) new evaluation technology, e.g., TEM, SEM, Raman scattering, photo luminescence and so on; (7) theoretical analysis of device physics, new physics in the nanotube & nanowire, e.g., Tomonaga liquid, one dimensional quantum transport and so on.

Invited Speakers:

“Nanowires for Nanoscale Electronics, Biosensors and Energy Applications”

Y. Cui (Stanford Univ., USA)

“Semiconductor Nanowires and their Application to Nanodevices”

T. Fukui (Hokkaido Univ., Japan)

“To be announced”

A. Keshavarzi (Intel, USA)

“Advances in Carbon Nanotube Devices and Circuits”

Y. M. Lin (IBM, USA)

Further invited speakers will be added.

RUMP SESSIONS

Following two Rump Sessions have been organized on September 20 (Thursday).

Session A

“Oxide Electronics–Status and Outlook–”

Organizer/Moderator:

M. Kawasaki (Tohoku Univ., Japan)

Increasing interests on oxides are attracted by the rich possibilities and keen demands of metal-oxides as the key materials for future electronics. High-k oxides for alternative gate dielectrics and ferroelectric capacitors for non-volatile memories are well known examples for the SSDM community. Even more exciting applications are now being uncovered, from ultraviolet light emitting devices and high mobility thin film transistors through electric-control of magnetism in multiferroics to resistance change nonvolatile memories. Several keynotes will be delivered for the latter by panelists and near-future challenges in the emerging materials research will be discussed with the audience.

Session B

“New Materials Meet Advanced Silicon Technology”
(tentative)

Organizers/Moderators:

H. Ishiuchi (Toshiba, Japan)
and a couple of additional Organizers/
Moderators

SHORT COURSE

Short Course entitled “Emerging Silicon Technology” will be held on Tuesday, September 18. All lectures are given in Japanese.

SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at <http://www.ssdm.jp>.

Please note that submissions by post will NOT be accepted.

<p><i>Deadline for Submission is 24:00, May 10, 2007(Japan time).</i></p>

The two-page paper must be prepared in English in 8.5-×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean, etc. fonts cannot be used for either figures or texts. The paper should report original, previously unpublished work, including specific results. Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

POSTER SESSIONS

Some of the papers will be presented in the Poster Session. All authors of poster presentations are requested to give short (2 minutes) presentations.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed, without opportunity for further revision, in the extended abstracts which will be distributed to conference participants during the conference.

SPECIAL ISSUE in JJAP

Authors of papers accepted for presentation at SSDM 2007 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2008.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

<p><i>Late News Papers Deadline is 24:00, July 30, 2007 (Japan time).</i></p>

Notices of acceptance will be e-mailed by mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include plenary sessions, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

AWARDS

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 2001.

SSDM Paper Award

Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.

An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF).

BANQUET

The conference banquet will be held on the evening of Wednesday, September 19. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

REGISTRATION

Participants are required to register online at the conference web site <http://www.ssdm.jp>, in which the forms for registration, short course and banquet will be available in the beginning of June, 2007.

The registration and banquet fees are:

	Registration Fee		Short Course (in Japanese)	Banquet
	Before 13:00, Aug. 13 (Japan time)	After 13:00, Aug. 13 (Japan time)		
Regular	¥45,000	¥50,000	¥15,000	¥7,000
Student	¥7,000		¥3,000	¥4,000
Accompanied person				¥4,000

* Fees include tax.

VISA REQUIREMENT

Overseas participants who require a visa should consult the nearest Japanese Embassy. Please note that obtaining a visa may take much longer than you anticipate, and we strongly recommend that you commence the application process as soon as possible. If your visa application requires an invitation to attend the SSDM conference, please contact SSDM Secretariat, ssdm@intergroup.co.jp.

LOCATION

SSDM2007 will be held at Tsukuba International Congress Center (EPOCHAL TSUKUBA).

2-20-3 Takezono, Tsukuba, Ibaraki

305-0032, Japan

Phone: +81-29-861-0001

Fax: +81-29-861-1209

Tsukuba International Congress Center has been contributing greatly to the continued development of science and technology, standing as the kernel place for such exchange, where people nearly 2 million have gathered since it was established in 1999. Just 50 km from Tokyo and 40 km from Narita Airport, the congress center is located in Tsukuba, the center of advanced technology, research and development, and the pre-eminent location for conventions.

<http://www.epochal.or.jp/index.html>

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho, Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2007-gb@or.knt.co.jp

Hotel Accommodations

KNT has blocked rooms at following hotels in Tsukuba for the conference period.

Reservations can be made through the conference website beginning in June.

If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

Hotel Name	Okura Frontier Hotel Tsukuba
Room Rates	Single: ¥11,550 Twin: ¥10,500 (per person, per night)
Hotel Deposit	¥20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-1364-1, Azuma Tsukuba-city, Ibaraki 305-0031, Japan
Phone	+81-29-852-1112
Access to Hotel	2 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	6 min. walk

Hotel Name	Okura Frontier Hotel Tsukuba Epochal
Room Rates	Single: ¥11,550 Twin: ¥10,500 (per person, per night)
Hotel Deposit	¥20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	2-20-1 Takezono, Tsukuba-city, Ibaraki 305-0032, Japan
Phone	+81-29-860-7700
Access to Hotel	8 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	Next to the site

Hotel Name	Hotel Grand Shinonome
Room Rates	Single: ¥7,500
Hotel Deposit	¥10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	488-1 Onozaki, Tsukuba-city, Ibaraki 305-0034, Japan
Phone	+81-29-856-2211
Access to Hotel	5 min. walk from Tsukuba Sta.
To Conference site	13 min. walk

Hotel Name	Hotel Route Tsukuba
Room Rates	Single: ¥6,825
Hotel Deposit	¥10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	1145-3 Hanamuro, Tsukuba-city, Ibaraki 305-0025, Japan
Phone	+81-29-860-2111
Access to Hotel	20 min. walk (or 5 min. by taxi) from Tsukuba Sta.
To Conference site	30 min. walk (or 10 min. by taxi)

Hotel Name	Tsukuba Daily Inn
Room Rates	Single: ¥6,930
Hotel Deposit	¥10,000
Check-in/out	Check-in:16:00/Check-out:10:00
Address	1-12-4 Sengen, Tsukuba-city, Ibaraki 305-0047, Japan
Phone	+81-29-851-0003
Access to Hotel	30 min. walk (or 7 min. by taxi) from Tsukuba Sta.
To Conference site	15 min. walk (or 3 min. by taxi)

Hotel Name	Akihabara Washington Hotel
Room Rates	Single: ¥11,550 Twin: ¥8,925 (per person, per night)
Hotel Deposit	¥20,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-8-3 Sakumacho, Kanda, Chiyoda-ku, Tokyo 101-0025, Japan
Phone	+81-3-3255-3311
Access to Hotel	1 min. walk from Tsukuba Express (JR) Akihabara Sta.
To Conference site	45 min. by Tsukuba Express (JR) and 8 min. walk

Hotel Name	Asakusa View Hotel
Room Rates	Single: ¥15,693
Hotel Deposit	¥20,000
Check-in/out	Check-in:13:00/Check-out:11:00
Address	3-17-1 Nishi-Asakusa, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1111
Access to Hotel	1 min. walk from Tsukuba Express (JR) Asakusa Sta.
To Conference site	40 min. by Tsukuba Express (JR) and 8 min. walk

Hotel Name	Hotel Sunroute Asakusa
Room Rates	Single: ¥9,500
Hotel Deposit	¥10,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-8-5 Kaminarimon, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1511
Access to Hotel	5 min. walk from Tsukuba Express (JR) Asakusa Sta.
To Conference site	40 min. by Tsukuba Express (JR) and 8 min. walk

Hotel Name	Tsukuba Kenshu Center
Room Rates	Single: ¥4,900/*¥400 for each breakfast
Hotel Deposit	The payment in full for your room charge
Check-in/out	Check-in:16:00(no later than 23:00)/Check-out:10:00
Address	1-13-5 Amakubo, Tsukuba-city, Ibaraki 305-0005, Japan
Phone	+81-29-851-5152
Access to Hotel	5 min. by bus and 5 min. walk from Tsukuba Sta.
To Conference site	5 min. walk and 10 min. by bus

Note: All room rates are per person per night, including breakfast, 10% service charge and 5% consumption tax.

* It is excluding breakfast in Tsukuba Kenshu Center.

More information for Tsukuba Kenshu Center, please contact KNT.

Application and payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website.

The page will be opened in early June and reservations should be made by no later than August 18, 2007 (Japan time).

* Confirmation sheet will be sent by KNT after the application deadline.

Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment.

All payment must be paid only in Japanese yen by one of the following methods:

1) Credit Card

(VISA, MasterCard, Diners Club, AMEX or JCB only)

* Please fill in the necessary items with your signature in the credit card section of the application form.

2) Bank Transfer

Sumitomo Mitsui Banking Corp.

Suzuran Branch

SWIFT Code: SMBCJPJT

Account Number: 6103515

Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation

In case of cancellation, a written notification should be sent to KNT to avoid any trouble.

The cancellation charges are:

Up to 14 days before the arrival dateNo Charge

13–7 days before10 % of daily room charge

6–2 days before40 % of daily room charge

Less than 2 days, or no notice given

.....100 % of daily room charge

Refund

Refunds will be made during or after the conference after deducting bank and/or credit card service charges and the cancellation penalties.

If payment was made by credit card, refund will be made to the same credit card.

If the payment was made by bank transfer, please inform us of your bank account.

* Communication fee of 500 JPY is not refundable.

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