2007 International Conference on Solid State Devices and Materials (SSDM 2007)

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ADVANCE PROGRAM

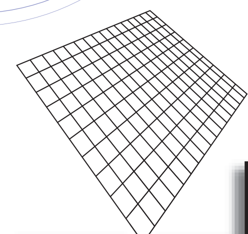
2007 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference September 19-21, 2007

Short Course September 18, 2007

Place Tsukuba International Congress Center (Tsukuba, Ibaraki, Japan)

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS
Technical-Cosponsored by
IEEE Electron Devices Society
in cooperation with
The Electrochemical Society of Japan
IEEE EDS Japan Chapter
IEEE Japan Council
The Institute of Electrical Engineers of Japan
The Institute of Electronics, Information and Communication Engineers
The Institute of Image Information and Television Engineers
Japan Institute of Electronics Packaging



Web Site : http://www.ssdm.jp

SSDM 2007 Time Table

Wednesday, September 19

Main Convention Hall

10:00-12:30 PL: Opening Session/SSDM Award

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
14:00-15:50 **Area 1: Advanced Gate Stack /Si Processing Science** A-1: Metal Gate-I	**14:00-16:00** **Area 3: CMOS Devices/Device Physics** B-1: Ge, SiGe Channel Transistor Technology	**14:00-15:50** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-1: Novel Interconnects	**14:00-15:50** **Area 5: Advanced Circuits and Systems** D-1: Scaling and Circuit Design Concern	**14:00-16:00** **Area 7: Photonic Devices and Device Physics** E-1: Quantum-Dot Devices	**14:00-16:00** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-1: Compound Semiconductors	**14:00-16:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-1: GaN FETs I	**14:00-16:00** **Area 10: Organic Materials Science, Device Physics, and Applications** H-1: Organic Photo-Electronics	**14:00-16:00** **Area 9: Physics and Applications of Novel Functional Materials and Devices** I-1: Novel Si Transistors	**14:00-15:50** **Area 4: Advanced Memory Technology** J-1: DRAM I	
16:15-18:15 **Area 1: Advanced Gate Stack /Si Processing Science** A-2: Ge MIS	**16:15-18:25** **Area 3: CMOS Devices/Device Physics** B-2: Transport in Nanoscale MOSFETs	**16:15-17:30** **Area 12: Spintronic Materials and Devices** C-2: Spintronic Materials and Quantum Structures	**16:15-18:15** **Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)** D-2: MEMS Technology	**16:15-18:15** **Area 7: Photonic Devices and Device Physics** E-2: Special Session: Photonic Crystals and Si Photonics I	**16:15-17:30** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-2: Oxides	**16:15-18:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-2: GaN FETs II	**16:15-18:00** **Area 10: Organic Materials Science, Device Physics, and Applications** H-2: Organic Light Emitting Devices	**16:15-18:00** **Area 9: Physics and Applications of Novel Functional Materials and Devices** I-2: Transport Through Novel Materials and Structures	**16:15-17:45** **Area 4: Advanced Memory Technology** J-2: Flash Memory I	

18:30-20:30 Banquet/Paper Award & Young Reseacher Award (Multi-Purpose Hall 1F)

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
9:00-10:30 **Area 1: Advanced Gate Stack /Si Processing Science** A-3: Reliability-I	**9:00-10:30** **Area 3: CMOS Devices/Device Physics** B-3: CMOS Integration	**9:00-10:30** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-3: Plasma Induced Damage of Low-k Materials	**9:00-10:20** **Area 5: Advanced Circuits and Systems** D-3: RF Components	**9:00-10:30** **Area 7: Photonic Devices and Device Physics** E-3: Special Session: Photonic Crystals and Si Photonics II	**9:00-10:15** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-3: Group-IV Semiconductors I	**9:00-10:15** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-3: High-Speed Devices and ICs I	**9:00-10:30** **Area 13: Applications of Nanotubes and Nanowires** H-3: Nanowire & Nanotube Sensors		**9:00-10:20** **Area 4: Advanced Memory Technology** J-3: Flash Memory II	(Poster setting)
10:45-12:15 **Short Presentation** **Area 1**	**10:45-12:15** **Short Presentation** **Area 3**	**10:45-12:15** **Short Presentation** **Area 2 and Area 12**	**10:45-12:15** **Short Presentation** **Area 5 and Area 11**	**10:45-12:15** **Short Presentation** **Area 7**	**10:45-12:15** **Short Presentation** **Area 8**	**10:45-12:15** **Short Presentation** **Area 6**	**10:45-12:15** **Short Presentation** **Area 10 and Area 13**	**10:45-12:15** **Short Presentation** **Area 9**	**10:45-12:15** **Short Presentation** **Area 4**	
13:00-15:00 Poster Session (Multi-Purpose Hall 1F)										
15:15-16:25 **Area 1: Advanced Gate Stack /Si Processing Science** A-5: Junction	**15:15-16:35** **Area 3: CMOS Devices/Device Physics** B-5: Mobility Characterization	**15:15-16:45** **Area 12: Spintronic Materials and Devices** C-5: Symposium on Magnetic Tunnel Junctions and Beyond	**15:15-16:15** **Area 5: Advanced Circuits and Systems** D-5: RF CMOS Circuits and Systems	**15:15-16:30** **Area 7: Photonic Devices and Device Physics** E-5: Special Session: Photonic Crystals and Si Photonics III	**15:15-16:30** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-5: Group-IV Semiconductors II	**15:15-16:15** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-5: High-Speed Devices and ICs II	**15:15-16:30** **Area 13: Applications of Nanotubes and Nanowires** H-5: Nanowire Growth and Devices I		**15:15-16:25** **Area 4: Advanced Memory Technology** J-5: PRAM	(Poster removed by 18:00)
16:45-18:05 **Area 1: Advanced Gate Stack /Si Processing Science** A-6: Reliability-II	**16:45-18:05** **Area 3: CMOS Devices/Device Physics** B-6: Device Technology	**17:00-18:00** **Area 12: Spintronic Materials and Devices** C-6: Symposium on Magnetic Tunnel Junctions and Beyond		**16:45-18:00** **Area 7: Photonic Devices and Device Physics** E-6: Detectors and Sensors	**16:45-17:45** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-6: Group-IV Semiconductors III	**16:45-18:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-6: Process and Characterization	**16:45-17:45** **Area 13: Applications of Nanotubes and Nanowires** H-6: Nanowire Growth and Devices II		**16:45-17:55** **Area 4: Advanced Memory Technology** J-6: ReRAM	

18:30-20:30 Rump Session **Room 101(A) "Oxide Electronics -Status and Outlook-"**
Room 102(B) "New Materials meet Advanced Silicon Technology"

Friday, September 21

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
9:00-10:30 **Area 1: Advanced Gate Stack /Si Processing Science** A-7: Metal Gate-II	**9:00-10:20** **Area 3: CMOS Devices/Device Physics** B-7: Stress Enhancement Technologies	**9:00-10:30** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-7: Interconnects for RF and Mixed Signal Application	**9:00-10:30** **Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)** D-7: Nano-Bio Devices I	**9:00-10:30** **Area 7: Photonic Devices and Device Physics** E-7: All-Optical Light Control	**9:00-10:15** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-7: Material Characterization	**9:00-10:30** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** G-7: Emerging Devices	**9:00-10:30** **Area 10: Organic Materials Science, Device Physics, and Applications** H-7: Organic Transistor I		**9:00-10:20** **Area 4: Advanced Memory Technology** J-7: DRAM II	
10:45-12:05 **Area 1: Advanced Gate Stack /Si Processing Science** A-8: High-k/Metal Gate Transistor	**10:45-12:25** **Area 3: CMOS Devices/Device Physics** B-8: Modeling and Simulation	**10:45-12:15** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-8: Interconnect Reliability	**10:45-12:15** **Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)** D-8: Nano-Bio Devices II	**10:45-12:15** **Area 7: Photonic Devices and Device Physics** E-8: Lasers and LEDs			**10:45-12:15** **Area 10: Organic Materials Science, Device Physics, and Applications** H-8: Organic Transistor II	**10:45-12:00** **Area 9: Physics and Applications of Novel Functional Materials and Devices** I-8: Novel Nanostructure Devices	**10:45-12:05** **Area 4: Advanced Memory Technology** J-8: FeRAM/MRAM	
13:15-14:55 **Area 1: Advanced Gate Stack /Si Processing Science** A-9: FUSI	**13:15-14:55** **Area 3: CMOS Devices/Device Physics** B-9: Post Planar CMOS	**13:15-15:05** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-9: Low-k and Airgap	**13:15-14:45** **Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)** D-9: Spectroscopy for Bio Sensing	**13:15-15:00** **Area 7: Photonic Devices and Device Physics** E-9: LEDs	**13:15-14:55** **Area 1: Advanced Gate Stack/Si Processing Science** F-9: Characterization	**13:15-14:35** **Area 5: Advanced Circuits and Systems** G-9: Imaging Technology	**13:15-14:45** **Area 10: Organic Materials Science, Device Physics, and Applications** H-9: Organic Transistor III	**13:15-15:00** **Area 9: Physics and Applications of Novel Functional Materials and Devices** I-9: Quantum Dots and Qubits	**13:15-15:00** **Area 13: Applications of Nanotubes and Nanowires** J-9: Carbon Nanotube Devices and Growth I	
	15:15-17:05 **Area 3: CMOS Devices/Device Physics** B-10: Noise and RF	**15:25-16:25** **Area 2: Characterization and Materials Engineering for Interconnect Integration** C-10: Nanoscale Characterization	**15:15-16:45** **Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)** D-10: μ-TAS and Medical Applications		**15:15-16:35** **Area 1: Advanced Gate Stack/Si Processing Science** F-10: Advanced Process	**15:15-16:35** **Area 5: Advanced Circuits and Systems** G-10: Connectivity		**15:15-16:45** **Area 9: Physics and Applications of Novel Functional Materials and Devices** I-10: Novel Devices	**15:15-16:30** **Area 13: Applications of Nanotubes and Nanowires** J-10: Carbon Nanotube Devices and Growth II	

SSDM 2007 Advance Program
General Information

DATE
Conference: **September 19-21, 2007 (Official language is English)**
Short Course: **September 18, 2007 (in Japanese)**

LOCATION
Tsukuba International Congress Center (EPOCHAL TSUKUBA)
2-20-3 Takezono, Tsukuba, Ibaraki, 305-0032, Japan
Phone: +81-29-861-0001   Fax: +81-29-861-1209
Tsukuba International Congress Center, located in Tsukuba Science City, is a core facility for research exchanges in Japan. People more than 2 million have visited the Center since its establishment in 1999, demonstrating the Center's great contribution to such exchanges. The Congress Center is located just 50 km from Tokyo and 40 km from Narita Airport. With the recent opening of the Tsukuba Express, Tsukuba can be accessed in 45 min from Akihabara, Tokyo.
http://www.epocal.or.jp/index.html

REGISTRATION
The registration desk will be open from September 18 to 21 in the entrance hall on the first floor. The registration hours are as follows:

September 18	9:00-17:00	Convention Hall (3F)
19	9:00-12:00	Main Convention Hall (1F)
19	12:00-17:00	Entrance Hall (1F)
20	9:00-17:00	Entrance Hall (1F)
21	9:00-15:30	Entrance Hall (1F)

Early registration will be accepted only through the conference website until August 17, 2007, 13:00 Japan time. (http://www.ssdm.jp)
Advanced registration through the conference website will be closed September 5, 2007, 17:00 Japan time. After the date, registration can be made at the conference site as on-site registration. Early registration is recommended.

	Registration Fee		Short Course (in Japanese)	Banquet
	Before 13:00, August 17 (Japan time)	After 13:00, August 17 (Japan time)		
Regular	JPY45,000	JPY50,000	JPY15,000	JPY7,000
Student	JPY7,000		JPY3,000	JPY4,000
Accompanied person				JPY4,000

* Fees include tax.

1) The registration fee includes one copy of the abstract book and a CD-ROM. However, it does not include the banquet, and an additional payment is required to attend the banquet (Regular: JPY7,000, Student/Accompanied person: JPY4,000).
2) Those who register as students are required to fax a copy of their current student ID to Kinki Nippon Tourist Co., Ltd. (KNT) (Fax: +81-3-5256-1588) at the time of registration and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of the online registration of individual information.
3) Registration is complete only after payment is made in full.

Payment Procedure
Payment can be made by:
- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. American Express 5. JCB
- A bank transfer to KNT Co., Ltd. (Message: SSDM)
  Account at Sumitomo Mitsui Banking Corp., Suzuran Branch, 1-3-12 Nishishimbashi, Minato-ku, Tokyo 105-0003, Japan (SWIFT Code: SMBCJPJT, Ordinary Account: 6103515, Account Name: Kinki Nippon Tourist Co., Ltd.)

* Personal checks are not acceptable.

Confirmation of Pre-Registration
Upon receipt of your online registration, a written confirmation will be faxed or e-mailed to you after your payment is confirmed.
Please bring this confirmation slip with you and present it to the registration desk.

Registration Cancellation
Conference:
Cancellation fee of JPY3,000 will be deducted from the refund. Cancellation should be made in writing to KNT Co., Ltd. No cancellation will be accepted on or after August 21, 2007. Extended Abstracts will be sent to absent registrants after the conference.

Short Course:
Cancellation fee of JPY2,000 will be deducted from the refund. Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be accepted on or after August 21, 2007. Short-course textbooks will be sent to the absent registrants after the conference.

Banquet:
Cancellation fee of JPY1,000 will be deducted from the refund, Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be acccepted on or after August 21, 2007.

Inquiries for Registration
Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho
Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2007-gb@or.knt.co.jp
Office hours: 9:30-17:30 (weekdays only)

On-site Registration
Registration fees should be paid in Japanese Yen or credit cards. VISA, MasterCard, Diners Club, American Express and JCB are acceptable. No personal checks are acceptable.

BANQUET
The conference banquet will be held on the evening of Wednesday, September 19. The banquet fee (Regular: JPY7,000, Student/Accompanied person: JPY4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

LATE NEWS PAPERS
Submission of Late News Papers has been already closed on 24:00, July 30, 2007 (Japan time). The accepted papers will be on "Advance Program Part II" which will be distributed at the venue during the conference.

SPECIAL Issue of JJAP
Authors of papers presented at SSDM 2007 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April 2008.

RUMP SESSIONS - September 20 (Thursday) 18:30-20:30

Session A (Room 101, 1F)

"Oxide Electronics – Status and Outlook –"

Increasing interests on oxides are attracted by the rich possibilities and keen demands of metal-oxides as the key materials for future electronics. High-k oxides for alternative gate dielectrics and ferroelectric capacitors for non-volatile memories are well known examples for the SSDM community. Even more exciting applications are now being uncovered, from ultraviolet light emitting devices and high mobility thin film transistors through electric-control of magnetism in multiferroics to resistance change nonvolatile memories. Several keynotes will be delivered for the latter by panelists and near-future challenges in the emerging materials research will be discussed with the audience.

Organizer/Moderator: M. Kawasaki (Tohoku Univ., Japan)

Panelists: H. Akinaga (AIST, Japan)
T. Kamiya (Tokyo Tech., Japan)
H. Okamoto (Univ. of Tokyo, Japan)

A couple of panelists may be added.

Session B (Room 102, 1F)

"New Materials Meet Advanced Silicon Technology"

Scaling device dimensions has been the most powerful and effective strategy to boost device performance for last 40 years. In recent years, however, we face a number of obstacles to the effectiveness of this strategy. Unfortunately, some of the obstacles seem to be irremovable by evolving the traditional "silicon technology". If fact, one might concern that some fundamental problems and limits reside in our traditional materials: Si, SiO_2, etc. Therefore, the introduction of materials which are/were new to researchers in silicon community is almost inevitable for enhancing device & LSI performance continuously (stepwise?) and for adding "new functionality" to LSIs in future, and will be a new vehicle, which takes us to a promised land (not a hell), where advanced LSIs improve our quality of life in many respects. In this rump session, we will discuss "new materials" for advanced silicon technology. Which materials will be used for which purposes, and when? What are criteria of introducing a certain material into LSIs? Can new or innovative materials (including nanoscale Si dots and wires) provide additional functionality to LSIs? By collaborating prominent panelists and audience, we will try to draw a private roadmap for new materials in LSIs. Particularly, we would like to encourage material specialists to join the discussion since the silicon technology really needs their help.

Organizer: H. Ishiuchi (Toshiba Corp., Japan)
Moderators: K. Uchida (Toshiba Corp., Japan)
F. Boeuf (ST Microelectronics, France)

Panelists: H. Watanabe (NEC Corp., Japan)
S. Takagi (Univ. of Tokyo, Japan)
T. Usui (Toshiba Corp., Japan)
A. S. Spinelli (Politecnico di Milano, Italy)
E. Y. Chang (National Chiao Tung Univ., Taiwan)
M. Mueller (NXP Semiconductors Research, Belgium)

One or two more panelists will be added.

SHORT COURSE

Short Course entitled “Emerging Silicon Technology” will be held on Tuesday, September 18 at Convention Hall (3F) . All lectures are given in Japanese.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

AWARDS

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 2001.

SSDM Paper Award

Given for the best paper presented at the previous year’s conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year’s conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted, and who have applied for the grant. Submitting an application form does not guarantee that the grant will be awarded. Each related area chair will choose one candidate from the applicants. Late news papers are not eligible for travel grant.

The grant is authorized by the Marubun Research Promotion Foundation (MRPF), which is one of the cooperation organizations. The grant covers part of the recipient’s travel costs, but does not necessarily cover all their expenses. Successful candidates must attend the ceremony which will be held during the conference (details of which will be given later) to receive the grant. Failure to attend will result in forfeiture of the grant.

VISA REQUIREMENT

All overseas participants must have a valid passport.

Overseas participants who require a visa should consult the nearest Japanese Embassy or Consulate as soon as possible. If your paper is accepted for presentation at SSDM 2007 and your visa application requires an invitation to attend the conference, please contact the SSDM Secretariat.

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F, 19-2 Kanda-Matsunaga-cho, Chiyoda-ku
Tokyo 101-8641, JAPAN
Phone: +81-3-5256-1581 Fax: +81-3-5256-1588
E-mail: ssdm2007-gb@or.knt.co.jp

Hotel Accommodations

Rooms have been reserved at hotels around Conference venue (EPOCHAL TSUKUBA) by KNT. Hotel reservations are proceeded on first-come-first-served basis. If your selected hotel is fully booked, we will make a reservation at your second choice hotel. After application deadline, KNT will send a confirmation slip informing the confirmed hotel name, and the exact room charge. Reservations can be made through the conference website. (http://www.ssdm.jp)

Hotel Name	**Okura Frontier Hotel Tsukuba**
Room Rates	Single: JPY11,550 Twin: JPY10,500 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-1364-1, Azuma Tsukuba, Ibaraki 305-0031, Japan
Phone	+81-29-852-1112
Access to Hotel	2 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	6 min. walk

Hotel Name	**Okura Frontier Hotel Tsukuba Epochal**
Room Rates	Single: JPY11,550 Twin: JPY10,500 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	2-20-1 Takezono, Tsukuba, Ibaraki 305-0032, Japan
Phone	+81-29-860-7700
Access to Hotel	8 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	Next to the site

Hotel Name	**Hotel Grand Shinonome**
Room Rates	Single: JPY7,500
Hotel Deposit	JPY10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	488-1 Onozaki, Tsukuba, Ibaraki 305-0034, Japan
Phone	+81-29-856-2211
Access to Hotel	5 min. walk from Tsukuba Sta.
To Conference site	13 min. walk

Hotel Name	**Hotel Route Tsukuba**
Room Rates	Single: JPY6,825
Hotel Deposit	JPY10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	1145-3 Hanamuro, Tsukuba, Ibaraki 305-0025, Japan
Phone	+81-29-860-2111
Access to Hotel	20 min. walk (or 5 min. by taxi) from Tsukuba Sta.
To Conference site	30 min. walk (or 10 min. by taxi)

Hotel Name	**Tsukuba Daily Inn**
Room Rates	Single: JPY6,930
Hotel Deposit	JPY10,000
Check-in/out	Check-in:16:00/Check-out:10:00
Address	1-12-4 Sengen, Tsukuba, Ibaraki 305-0047, Japan
Phone	+81-29-851-0003
Access to Hotel	30 min. walk (or 7 min. by taxi) from Tsukuba Sta.
To Conference site	15 min. walk (or 3 min. by taxi)

Hotel Name	**Akihabara Washington Hotel**
Room Rates	Single: JPY11,550 Twin: JPY8,925 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-8-3 Sakumacho, Kanda, Chiyoda-ku, Tokyo 101-0025, Japan
Phone	+81-3-3255-3311
Access to Hotel	1 min. walk from Tsukuba Express Akihabara Sta.
To Conference site	45 min. by Tsukuba Express and 8 min. walk

Hotel Name	**Asakusa View Hotel**
Room Rates	Single: JPY15,693
Hotel Deposit	JPY20,000
Check-in/out	Check-in:13:00/Check-out:11:00
Address	3-17-1 Nishi-Asakusa, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1111
Access to Hotel	1 min. walk from Tsukuba Express Asakusa Sta.
To Conference site	40 min. by Tsukuba Express and 8 min. walk

Hotel Name	**Hotel Sunroute Asakusa**
Room Rates	Single: JPY9,500
Hotel Deposit	JPY10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-8-5 Kaminarimon, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1511
Access to Hotel	5 min. walk from Tsukuba Express Asakusa Sta.
To Conference site	40 min. by Tsukuba Express and 8 min. walk

Hotel Name	**Tsukuba Kenshu Center**
Room Rates	Single: JPY4,900 Single with breakfast: JPY5,300
Hotel Deposit	The payment in full for your room charge
Check-in/out	Check-in:16:00(no later than 23:00)/Check-out:10:00
Address	1-13-5 Amakubo, Tsukuba, Ibaraki 305-0005, Japan
Phone	+81-29-851-5152
Access to Hotel	10 min. by bus and 10 min. walk from Tsukuba Sta.
To Conference site	10 min. walk and 15 min. by bus

Notes: 1) All room rates are per person per night including breakfast and 10% service charge, but excluding consumption tax.
2) The above rates are valid only during the period of the SSDM 2007 meeting.
3) Communication fee of 500 JPY is required for per reservation and this is charged as handling charge for KNT.
4) The deposit will be deducted from your hotel bill. Please settle the balance with the hotel cashier.
5) The above rates and information are subject to change without notice.
6) It is excluding breakfast in room charge at Tsukuba Kenshu Center. More information, please contact to KNT.

Application and Payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website. The page will be opened in early June and hotel reservations should be made by no later than August 18 , 2007 (Japan time) . A confirmation sheet will be sent by KNT after the application crealine.
Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment. All payment must be paid only in Japanese yen by one of the following methods.

1) Credit Card:
   (VISA, MasterCard, Diners Club, American Express or JCB only)
   * Please fill in the necessary items with your signature in the credit card section of the application form.
2) Bank Transfer:
   Sumitomo Mitsui Banking Corp.
   Suzuran Branch
   SWIFT Code: SMBCJPJT
   Ordinary Account: 6103515
   Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation Policy for Accommodations

In case of cancellation, a written notification should be sent to KNT by e-mail (ssdm2007-gb@or.knt.co.jp) or by FAX (+81-3-5256-1588) to avoid any trouble.
Hotels: Up to 14 days before the arrival date No Charge
13−7 days before .... 10 % of daily room charge
6-2 days before .... 40 % of daily room charge
Less than 2 days, or no notice given . 100 % of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate’s stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Tsukuba is warm and sometimes humid in September. The temperature range is 18-30℃ .

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tsukuba (conference site) and Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

SSDM 2007 INSTRUCTION for SPEAKERS

Oral Presentation

Time Schedule

	Session Time	Presentation	Discussion
Plenary	40 min.	35 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	17 min.	3 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of speech , Third: End of discussion.

Audio-Visual Equipment

The meeting rooms will contain the following audiovisual equipment:

・LCD projector **(PC itself is not provided)**
・Microphone
・Projection laser pointer

Speakers wishing to present their papers using the LCD projector are requested to verify their PC's compatibility with the LCD projector that will be located in the Preview Room (402) on the fourth floor prior to their presentations.

Poster Presentation

Poster sessions are scheduled for Thursday, September 20, from 13:00 to 15:00 at Multi-Purpose Hall(1F). Poster boards will be available with identifying labels at Multi-Purpose Hall on the first floor. Authors are requested to prepare their posters between 9:00 and 12:00 on September 20 and remove them by 18:00 on September 20. Any posters remaining after 18:00 will be disposed of by the secretariat. Usable space on each poster board will be approximately 900 mm wide and 1,500 mm high. Pushpins will be available. Each presentation will be assigned a board, labeled with the paper number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are required to make 2 minutes short oral presentation of September 20. The presentation time should be kept strictly to 2 minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations be held in a quick, successive sequence. While one speaker is giving his/her presentation, the next several speakers should wait nearby in line for their turn in order to move on to the next presentation. Note that any absent speakers will be skipped and each presentation will be automatically stopped after 2 minutes have elapsed. Only a PC projector will be made available. You should send your presentation file to the secretariat (ssdm2007-abs@intergroup.co.jp) by e-mail by August 24. The file must be an exact “2-page” landscape PDF. Because the presentation time is limited, please describe your research objective and results clearly and do NOT show the author list or the title on your file, those of which will be prepared by the SSDM Secretariat.

Short oral presentations will be held, as follows.

Room 101	Area 1		
Room 102	Area 3	Room 303	Area 6
Room 201A	Area 2, 12	Room 304	Area 10, 13
Room 201B	Area 5, 11	Room 405	Area 9
Room 202A	Area 7	Room 406	Area 4
Room 202B	Area 8		

Main Convention Hall, 1F

PL: Opening Session (10:00-12:30)
Chairpersons: Y. Awano, Fujitsu Labs. Ltd. and S. Zaima, Nagoya Univ.

10:00 PL-0
Welcome Address and Award Presentation
N. Yokoyama, Fujitsu Labs. Ltd.

10:30 PL-1
New Technology: Silicon Photonics: Opportunity, Challenges & Applications
M. Paniccia, Intel Corp., USA

11:10 PL-2
Organic Transistors: towards Ambient Electronics
T. Someya, Univ. of Tokyo, Japan

11:50 PL-3
Try Disruptive Technology!
H. Watanabe, Selete Inc., Japan

12:30-14:00 Lunch

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 5: Advanced Circuits and Systems**	**Area 7: Photonic Devices and Device Physics**
A-1: Metal Gate-I (14:00-15:50) Chairs: Y. Nara (Selete) J. Yugami (Renesas Tech. Corp.)	B-1: Ge, SiGe Channel Transistor Technology (14:00-16:00) Chairs: J. C. S. Woo (Univ. of California, Los Angeles) Y. Momiyama (Fujitsu Labs. Ltd.)	C-1: Novel Interconnects (14:00-15:50) Chairs: T. Yoda (Toshiba Corp.) M. Nihei (Fujitsu Labs. Ltd.)	D-1: Scaling and Circuit Design Concern (14:00-15:50) Chairs: H. Kobayashi (Gunma Univ.) T. Komuro (Agilent Technologies International Japan, Ltd.)	E-1: Quantum-Dot Devices (14:00-16:00) Chairs: M. Sugawara (Fujitsu Labs. Ltd.) M. Tokushima (NEC Corp.)

※ Country of first author's affiliation is shown in parentheses.

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 4: Advanced Memory Technology**
F-1: Compound Semiconductors (14:00-16:00) Chairs: M. Takahasi (JAEA) T. Fukui (Hokkaido Univ.)	G-1: GaN FETs I (14:00-16:00) Chairs: S. Tanaka (NEC Corp.) M. Kuzuhara (Univ. of Fukui)	H-1: Organic Photo-Electronics (14:00-16:00) Chairs: H. Usui (Tokyo Univ. of Agri. and Tech.) H. Kajii (Osaka Univ.)	I-1: Novel Si Transistors (14:00-16:00) Chairs: Y. Takahashi (Hokkaido Univ.) Y. Suda (Tokyo Univ. of Agri. and Tech.)	J-1: DRAM I (14:00-15:50) Chairs: I. Asano (Elpida Memory, Inc.) H. Jeong (Samsung Electronics Co., Ltd.)

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 5: Advanced Circuits and Systems**	**Area 7: Photonic Devices and Device Physics**
14:00 A-1-1 (Invited) Challenges for PMOS metal gate electrodes and solutions for low power applications J. Schaeffer, *Freescale Semiconductor Inc. (USA)*	**14:00 B-1-1** High mobility Ge channel metal source/drain pMOSFETs with nickel fully silicided gate K. Ikeda[1], N. Taoka[2], Y. Yamashita[1], M. Harada[1], K. Suzuki[1], T. Yamamoto[1], N. Sugiyama[1] and S. Takagi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo (Japan)*	**14:00 C-1-1 (Invited)** Si-Based Infrared Light Emitters Using Semiconducting Iron Disilicide T. Suemasu, S. Murase, Y. Ugajin and M. Suzuno, *Univ. of Tsukuba (Japan)*	**14:00 D-1-1 (Invited)** Next generation compact model for digital and analog circuit design T. Ohguro, *Toshiba Corp. (Japan)*	**14:00 E-1-1 (Invited)** High-Speed Quantum Dot Lasers P. Bhattacharya and Z. Mi, *Univ. of Michigan (USA)*
14:30 A-1-2 PMOSFET Vth Modulation Technique using Fluorine Treatment through ALD-TiN Suitable for CMOS Devices K. Tai, S. Yamaguchi, K. Tanaka, T. Hirano, I. Oshiyama, S. Kazi, T. Ando, M. Nakata, M. Yamanaka, R. Yamamoto, S. Kanda, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, N. Nagashima and S. Kadomura, *Sony Corp. (Japan)*	**14:20 B-1-2** Integration of Dual Channels MOSFET on Defect-Free, Tensile-Strained Germanium on Silicon H. Zang[1,2], W. Y. Loh[2], J. D. Ye[2], T. H. Loh[2], G. Q. Lo[2] and B. J. Cho[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*	**14:30 C-1-2** Electrical properties of carbon nanotubes grown at a low temperature by radical chemical vapor deposition for future LSI interconnects D. Yokoyama[1], K. Ishimaru[1], T. Iwasaki[1], S. Sato[2], T. Hyakushima[2], M. Nihei[2], Y. Awano[2] and H. Kawarada[1], *[1]Waseda Univ. and [2]MIRAI-Selete (Japan)*	**14:30 D-1-2 (Invited)** Characterization and modeling of layout dependent parametric variability of nanometer devices C. Guardiani, *PDF Solutions (Italy)*	**14:30 E-1-2 (Invited)** MOCVD Growth of Quantum-Dot Optical Devices K. Kawaguchi[1], N. Yasuoka[1], M. Ekawa[1], H. Ebe[2], T. Akiyama[3], M. Sugawara[1,3] and Y. Arakawa[2], *[1]Fujitsu Labs. Ltd., [2]Univ. of Tokyo and [3]QD Laser Inc. (Japan)*

Wednesday, September 19

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 4: Advanced Memory Technology**
14:00 F-1-1 (Invited) InAs/In(Ga,Al)AsSb Quantum Dot Heterostructures for Photonic Devices J. I. Chyi[1,2], P. C. Chiu[1], M. J. Shiau[1], T. P. Hsieh[1] and M. N. Chang[3], *[1]National Central Univ., [2]Academic Sinica and [3]National Nano Device Labs. (Taiwan)*	**14:00 G-1-1 (Invited)** Next Generation High-Efficiency RF Transmitter Technology for Basestations P. Asbeck[1], D. Kimball[1], J. Jeong[2], P. Draxler[1], C. Hsia[1] and L. Larson[1], *[1]Univ. of California, San Diego and [2]Kwangwoon Univ. (USA)*	**14:00 H-1-1 (Invited)** Plastic dye-sensitized solar cells and solidification with nano-carbon materials T. Miyasaka[1,2], *[1]Toin Univ. of Yokohama and [2]Peccell Tech., Inc. (Japan)*	**14:00 I-1-1 (Invited)** 3D Stacked Nanowires CMOS Integration with a Damascene Finfet Process T. Ernst[1], C. Dupré[1,2], E. Dornel[1], J. C. Barbé[1], S. Bécu[1], C. Vizioz[1], V. Delaye[1], F. Andrieu[1], J. M. Hartmann[1], S. Barnola[1], T. Poiroux[1], O. Faynot[1], G. Ghibaudo[2] and S. Deleonibus[1], *[1]CEA-LETI and [2]IMEP (France)*	**14:00 J-1-1 (Invited)** Overview and Future Challenges of Floating Body RAM Technologies T. Shino, T. Ohsawa, T. Hamamoto and A. Nitayama, *Toshiba Corp. (Japan)*
14:30 F-1-2 (Invited) Present Status and Future Issues of III-V Semiconductor Nanowires K. Hiruma, M. Yazawa, K. Haraguchi, K. Ogawa and T. Katsuyama, *Hitachi, Ltd. (Japan)*	**14:30 G-1-2** Normally-off AlGaN/GaN MIS-HFETs Using Non-polar *a*-Plane M. Kuroda, T. Ueda and T. Tanaka, *Matsushita Electric Industrial Co., Ltd. (Japan)*	**14:30 H-1-2** Efficiency Improvement of Organic Solar Cells by Annealing for Active Layer C. K. Chen, Y. S. Tsai, W. P. Chu, L. W. Ji and T. H. Meen, *National Formosa Univ. (Taiwan)*	**14:30 I-1-2** 3D Multi-gate NMOS Mobility Enhancement with High-tensile ILD-SiN_x Stressor W. S. Liao[1], S. Y. Huang[1], K. M. Chen[2], H. C. Tsen[1] and L. Chung[1], *[1]UMC and [2]National Nano Device Labs. (Taiwan)*	**14:30 J-1-2** URCAT (U-shaped-Recess-Channel-Array Transistor) Technology for 60nm DRAM and beyond C. Lee, J. C. Park, S. H. Park, S. S. Lee, S. D. Hong, I. G. Kim, Y. J. Choi, T. W. Lee, G. Y. Jin and K. Kim, *Samsung Electronics Co., Ltd. (Korea)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

14:50 A-1-3
Low Threshold Voltage Gate-First pMISFETs with Poly-Si/TiN/HfSiON Stacks Fabricated with PVD-based In-situ Solid Phase Interface Reaction (SPIR) Method
N. Kitano[1,3], H. Arimura[1], S. Horie[1], T. Hosoi[1], T. Shimura[1], H. Watanabe[1], T. Kawahara[2], S. Sakashita[2], Y. Nishida[2], J. Yugami[2], T. Minami[3] and M. Kosuda[3], *[1]Osaka Univ., [2]Renesas Tech. Corp. and [3]Canon ANELVA Corp. (Japan)*

15:10 A-1-4
Achieving Band Edge Effective Work Function of Gate First Metal Gate by Oxygen Anneal Processes: Low Temperature Oxygen Anneal (LTOA) and High Pressure Oxygen Anneal (HPOA) Processes
C. S. Park[1], S. C. Song[1], C. Burham[2], H. B. Park[3], H. Niimi[4], B. S. Ju[1], J. Barnett[1], C. Y. Kang[1], P. Lysaght[1], G. Bersuker[1], R. Choi[1], H. K. Park[5], H. Hwang[5], B. H. Park[6], S. Kim[6], P. Kirsch[7], B. H. Lee[7] and R. Jummy[7], *[1]SEMATECH, [2]Univ. of Texas at Austin, [3]Sumsung Assigner, [4]TI Assignee, [5]GIST, [6]Poongsan Microtec and [7]IBM (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

14:40 B-1-3
Electrical Stress Effects on Mobility of Germanium-On-Insulator (GeOI) pMOSFETs with HfO_2 Gate Dielectric
J. H. Yi, S. Oh and H. S. P. Wong, *Stanford Univ. (USA)*

15:00 B-1-4
Pt-germanide Formed by Laser Annealing and Its Application for Schottky Source/Drain MOSFET Integrated with TaN/CVD-HfO_2/Ge Gate Stack
R. Li[1], S. J. Lee[1], D. Z. Chi[2], M. H. Hong[1] and D. L. Kwong[3], *[1]National Univ. of Singapore, [2]Inst. of Materials Research and Engineering and [3]Inst. of Microelectronics (Singapore)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

14:50 C-1-3
Carbon Nanotube Vias Fabricated by Remote Plasma-Enhanced Chemical Vapor Deposition
M. Katagiri, N. Sakuma, M. Suzuki, T. Sakai, S. Sato, T. Hyakushima, M. Nihei and Y. Awano, *MIRAI-Selete (Japan)*

15:10 C-1-4
A Novel Contact-plug Process with Low Resistance Nucleation Layer Using B_2H_6-reduction W-ALD Method for 32 nm CMOS Devices and Beyond
A. Yutani, K. Ichinose, K. Maekawa, K. Asai and M. Kojima, *Renesas Tech. Corp. (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

15:10 D-1-3
Investigation of Matching Performance for Uniaxial Strained PMOSFETs
J. J. Y. Kuo, W. P. N. Chen and P. Su, *National Chiao Tung Univ. (Taiwan)*

15:30 D-1-4
Novel Soft Error Hardened Latches and Flip-Flops
T. Uemura, R. Tanabe, Y. Tosaka and S. Satoh, *Fujitsu Labs. Ltd. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

15:00 E-1-3
First Demonstration of Electrically Driven 1.55 μm Single-Photon Generator
T. Miyazawa[1], S. Hirose[2], S. Okumura[2], K. Takemoto[2], M. Takatsu[2], T. Usuki[1], N. Yokoyama[2] and Y. Arakawa[1], *[1]Univ. of Tokyo and [2]Fujitsu Labs. Ltd. (Japan)*

15:15 E-1-4
Electroluminescence from Multiple-Stacked Structures of Impurity Doped Si Quantum Dots
K. Okuyama, K. Makihara, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

15:00 F-1-3
In situ Metal Mask for Selective Area Growth of Thin Epitaxial Layers
S. Ohkouchi[1,2], N. Ozaki[3], Y. Takata[3], Y. Kitagawa[3], Y. Nakamura[4], N. Ikeda[5], Y. Sugimoto[3,5] and K. Asakawa[3], *[1]AIST, [2]NEC Corp., [3]Univ. of Tsukuba, [4]Kumamoto Univ. and [5]NIMS (Japan)*

15:15 F-1-4
Optimization of Well Width and of N Composition on Optical Properties for GaNAs/GaAs MQW grown by RF-MBE
K. Fujii[1], D. Nakase[1], T. Kumamoto[1], Y. Iwata[1], N. Tsurumachi[1], H. Miyagawa[1], H. Itoh[1], S. Nakanishi[1], H. Akiyama[2] and S. Koshiba[1], *[1]Kagawa Univ. and [2]Univ. of Tokyo (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

14:45 G-1-3
Gain Improvement of Enhancement-mode AlGaN/GaN HEMTs Using Dual-Gate Architectures
R. Wang, Y. Wu, W. C. W. Tang, K. M. Lau and K. J. Chen, *Hong Kong Univ. of Sci. and Tech. (China)*

15:00 G-1-4
p-type InGaN Cap Layer for Normally-off Operation in AlGaN/GaN HFETs
M. Shimizu[1], G. Piao[1], M. Inada[1], H. Okumura[1], Y. Yano[2] and N. Akutsu[2], *[1]AIST and [2]Taiyo Nippon Sanso Corp. (Japan)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

14:45 H-1-3
Surface Plasmon Excitation and Emission Light properties for Prism/MgF_2/Ag/MEH-PPV Film Structure
K. Shinbo, M. Hafuka, M. Minagawa, Y. Ohdaira, A. Baba, K. Kato and F. Kaneko, *Niigata Univ. (Japan)*

15:00 H-1-4
Fabrication of Dual-disks Microlasers in Thiophene/Phenylene Co-oligomers
F. Sasaki[1], S. Kobayashi[1], S. Haraichi[1], S. Fujiwara[2], Y. Ido[2], K. Bando[2], Y. Masumoto[2] and S. Hotta[3], *[1]AIST, [2]Univ. of Tsukuba and [3]Kyoto Inst. of Tech. (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

14:45 I-1-3
The Drivability Enhancement Mechanisms in Nano-grating MOSFETs
X. Zhu[1], S. Kuroki[1], K. Kotani[1], M. Fukuda[2], H. Shido[2], Y. Mishima[2] and T. Ito[1], *[1]Tohoku Univ. and [2]Fujitsu Labs. Ltd (Japan)*

15:00 I-1-4
Low Contact Resistance with Low Schottky Barrier for N-type Silicon Using Yttrium Silicide
T. Isogai, H. Tanaka, T. Goto, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

14:50 J-1-3
RC-FinFET (Recessed Channel FinFET) Cell Transistor Technology for Future Generation DRAMs
M. Yoshida, J. R. Kahng, J. S. Moon, K. H. Jung, K. Kim, H. Sung, C. Lee, C. K. Kim, W. Yang and D. Park, *Samsung Electronics Co., Ltd. (Korea)*

15:10 J-1-4
Investigation on the Body Bias Dependency of Gate Induced Drain Leakage Current in the Body-Tied finFET
C. Lee, M. Yoshida, K. H. Jung, C. K. Kim, H. J. Kim, H. Park, W. S. Lee, K. Kim, J. Kahng, W. Yang and D. Park, *Samsung Electronics Co., Ltd. (Korea)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

15:30 A-1-5
Gate First PFET Poly-Si/TiN/Al_2O_3 Gate Stacks with Inversion Thicknesses Less than 15Å for High Performance or Low Power CMOS Applications
B. P. Linder, V. Narayanan, V. K. Paruchuri, E. Cartier and S. Kanakasabapathy, *IBM (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

15:20 B-1-5
Silicon Strain-Transfer-Layer (STL) and Graded Source/Drain Stressors for Enhancing the Performance of Silicon-Germanium Channel P-MOSFETs
G. H. Wang[1], E. H. Toh[1], K. M. Hoe[1], S. Tripathy[1], S. Balakumar[1], G. Q. Lo[2], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

15:40 B-1-6
New Observations on the Narrow Width Effect of the Hot Carrier and NBTI Reliabilities in pMOSFETs with Various Types of Strains
S. S. Chung[1], D. C. Huang[2], C. S. Lai[2], C. H. Tsai[3], P. W. Liu[3], Y. H. Lin[3], C. T. Tsai[3], G. H. Ma[3], S. C. Chien[3] and S. W. Sun[3], *[1]National Chiao Tung Univ., [2]Chang Gung Univ. and [3]UMC (Taiwan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

15:30 C-1-5
Plasma-Enhanced ALD Ru Thin Films on PVD-TaN Films with Smooth Morphology at Low Temperature Using DER Ru Precursor
K. Namba[1], N. Hosoi[1], N. Tarumi[1], H. Shinriki[2] and S. Ogawa[1], *[1]Selete and [2]ASM Japan K.K. (Japan)*

Room 201B (D)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

15:30 E-1-5
Electric-field control of coupled states in weakly coupled quantum dots
I. Morohashi, K. Komori, K. Goshima, T. Sugaya, S. Yamauchi and A. Shikanai, *[1]AIST and [2]CREST-JST (Japan)*

15:45 E-1-6
Improvement in Characteristics of InGaAs/GaAs Quantum-Dot PIN Photodetectors with Antireflection Photonic Crystals
J. J. Chen, Y. K. Su, R. W. Chuang, H. C. Yu, W. C. Chen, K. Y. Cheng and T. H. Shen, *National Cheng Kung Univ. (Taiwan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

15:30 F-1-5
Formation of InGaAs-On-Insulator Structures by Epitaxial Lateral Over Growth from (111) Si
T. Hoshii[1], M. Deura[1], M. Shichijo[1], M. Sugiyama[1], S. Sugahara[2], M. Takenaka[1], Y. Nakano[1] and S. Takagi[1], *[1]Univ. of Tokyo and [2]Tokyo Tech. (Japan)*

15:45 F-1-6
Growth of GaN on Si (111) using simultaneous AlN/α-Si_3N_4 buffer structure
T. H. Yang, J. C. Chang, J. T. Ku, S. G. Shen, Y. C. Chen and C. Y. Chang, *National Chiao Tung Univ. (Taiwan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

15:15 G-1-5
Finger Length Optimization for AlGaN/GaN HEMT and InGaP/GaAs HBT by Using FDTD Electromagnetic and Device Co-Simulation Technique
A. Chokki, Y. Shinohara, R. Ishikawa and K. Honjo, *Univ. of Electro-Communications (Japan)*

15:30 G-1-6
Layout Optimization of AlGaN/GaN HEMTs for High-power Applications
Y. S. Lin[1], T. C. Li[2], Y. C. Wang[3] and S. S. H. Hsu[1], *[1]National Tsing Hua Univ., [2]Industrial Tech. Research Inst. and [3]National Chiao Tung Univ. (Taiwan)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

15:15 H-1-5
Orientational Re-ordering of Polar Organic Monolayers by Cooperative Molecular Field Effect
D. Taguchi, N. Kajimoto, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

15:30 H-1-6
Embedded Process and Characterization Analysis of Discrete Capacitor in Organic-Base Substrate
S. M. Wu[1], E. Jahja[1], J. W. Wang[2], Z. Z. Lai[1] and W. K. Yeh[1], *[1]National Univ. of Kaohsiung and [2]ASE Electronics, Inc. (Taiwan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

15:15 I-1-5
Double-Spacer Impact-ionization MOS Transistor: Characterization and Analysis
E. H. Toh[1], G. H. Wang[1], G. Q. Lo[2], L. Chan[1], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

15:30 I-1-6
Identification of Single and Coupled Acceptors in Silicon Nano Field-Effect Transistors
M. A. H. Khalafalla, Y. Ono, K. Nishiguchi and A. Fujiwara, *NTT Corp. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

15:30 J-1-5
The Effect of Radical Oxidation on DRAM Cell Transistor with S-RCAT
S. G. Park, S. H. Joe, J. H. Kim, H. S. Song, I. D. Choi, S. H. Han, Y. S. Ahn, S. B. Park, J. S. Lee, S. N. Kim, W. T. Choi, K. J. Kim and K. S. Oh, *SamSung Electronics Co., Ltd. (Korea)*

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Break				
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 12: Spintronic Materials and Devices**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
A-2: Ge MIS (16:15-18:15) Chairs: S. Miyazaki (Hiroshima Univ.) H. Hwang (Gwangju Inst. of Sci. & Engineering)	B-2: Transport in Nanoscale MOSFETs (16:15-18:25) Chairs: F. Boeuf (STMicro-electronics) Y. Kamakura (Osaka Univ.)	C-2: Spintronic Materials and Quantum Structures (16:15-17:30) Chairs: Y. Ohno (Tohoku Univ.) S. Sugahara (Tokyo Tech.)	D-2: MEMS Technology (16:15-18:15) Chairs: M. Sasaki (Toyota Technological Inst.) O. Nakagawara (Murata Manufacturing Co., Ltd.)	E-2: Special Session: Photonic Crystals and Si Photonics I (16:15-18:15) Chairs: M. Sugawara (Fujitsu Labs. Ltd.) M. Tokushima (NEC Corp.)

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	
	15:45 G-1-7 A New 20-element distributed Small-Signal Model and Integrated Intelligent Extraction Method applied to AlGaN/GaN HEMTs up to 40GHz J. Lu, B. Liu, Y. Wang, M. Li, L. Ma, Z. Wang and Z. P. Yu, *Tsinghua Univ. (China)*	**15:45 H-1-7** Influence of Organic Functional Groups on the Electrical Properties of Carbon Black - A Theoretical Study A. Chutia, Z. Zhu, R. Sahnoun, H. Tsuboi, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*	**15:45 I-1-7** Photon-induced single-hole-tunneling current modulation in Si multiple-tunnel-junction field-effect transistor Z. A. Burhanudin, R. Nuryadi and M. Tabe, *Shizuoka Univ. (Japan)*	
Break				
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 4: Advanced Memory Technology**
F-2: Oxides (16:15-17:30) Chairs: J. I. Chyi (National Central Univ.) H. Yamaguchi (NTT Basic Research Labs.)	G-2: GaN FETs II (16:15-18:00) Chairs: T. Tanaka (Matsushita Electric Industrial Co., Ltd.) Y. Ohno (Univ. of Tokushima)	H-2: Organic Light Emitting Devices (16:15-18:00) Chairs: S. Tokito (NHK) M. Iwamoto (Tokyo Tech.)	I-2: Transport Through Novel Materials and Structures (16:15-18:00) Chairs: T. Fujisawa (NTT) K. Hirakawa (Univ. of Tokyo)	J-2: Flash Memory I (16:15-17:45) Chairs: Y. Yamauchi (Sharp Corp.) C. Hsu (eMemory Technology Inc.)

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 12: Spintronic Materials and Devices**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
16:15 A-2-1 Evaluation of SiO_2/GeO_2/Ge MIS Interface Properties by Low Temperature Conductance Method H. Matsubara[1], H. Kumagai[1], S. Sugahara[2], M. Takenaka[1], S. Takagi[1], *[1]Univ. of Tokyo and [2]Tokyo Tech. (Japan)*	**16:15 B-2-1 (Invited)** Technology Oriented Analytical Models of MOSFETs in the Quasi Ballistic Regime R. Clerc[1], Q. Rafhay[1], M. Ferrier[1], P. Palestri[2], G. Ghibaudo[1] and L. Selmi[2], *[1]IMEP and [2]Univ. of Udine (France)*	**16:15 C-2-1** Atomically Controlled Hetero-Epitaxy of DO3-type Fe_3Si on Ge(111) Substrate K. Ueda[1], Y. Ando[1], M. Kumano[1], T. Sadoh[1], K. Narumi[2], Y. Maeda[3] and M. Miyao[1], *[1]Kyushu Univ., [2]JAEA and [3]Kyoto Univ. (Japan)*	**16:15 D-2-1 (Invited)** Fabrication of 3-dimensional structure by nanoimprint process Y. Hirai, *Osaka Prefecture Univ. (Japan)*	**16:15 E-2-1 (Invited)** Nanophotonic technologies for PC-SMZ-based all-optical flip-flop Switch: PC-FF Y. Sugimoto[1,2] and K. Asakawa[1], *[1]Univ. of Tsukuba, [2]NIMS (Japan)*
16:35 A-2-2 Direct Evidence of GeO Volatilization from GeO_2 Films and Impact of Its Suppression on GeO_2/Ge MIS Characteristics S. Suzuki, K. Kita, H. Nomura, T. Nishimura and A. Toriumi, *Univ. of Tokyo (Japan)*	**16:45 B-2-2** Influences of Elastic and Inelastic Scatterings on Ballistic Transport in MOSFETs H. Tsuchiya[1], S. Takagi[2,3], *[1]Kobe Univ., [2]MIRAI-ASRC and [3]Univ. of Tokyo (Japan)*	**16:30 C-2-2** MOVPE Condition Dependences of MnAs Nanoclusters Grown on GaInAs (111)A Surfaces H. Iguchi, S. Hara, J. Motohisa and T. Fukui, *Hokkaido Univ. (Japan)*	**16:45 D-2-2** Large Displacement Micro XY-Stage with Paired Moving Plates M. Sasaki[1], F. Bono[2] and K. Hane[2], *[1]Toyota Technological Inst. and [2]Tohoku Univ. (Japan)*	**16:45 E-2-2** Optical-Nonlinearity-Induced Phase Shift via Selective Area Grown InAs-QDs in a Photonic Crystal Waveguide Y. Kitagawa[1], N. Ozaki[1], Y. Takata[1], N. Ikeda[2], S. Ohkouchi[1,3,4], Y. Sugimoto[1,2] and K. Asakawa[1,2], *[1]Univ. of Tsukuba, [2]NIMS, [3]NEC Corp. and [4]AIST (Japan)*
16:55 A-2-3 Experimental Evidence of Coexistence of Interface Traps Interacting with Majority and Minority Carriers in Ge MIS Structures N. Taoka[1], Y. Yamashita[2], M. Harada[2], K. Ikeda[2], T. Yamamoto[2], N. Sugiyama[2] and S. Takagi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo (Japan)*	**17:05 B-2-3** Mobility and Backscattering in Germanium n-type Inversion Layers Q. Rafhay[1,2], P. Palestri[2], D. Esseni[2], R. Clerc[1] and L. Selmi[2], *[1]IMEP and [2]Univ. of Udine (France)*	**16:45 C-2-3** Structure and Magnetic Properties of Gd-doped Gallium Arsenide grown by MBE H. Miyagawa[1], H. Shiraoka[1], S. Higuchi[1], K. Fujii[1], N. Takahashi[1], Y. Watanabe[2], K. Oda[2], N. Tsurumachi[1], S. Nakanishi[1], H. Itoh[1] and S. Koshiba[1], *[1]Kagawa Univ. and [2]Univ. of Tokyo (Japan)*	**17:00 D-2-3** RF-MEMS Switch Structure for Low-Voltage Actuation and High-Density Integration K. Kuwabara[1], N. Sato[1], H. Morimura[1], J. Kodate[1], T. Kamei[2], K. Machida[2] and H. Ishii[1], *[1]NTT Corp. and [2]NTT Advanced Tech. Corp. (Japan)*	**17:00 E-2-3** Imprint Property of Optical Mach-Zehnder Interferometer Using Sputter Deposited (Ba,Sr)TiO_3 at Low Temperature M. Suzuki, K. Nagata and S. Yokoyama, *Hiroshima Univ. (Japan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 4: Advanced Memory Technology**
16:15 F-2-1 Characterization of Zinc Oxide Films Grown by a Newly Developed Plasma Enhanced MOCVD Employing Microwave Excited High Density Plasma H. Asahara[1,2], A. Inokuchi[1,3], K. Watanuki[1,4], M. Hirayama[1], A. Teramoto[1] and T. Ohmi[1], *[1]Tohoku Univ., [2]ROHM Co., Ltd., [3]Tokyo Electron Ltd. and [4]Ube Industries Ltd. (Japan)*	**16:15 G-2-1 (Invited)** Parasitic effects and reliability issues on GaN based HEMTs G. Meneghesso[1], C. Dua[2], M. Peroni[3], M. Uren[4] and E. Zanoni[1], *[1]Univ. of Padova, [2]Alcatel-Thales III-V Lab., [3]Selex-SI and [4]QinetiQ Ltd. (Italy)*	**16:15 H-2-1 (Invited)** Charge Transport through Molecular Wires and Inorganic Nanowires T. Lee, W. K. Hong, G. Jo, T. W. Kim, J. Maeng, H. Song, G. Wang and A. Yoon, *GIST (Korea)*	**16:15 I-2-1 (Invited)** Nanopatterned epitaxial graphene for nano electronics C. Berger, *Georgia Inst. of Tech. (USA)*	**16:15 J-2-1 (Invited)** 3D Device Stacking Technology for Future Memory S. M. Jung, *Samsung Electronics Co., Ltd. (Korea)*
16:30 F-2-2 Dot-height dependence of Photoluminescence from ZnO quantum dots A. Nakamura[1], K. Okamatsu[1], T. Tawara[2], H. Gotoh[2], J. Temmyo[1] and Y. Matsui[3], *[1]Shizuoka Univ., [2]NTT Corp. and [3]NIMS (Japan)*	**16:45 G-2-2** Reduced gate leakage for AlGaN/GaN HEMTs grown on a-plane (11$\bar{2}$0) sapphire S. Lawrence Selvaraj and T. Egawa, *Nagoya Inst. of Tech. (Japan)*	**16:45 H-2-2** Polymer Light-Emitting Diodes Using Poly(9,9-dioctylfuorene) Gel by Thermal Printing Method H. Kajii, D. Kasama and Y. Ohmori, *Osaka Univ. (Japan)*	**16:45 I-2-2** Room Temperature Oscillation in Si/$Si_{1-x}Ge_x$ Resonant Tunneling Diode Y. Suda[1], H. Maekawa[1], N. Asaoka[2] and M. Suhara[2], *[1]Tokyo Univ. of Agri. and Tech. and [2]Tokyo Metropolitan Univ. (Japan)*	**16:45 J-2-2** Improving the Cell Characteristics Using SiN Liner at Active Edge in 4 G NAND Flash D. Kang[1,2], S. Jang[2], K. Lee[2], J. Kim[2], D. Chang[2], H. Kwon[2], W. Lee[2], I. H. Park[1], J. S. Kim[1], J. H. Lee[1], B. G. Park[1], J. D. Lee[1] and H. Shin[1], *[1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)*
16:45 F-2-3 Theoretical Study on Electronic and Electrical Properties of Nano Structural ZnO Z. Zhu, A. Chutia, R. Sahnoun, H. Tsuboi, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*	**17:00 G-2-3** First Operation of AlGaN Channel High Electron Mobility Transistors with Sufficiently Low Resistive Source/Drain Contact formed by Si Ion Implantation T. Nanjo[1], M. Takeuchi[2,3], M. Suita[1], Y. Abe[1], T. Oishi[1], Y. Tokuda[1] and Y. Aoyagi[2,3], *[1]Mitsubishi Electric Corp., [2]RIKEN and [3]Tokyo Tech. (Japan)*	**17:00 H-2-3** Co-doping in Spin-coated Hole Transport Layer for Flexible Organic Light Emitting Diodes S. L. Chen[1], S. H. Wang[1], F. S. Juang[1], Y. S. Tsai[1] and P. H. Yeh[2], *[1]National Formosa Univ. and [2]TPO Displays Corp. (Taiwan)*	**17:00 I-2-3** Direct Observation of Freeze-out Effect in Si by Kelvin Probe Force Microscope M. Ligowski[1,2], R. Nuryadi[1], A. Ichiraku[1], M. Anwar[1], R. Jablonski[2] and M. Tabe[1], *[1]Shizuoka Univ. and [2]Warsaw Univ. of Tech. (Japan)*	**17:05 J-2-3** Nanocrystal floating gate memory devices using atomic layer deposited TiN/Al_2O_3 nanolaminate layers S. Maikap[1], P. J. Tzeng[2], T. Y. Wang[3], H. Y. Lee[2], C. H. Lin[2], S. C. Lo[2], L. S. Lee[2], J. R. Yang[3], M. J. Kao[2] and M. J. Tsai[2], *[1]Chang Gung Univ., [2]Industrial Tech. Research Inst. and [3]National Taiwan Univ. (Taiwan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

17:15 A-2-4
Fabrication of HfO_xN_y Dielectrics on Ge from HfN_x Deposition
T. Maeda[1], Y. Morita[1] and S. Takagi[1,2], *[1]MIRAI, ASRC-AIST and [2]Univ. of Tokyo (Japan)*

17:35 A-2-5
Thermally Robust Germanium MIS Gate Stacks with $LaYO_3$ Dielectric Film
T. Takahashi, Y. Zhao, T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

17:55 A-2-6
Effects of Sulfur Passivation on Ge MOS Capacitors with High-k Gate Dielectric
R. L. Xie, C. X. Zhu, *National Univ. of Singapore (Singapore)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

17:25 B-2-4
Schottky Barrier MOSFETs as Resonant Tunneling Devices
S. Toriyama[1] and N. Sano[2], *[1]Toshiba Corp. and [2]Univ. of Tsukuba (Japan)*

17:45 B-2-5
Coarse-Grain 3D Quantum Simulations of Nanoscale MOSFET
G. Mil'nikov[1], N. Mori[1], Y. Kamakura[1] and T. Ezaki[2], *[1]Osaka Univ. and [2]Hiroshima Univ. (Japan)*

18:05 B-2-6
Multiband Simulation of Uniaxially Stressed Silicon MOSFETs Based on Non-Equilibrium Green's Function Method
H. Fitriawan, S. Souma and M. Ogawa, *Kobe Univ. (Japan)*

Room 201A (C)

Area 12: Spintronic Materials and Devices

17:00 C-2-4
Spin resolved spectroscopy of upper subbands in two-dimensional electron systems by direct transport measurements
Y. Niida[1,2], K. Takashina[1], A. Fujiwara[1], T. Fujisawa[1] and Y. Hirayama[2,3], *[1]NTT Corp., [2]Tohoku Univ. and [3]SORST-JST (Japan)*

17:15 C-2-5
The Reduction of g factor at Different Quantum States
S. M. Huang[1,2], H. Akimoto[1], K. Kono[1], J. J. Lin[2], S. Tarucha[3,4] and K. Ono[1,4], *[1]RIKEN, [2]National Chiao Tung Univ., [3]Univ. of Tokyo and [4]SORST-JST (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

17:15 D-2-4
Performance of Tense Thin Film Torsion Bar for Large-Rotation and Low-Voltage Driving of Micromirror
M. Sasaki[1], S. Yuki[2] and K. Hane[2], *[1]Toyota Technological Inst. and [2]Tohoku Univ. (Japan)*

17:30 D-2-5
Ferrite and copper electroless plating to photopolymerized resin for micro molding of three-dimensional structures
S. Kitayama, T. Yoshimura, S. Maruo and K. Mukai, *Yokohama National Univ. (Japan)*

17:45 D-2-6
Durability of Quartz Mold and Failure Mode Analysis in Imprint Lithography
H. Ooe, T. Kanagawa, T. Hagi and Y. Yoshino, *Murata Manufacturing Co., Ltd. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

17:15 E-2-4 (Invited)
Quantum Confined Ultra-Thin Silicon Light-Emitting Transistor for On-Chip Optical Interconnection
S. Saito, D. Hisamoto, H. Shimizu, H. Hamamura, R. Tsuchiya, Y. Matsui, T. Mine, T. Arai, N. Sugii, K. Torii, S. Kimura and T. Onai, *Hitachi, Ltd. (Japan)*

17:45 E-2-5
Cavity Effect in Nanocrystalline Porous Silicon Ballistic Lighting Device
B. Gelloz, M. Sato and N. Koshida, *Tokyo Univ. of Agri. and Tech. (Japan)*

18:00 E-2-6
Visible Light Emission from Controlled α-Si/SiN Multi-layer Structures
Q. Chen[1], W. K. Tan[1], M. B. Yu[1], L. Ding[2], T. P. Chen[2], G. Q. Lo[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]Nanyang Technological Univ. (Singapore)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

17:00 F-2-4
Defect Passivation by Hydrogen in Zinc Oxide Films Grown by MOCVD
J. Jo[1], O. Seo[2], H. Choi[1] and B. Lee[3], *[1]Ajou Univ., [2]Samsung Advanced Inst. of Tech. and [3]CDA Co., Ltd. (Korea)*

17:15 F-2-5
Development of the multi-scale simulator for the dye-sensitized TiO_2 nanoporous electrode based on quantum chemical calculation
K. Ogiya, C. Lv, R. Sahnoun, M. Koyama, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

17:15 G-2-4
Hot-Carrier Stress Effects on AlGaN/GaN HEMTs Employing 500 °C Oxidized Ni/Au Gate
Y. H. Choi, J. Lim, I. H. Ji, K. H. Cho and M. K. Han, *Seoul National Univ. (Korea)*

17:30 G-2-5
Increase of Breakdown Voltage in AlGaN/GaN HEMTs by Employing As+ Ion Implantation on SiO_2 Passivation Layer
J. Lim[1], Y. H. Choi[1], I. H. Ji[1], K. H. Cho[1], J. Lee[2], W. Jo[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Ewha Womans Univ. (Korea)*

17:45 G-2-6
Enhanced DC Characteristics of Si delta-doped AlGaN/GaN HFETs with p-GaN Backbarrier
H. C. Lee[1], S. Y. Hyun [1], S. W. Yun[1], C. Ostermaier[1], W. Y. Lee[1], J. B. Ha[1], H. I. Cho[1], S. H. Hahm[1], C. K. Hahn[2], H. C. Choi[1] and J. H. Lee[1], *[1]Kyungpook National Univ. and [2]Korea Electronics Tech. Inst. (Korea)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

17:15 H-2-4
Interface Control by Surface-Initiated Deposition Polymerization and its Application to Organic Light Emitting Devices
A. Kawakami[1], K. Katsuki[1], R. C. Advincula[2], K. Tanaka[1] and H. Usui[1], *[1]Tokyo Univ. of Agri. And Tech. and [2]Univ. of Houston (Japan)*

17:30 H-2-5
Multi-Color Panel Based on a White Organic Light Emitting Diode with Color Filter
S. H. Su[1], C. C. Hou[1], H. Tu[1], C. M. Wu[1], G. Y. Lian[1], J. F. Li[2], M. Yokoyama[1] and K. S. Hwang[2], *[1]I-Shou Univ. and [2]National Chung Cheng Univ. (Taiwan)*

17:45 H-2-6
Utilizing Transparent ZnO Thin Film as Permeation-Barrier to Assist Top Emission Polymer Light-Emitting Devices Light Outcoupling and Longevity
Y. H. Lu, Y. H. Liao, C. Y. Shih, Y. C. Huang and K. C. Liu, *Chang Gung Univ. (Taiwan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

17:15 I-2-4
Effect of Size Reduction on Operation Temperature and Switching Power in GaAs-Based Schottky-Wrap-Gate Quantum Wire Transistors
Y. Shiratori and S. Kasai, *Hokkaido Univ. (Japan)*

17:30 I-2-5
Structure, Conductance and Strength of Atomic-Sized Iridium Wires
T. Kizuka and M. Ryu, *Univ. of Tsukuba (Japan)*

17:45 I-2-6
Pulse-controlled electromigration
T. Hayashi and T. Fujisawa, *NTT Corp. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

17:25 J-2-4
Memory Window Enhancement of MOS Memory Devices with High Density Self-Assembled Tungsten Nano-dot
Y. Pei, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. (Japan)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
			Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	
			18:00 D-2-7 Dual-FFPI Temperature Sensor with a Low-Cost LED Light Source M. C. Wang[1], Y. T. Tseng[2], F. G. Tseng[2], J. E. Wang[3] and H. F. Taylor[3], *[1]Ming-Hsin Univ. of Sci. and Tech., [2]National Tsing Hua Univ. and [3]Texas A&M Univ. (Taiwan)*	

18:30-20:30 Banquet/Paper Award & Young Reseacher Award (Multi-Purpose Hall 1F)

Wednesday, September 19

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)

18:30-20:30 Banquet/Paper Award & Young Reseacher Award (Multi-Purpose Hall 1F)

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-3: Reliability-I
(9:00-10:30)
Chairs: J. Yugami (Renesas Tech. Corp.)
Y. Tsunashima (Toshiba Corp.)

9:00 A-3-1(Invited)
A Study of NBTI and PBTI (Charge Trapping) in High k Stacks with NiSi, TiN, Re Gates
S. Zafar, Y. H. Kim, V. Paruchuri, V. Narayanan, B. Doris, A. Callegari, J. Stathis and T. Ning, *IBM (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-3: CMOS Integration
(9:00-10:30)
Chairs: K. Shibahara (Hiroshima Univ.)
H. Wakabayashi (Sony Corp.)

9:00 B-3-1(Invited)
Low Standby Power CMOS Process Integration Scheme for 45-32 nm node
K. Imai, *NEC Electronics Corp. (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-3: Plasma Induced Damage of Low-k Materials
(9:00-10:30)
Chairs: S. Ogawa (Selete)
T. Tatsumi (Sony Corp.)

9:00 C-3-1(Invited)
Generation Mechanism of Etching Damages on Low-k SiOCH Films and Development of Novel Damage Evaluation Technique
M. Hori, *Nagoya Univ. (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

D-3: RF Components
(9:00-10:20)
Chairs: R. Fujimoto (Toshiba Corp.)
T. Hamasaki (Texas Instruments Japan Ltd.)

9:00 D-3-1
A 0.49-6.50 GHz Wideband LC-VCO with High-IRR in a 180 nm CMOS Technology
Y. Kobayashi, K. Ohashi, Y. Ito, H. Ito, K. Okada and K. Masu, *Tokyo Tech. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-3: Special Session: Photonic Crystals and Si Photonics II
(9:00-10:30)
Chairs: O. Wada (Kobe Univ.)
R. Akimoto (AIST)

9:00 E-3-1(Invited)
LSI on-chip optical interconnection with Si nano-photonics
J. Fujikata[1], K. Nishi[1], A. Gomyo[1], J. Ushida[1], T. Ishi[1], H. Yukawa[1], D. Okamoto[1], M. Nakada[1], T. Shimizu[1], M. Kinoshita[1], K. Nose[1], M. Mizuno[1], T. Tsuchizawa[2], T. Watanabe[2], K. Yamada[2], S. Itabashi[2] and K. Ohashi[1], *[1]MIRAI-Selete and [2]NTT Microsystem Integration Labs. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-3: Group-IV Semiconductors I
(9:00-10:15)
Chairs: K. Hiruma (Hokkaido Univ.)
K. Nishi (NEC Corp.)

9:00 F-3-1
Fabrication of 3-D Silicon Micro Probes for Neural Recording Using Multi-Step VLS Growth
A. Ikedo[1], N. Funagayama[1], T. Kawashima[1], H. Takao[1,2], K. Sawada[1,2] and M. Ishida[1,2], *[1]Toyohashi Univ. of Tech. and [2]CREST-JST (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-3: High-Speed Devices and ICs I
(9:00-10:15)
Chairs: S. Yamahata (NTT)
Y. J. Chan (National Central Univ. Taiwan)

9:00 G-3-1(Invited)
Class-F Microwave Amplifier Design Using GaAs-HBT and GaN-HEMT
K. Honjo, R. Ishikawa, T. Yoshida and C. Zheng, *Univ. of Electro-Communications (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-3: Nanowire & Nanotube Sensors
(9:00-10:30)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Cui (Stanford Univ.)

9:00 H-3-1(Invited)
Nanowires for Nanoscale Electronics, Biosensors and Energy Applications
S. Meister, C. K. Chan, H. Peng and Y. Cui, *Stanford Univ. (USA)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-3: Flash Memory II
(9:00-10:20)
Chairs: Y. Shimamoto (Hitachi, Ltd.)
C. Hsu (eMemory Tech. Inc.)

9:00 J-3-1
2-bit/cell Characteristics of High-Density and High-Performance SONOS Flash Memory Cell with Recessed Channel Structure
K. R. Han, Y. M. Kim, K. H. Park, S. G. Jung, B. K. Choi and J. H. Lee, *Kyungpook National Univ. (Korea)*

Thursday, September 20

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

9:30 A-3-2
Comprehensive Understanding of PBTI and NBTI reliability of High-k / Metal Gate Stacks with EOT Scaling to sub-1nm
M. Sato[1], K. Yamabe[2], K. Shiraishi[2], S. Miyazaki[3], K. Yamada[4], C. Tamura[2], R. Hasunuma[2], S. Inumiya[1], T. Aoyama[1], Y. Nara[1] and Y. Ohji[1], *[1]Selete, [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Waseda Univ. (Japan)*

9:50 A-3-3
Performance and Reliability Improvement by Optimized Nitrogen Content of TaSiNx Metal Gate in Metal/ HfSiON nFETs
T. Onizawa, M. Sato, T. Aoyama, T. Eimori, Y. Nara and Y. Ohji, *Selete (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

9:30 B-3-2
High Performance and Low Leakage CMOS for 45nm Low Power Technology and Beyond
J. P. Han[1], Y. M. Lee[2], H. Utomo[3], R. Lindsay[1], M. Eller[1], J. C. Kim[4], V. Sardesai[3], V. Chan[3], S. Fang[3], J. Holt[3], T. N. Adam[3], H. Zhuang[1], W. Wille[3], Z. Lun[2], H. Wang[3], T. Dyer[3], J. Yan[1], O. J. Kwon[3], O. S. Kwon[1], C. W. Lai[2], T. J. Tang[2], S. S. Tan[2], J. Yuan[3], J. Li[3], H. Ng[3], H. Shang[3], J. Sudijono[2], D. Schepis[3], M. Ieong[3], Y. Li[3], J. H. Ku[4], A. Gutmann[1] and M. Hierlemann[1], *[1]Infineon Technologies AG, [2]Chartered Semiconductor Manufacturing Ltd., [3]IBM and [4]Samsung Electronics Co., Ltd. (USA)*

9:50 B-3-3
In-Depth Study of Two-Dimensional Layout Dependences in Multiple-Stressor CMOS for 45 nm Technology Node High-Performance Applications
T. Miyashita[1], J. Ogura[2], T. Owada[2], T. Sakuma[1], H. Nomura[2], H. Miyaoka[2], A. Hasegawa[2], S. Yamaguchi[2] and S. Satoh[1], *[1]Fujitsu Labs. Ltd. and [2]Fujitsu Ltd. (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

9:30 C-3-2
Impact of Barrier Metal Sputtering on Low-k SiOCH Films with Various Chemical Structures
N. Inoue, N. Furutake, F. Ito, H. Yamamoto, T. Takeuchi and Y. Hayashi, *NEC Corp. (Japan)*

9:50 C-3-3
Process Induced Damage Analysis of Low-k SiOCH Films Focusing on Siloxane Network and Methyl End Group
S. Nakao, K. Kinoshita and S. Ogawa, *Selete (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

9:20 D-3-2
Evaluation of Digital Crosstalk Noise on a Differential Input VCO
A. Toya[1], Y. Murasaka[2], T. Ohmoto[2] and A. Iwata[1,2], *[1]Hiroshima Univ. and [2]A-R-Tec Corp. (Japan)*

9:50 D-3-3
A New Symmetric Inductor Model for RF Circuits under Single-end and Differential Operations
J. C. Guo and T. Y. Tan, *National Chiao Tung Univ. (Taiwan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

9:30 E-3-2
A Study on the Design and Properties of an SiON/SiO_2 Waveguide: The Effect of the Substrate on Propagation Loss
J. Ushida[1], A. Gomyo[1], J. Fujikata[1], D. Okamoto[1], K. Nishi[1], K. Ohashi[1], T. Watanabe[2], T. Tsuchizawa[2], K. Yamada[2] and S. Itabashi[2], *[1]MIRAI-Selete and [2]NTT Microsystem Integration Labs. (Japan)*

9:45 E-3-3
Proposal of a Silicon Optical Modulator Based on Inversion-Carrier Absorption
T. Hirata, K. Kajikawa, T. Tabei and H. Sunami, *Hiroshima Univ. (Japan)*

Thursday, September 20

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:15 F-3-2
Demonstration of holes in strained Ge quantum wells with much higher drift mobility and density than that of electrons in strained Si channels
M. Myronov[1], K. Sawano[1], K. M. Itoh[2] and Y. Shiraki[1], *[1]Musashi Inst. of Tech. and [2]Keio Univ. (Japan)*

9:30 F-3-3
Pulsed Laser Irradiation of Silicon-Germanium-on-Insulator ($Si_{0.17}Ge_{0.83}OI$) Substrates for Strain Relaxation and Defect Reduction
G. H. Wang[1], E. H. Toh[1], X. Wang[2], K. M. Hoe[3], S. Tripathy[1], G. Q. Lo[3], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Singapore Inst. of Manufacturing Tech. and [3]Inst. of Microelectronics (Singapore)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

9:30 G-3-2
High-Performance InGaAs/InP Composite-Channel High Electron Mobility Transistors Grown by Metal Organic Vapor-Phase Epitaxy
H. Sugiyama[1], T. Kosugi[1], H. Yokoyama[1], K. Murata[1], Y. Yamane[2], M. Tokumitsu[1] and T. Enoki[1], *[1]NTT Corp. and [2]NTT Electronics Corp. (Japan)*

9:45 G-3-3
Low Power Consumption and Low Noise InGaP/GaAs HBT MMIC Amplifier for Full-Band UWB Receiver
R. Ishikawa[1], T. Abe[1], M. Shimada[2] and K. Honjo[1], *[1]Univ. of Electro-Communications and [2]NANOTECO Corp. (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

9:30 H-3-2
Electrical Sensing of Calcium Ions using Silicon Nanowire Array
A. Agarwal[1], W. L. Wong[1,2], K. L. Yang[2], S. Balakumar[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore (Singapore)*

9:45 H-3-3
Fabrication of vertically-aligned CNT electrodes using plasma-enhanced CVD for chemical sensors
Y. Kojima, S. Kishimoto, M. Okochi, H. Honda and T. Mizutani, *Nagoya Univ. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

9:20 J-3-2
ESR and PL Study of Charge Trapping Centers in Silicon Nitride Films and Its Verification with Novel ONO-Sidewall 2-bit/cell Nonvolatile Memory
A. Toki[1], N. Shinohara[1], M. Nakano[2], H. Kotaki[2] and Y. Kamigaki[1], *[1]Kagawa Univ. and [2]Sharp Corp. (Japan)*

9:40 J-3-3
ONO Thickness Dependency of Complementary Bit Disturb in SONOS-type Nonvolatile Memory
K. Kikuchi, *Spansion Japan Ltd. (Japan)*

Thursday, September 20

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

10:10 A-3-4
nMOSFET Reliability Improvement attributed to the Interfacial Dipole formed by La Incorporation in HfO_2
C. Y. Kang[1], P. kirsch[2], D. Heh[1], C. Young[1], P. Sivasubramani[1], G. Bersuker[1,] S. C. Song[1], R. Choi[1], B. H. Lee[2], J. Lichtenwalner[3], J. S. Jur[3], A. I. Kingon[3] and R. Jammy[2], *[1]SEMATECH, [2]IBM Assignee and [3]North Carolina State Univ. (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

10:10 B-3-4
Is a "Power Optimized" Roadmap Realistic for High Performance Applications?
F. Boeuf and T. Skotnicki, *STMicroelectronics (France)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

10:10 C-3-4
Plasma Cure Process for Porous SiOCH Films using CF_4 Gas
K. Tomioka, J. Nakahira, S. Kondo, S. Ogawa and S. Saito, *Selete (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

10:10 D-3-4
Thick Au High-Q Inductor and Its Chip-on-Chip Bonding on an RF IC for Various Frequencies
J. Kodate[1], K. Kuwabara[1], N. Sato[1], H. Morimura[1], K. Kudou[2], K. Machida[2] and H. Ishii[1], *[1]NTT Corp. and [2]NTT AT (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

10:00 E-3-4
Photoelastic Effect in Silicon Ring Resonator
Y. Amemiya, Y. Tanushi, T. Tokunaga and S. Yokoyama, *Hiroshima Univ. (Japan)*

10:15 E-3-5
Magneto-optic Effect in Amorphous $Bi_3Fe_5O_{12}$ Waveguide Sputtered at Room Temperature
H. Taura, Y. Shishido, Y. Tanushi, T. Tokunaga and S. Yokoyama, *Hiroshima Univ. (Japan)*

Break

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Short Presentation P-1 (10:45-12:15) Chair: H. Fukutome (Fujitsu Labs. Ltd.)	Short Presentation P-3 (10:45-12:15) Chair: S. Hayashi (Matsushita Electric Industrial Co., Ltd.)	Short Presentation P-2 and P-12 (10:45-12:15) Chair: S. Ogawa (Selete)	Short Presentation P-5 and P-11 (10:45-12:15) Chairs: R. Fujimoto (Toshiba Corp.) H. Tabata (Univ. of Tokyo)	Short Presentation P-7 (10:45-12:15) Chair: M. Sugawara (Fujitsu Labs. Ltd.)

Thursday, September 20

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:45 F-3-4
Strain-Relaxed $Si_{1-x}Ge_x$ and Strained Si Grown by Sputter Epitaxy
H. Hanafusa[1], Y. Suda[1], A. Kasamatsu[2], N. Hirose[2], T. Mimura[2] and T. Matsui[2], *[1]Tokyo Univ. of Agri. and Tech. and [2]NICT. (Japan)*

10:00 F-3-5
A Novel Approach to Fabricate ～ 120 nm Thick Fully Relaxed Ge-on-Insulator
S. Balakumar[1], K. M. Hoe[1], W. Tang[1], Y. L. Foo[2], S. Tripathy[2], C. H. Tung[1], G. Q. Lo[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]Inst. of Materials Research and Engineering (Singapore)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

10:00 G-3-4
Ku-band Compact Multi-layer Monolithic Microwave Digital Attenuator using InP/InGaAs PIN Diodes
H. Eom, J. G. Yang, S. Choi and K. Yang, *KAIST (Korea)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

10:00 H-3-4
Comparison of Top gate Structures for Carbon Nanotube Field Effect Transistor Biosensor
M. Abe[1,2], K. Murata[1,2,3], T. Ataka[1,2] and K. Matsumoto[2,3,4,5], *[1]Olympus Corp., [2]NEDO, [3]CREST-JST, [4]AIST and [5]Osaka Univ. (Japan)*

10:15 H-3-5
Development of gas sensors based on tungsten oxide nanowires in a metal/SiO_2/metal structure and their sensing responses to NO_2
R. M. Ko[1], Z. F. Wen[1], S. J. Wang[1], J. K. Lin[1], G. H. Fan[1], W. I. Shu[1] and B. W. Liou[2], *[1]National Cheng Kung Univ. and [2]WuFeng Inst. of Tech. (Taiwan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

10:00 J-3-4
Ramping Amplitude Multi-Frequency Charge Pumping Technique for Silicon-Oxide-Nirtride-Oxide-Silicon Flash EEPROM Cell Transistors
W. H. Choi[1], H. S. Joo[1], I. S. Han[1], S. S. Park[1], H. M. Kwon[1], T. G. Goo[1], O. S. Yoo[1], M. K. Na[1], J. C. Om[2], S. S. Lee[2], G. H. Bae[2], H. D. Lee[1] and G. W. Lee[1], *[1]Chungnam National Univ. and [2]Hynix Semiconductor Inc. (Korea)*

Break

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Short Presentation P-8 (10:45-12:15) Chair: H. Yamaguchi (NTT Corp.)	Short Presentation P-6 (10:45-12:15) Chair: M. Kuzuhara (Univ. of Fukui)	Short Presentation P-10 and P-13 (10:45-12:15) Chairs: T. Kamata (AIST) K. Matsumoto (Osaka Univ.)	Short Presentation P-9 (10:45-12:15) Chair: Y. Takahashi (Hokkaido Univ.)	Short Presentation P-4 (10:45-12:15) Chair: I. Asano (Elpida Memory, Inc.)

POSTER SESSION (13:00-15:00, Multi Purpose Hall)

P1
Advanced Gate Stack / Si Processing Science
(23 Papers)

P-1-1
Real-time monitoring of initial oxidation of Si(110)-16×2 Surface by Si 2p Photoemission spectroscopy
Y. Yamamoto[1], H. Togashi[1], A. Kato[1], S. Hasegawa[1], S. Goto[1], T. Nakano[1], M. Suemitsu[1], Y. Narita[2], A. Yoshigoe[3] and Y. Teraoka, *[1]Tohoku Univ., [2]Kyushu Inst. of Tech. and [3]JAEA (Japan)*

P-1-2
Si Oxidation Mechanism in Ar/O_2 Surface Wave Plasma
K. Takeda, S. Takashima and M. Hori, *Nagoya Univ. (Japan)*

P-1-3
A lithographical method by oxidization through a conductive template in contact with a silicon substrate mediated by a thin water layer
C. H. Hsieh, J. D. Liao, C. S. Kuo, C. Y. Huang and B. H. Wu, *National Cheng Kung Univ. (Taiwan)*

P-1-4
Pr-Oxide-Based Dielectric Films on Ge Substrates
M. Sakashita, N. Kito, A. Sakai, H. Kondo, O. Nakatsuka, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*

P-1-5
Physical and Electrical Properties of Addition Ti into Er_2O_3 Gate Dielectrics
T. M. Pan, W. H. Hsu, C. C. Huang, W. S. Huang, K. C. Huang and J. L. Hong, *Chang Gung Univ. (Taiwan)*

P-1-6
In-Situ Fluorinated Low-Temperature Polycrystalline Silicon (LTPS) Thin-Film Transistors (TFT) with Low Trapping and Off Current by CF_4 Plasma
W. H. Sung[1], C. H. Kao[1], H. K. Peng[1], S. F. Huang[2], W. F. Tsai[2], C. F. Ai[2], C. R. Chen[3] and C. S. Lai, *[1]Univ. of Chang Gung, [2]Inst. of Nuclear Energy Research and [3]Corp. of Material Sci. Service (Taiwan)*

P-1-7
Improvement of Electrical Characteristics for Novel Fluorine-Incorporated Poly-Si TFTs with TiN Gate Electrode and Pr_2O_3 Gate Dielectric
C. W. Chang[1], J. J. Huang[1], H. R. Chang[1], J. W. Lee[2] and T. F. Lei[1], *[1]National Chiao Tung Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*

P-1-8
Nanoscale-order Homogeneous Structure of SiO_2 Film on Poly-silicon Grown at Room Temperature using UV Light Excited Ozone
N. Kameda[1,2], T. Nishiguchi[1,2], Y. Morikawa[1], M. Kekura[1], H. Nonaka[2] and S. Ichimura[2], *[1]Meidensha Corp. and [2]AIST (Japan)*

P-1-9
Robust High-κ HfO_xN_y n-MOSFETs Using Low Work Function TbN Gate
N. C. Su, C. H. Wu, S. J. Wang, C. K. Chiang, and C. C. Cheng, *National Cheng Kung Univ. (Taiwan)*

P-1-10
Crystalline and electrical properties of mictamict TiSiN gate MOS capacitors
K. Furumai, H. Kondo, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*

P-1-12
Galvanic Corrosion Suppression of High-k/Metal Gates using Organic Solvent based HF
D. Watanabe, H. Aoki, S. Hotta, C. Kimura and T. Sugino, *Osaka Univ. (Japan)*

P-1-13
Dual Metal Gate MOSFETs with Symmetrical Threshold Voltages Using Work Function Tuned Ta/Mo Bi-layer Metal Gates
T. Matsukawa, Y. X. Liu, K. Endo, M. Masahara, Y. Ishikawa, H. Yamauchi, J. Tsukada, K. Ishii and E. Suzuki, *AIST (Japan)*

P-1-14
TiN Gate Work Function Control Using Nitrogen Gas Flow Ratio and RTA-Temperature
Y. X. Liu[1], T. Hayashida[2], T. Matsukawa[1], K. Endo[1], M. Masahara[1], S. O'uchi[1], K. Sakamoto[1], K. Ishii[1], J. Tsukada[1], Y. Ishikawa[1], H. Yamauchi[1], A. Ogura[2] and E. Suzuki[1], *[1]AIST and [2]Meiji Univ. (Japan)*

P-1-15
Reduced Interfacial Layer Thickness and Gate Leakage Current of ALD Grown HfAlO with TaN Gates using Chemical Oxides and Spike-Annealing
Y. J. Lee[1], B. A. Tsai[2], H. Y. Peng[1], C. P. J. Tzeng[3] and K. S. Chang-liao[2], *[1]National Nano Device Labs., [2]National Tsing Hua Univ. and [3]Industrial Tech. Research Inst. (Taiwan)*

P-1-16
Full Range Work Function Modulation by Nitrogen Incorporation in Hf-Mo Binary Alloys Gate Electrode
C. S. Lai[1], C. W. Huang[1], H. K. Peng[1], C. H. Chen[1], Y. C. Fang[2], L. Hsu[2], H. C. Wang[2], C. Y. Lee[3] and S. J. Lin[3], *[1]Chang Gung Univ., [2]Chung-Shan Inst. and [3]Nanya Tech. Corp. (Taiwan)*

P-1-17
Quantitative Characterization of Plasma-Induced Defect Generation Process in Exposed Thin Si Surface Layers
K. Eriguchi, A. Ohno, D. Hamada, M. Kamei, H. Fukumoto and K. Ono, *Kyoto Univ. (Japan)*

P-1-18
Pulsed Focused-Laser Beam Annealing of Ultra-Shallow Implanted Silicon and In Situ Dopant Activation Monitoring
W. S. Yoo and K. Kang, *WaferMasters, Inc. (USA)*

P-1-19
UV-VIS Raman Characterization of High Dose Ultra Shallow Implanted Silicon before and after Excessive Annealing
T. Sasaki[1], H. Minami[1], K. Kisoda[2], W. S. Yoo[3], M. Yoshimoto[1] and H. Harima[1], *[1]Kyoto Inst. of Tech., [2]Wakayama Univ. and [3]WaferMasters, Inc. (Japan)*

P-1-20
Activation of Implanted Phosphorus Atoms in Silicon Wafers by Infrared Semiconductor Laser Annealing Using Carbon Films as Optical Absorption Layers
N. Sano[1], T. Sameshima[2], Y. Matsuda[3] and Y. Andoh[3], *[1]Hightec Systems Corp., [2]Tokyo Univ. of Agri. and Tech. and [3]Nissin Ion Equipment Co., Ltd. (Japan)*

P-1-21
Effect of Ion Implantation on Dislocation Motion in SiGe/Si Heterostructures
A. Hara, *Tohoku-Gakuin Univ. (Japan)*

P-1-22
Schottky Barrier Height Modulation for Nickel Silicide on n-Si (100) using Antimony Segregation
H. S. Wong, L. Chan, G. Samudra and Y. C. Yeo, *National Univ. of Singapore (Singapore)*

P-1-23
In-situ Doped Si Selective Epitaxial Growth for Raised Source/Drain Extension CMOSFET
T. Ikuta[1,2], Y. Miyanami[1], S. Fujita[1], H. Iwamoto[1], S. Kadomura[1], T. Shimura[2], H. Watanabe[2] and K. Yasutake[2], *[1]Sony Corp. and [2]Osaka Univ. (Japan)*

P-1-24
Top-view imaging of 65 nm gate length metal-oxide-semiconductor field effect transistors by scanning capacitance microscopy
Y. Naitou[1], A. Ando[1], H. Ogiso[1], S. Kamohara[2], F. Yano[2] and A. Nishida[2], *[1]AIST and [2]MIRAI-Selete (Japan)*

P2
Characterization and Materials Engineering for Interconnect Integration
(12 Papers)

P-2-1
Low Dielectric Constant Non-Porous Fluorocarbon Films for Inter-Layer Dielectric
A. Itoh[1,2], A. Inokuchi[1,3], S. Yasuda[1], A. Teramoto[1], T. Goto[1], M. Hirayama[1] and T. Ohmi[1], *[1]Tohoku Univ., [2]ZEON Corp. and [3]Tokyo Electron Inc. (Japan)*

P-2-2
The Evaluation of New Amorphous Hydrocarbon Film aCHx, for Copper Barrier Dielectric Film in Low-k Copper Metallization
H. Ishikawa[1,2], T. Nozawa[1], T. Matsuoka[1], A. Teramoto[2], M. Hirayama[2], T. Ito[2] and T. Ohmi[2], *[1]Tokyo Electron Ltd. and [2]Tohoku Univ. (Japan)*

P-2-3
Effects of vapor phase transport synthesis on the properties of porous silica films
Y. Cho[1], T. Seo[1], K. Kohmura[2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Mitsui Chemicals, Inc. (Japan)*

P-2-4
Integration of MIM Capacitors on BCB with Thin-Film MCM-D Technology
J. Maeng[1], S. Song[1], C. S. Yoo[1], H. Lee[2] and K. Seo[1], *[1]Seoul National Univ. and [2]Samsung Electronics Co., Ltd. (Korea)*

P-2-5
Novel Ta-Precursors for the CVD and ALD of TaN_x diffusion barrier layers
M. Pokoj, I. Németh, K. Volz, D. Gaess, A. Merkoulov, J. Sundermeyer and W. Stolz, *Philipps Univ. (Germany)*

P-2-7
Characterization of Strain in Si for High Performance MOSFETs
D. Kosemura[1], Y. Kakemura[1], T. Yoshida[1], A. Ogura[1], M. Kohno[2], T. Nishita[2] and T. Nakanisi[2], *[1]Meiji Univ. and [2]Tokyo Electron AT Ltd. (Japan)*

P-2-8
Raman Spectroscopic Study for Determining Stress Component in Single Crystal Silicon Microstructure using Multivariate Analysis
N. Naka[1], S. Kashiwagi[1], Y. Nagai[2], T. Namazu[2], S. Inoue[2] and K. Ohtsuki[1], *[1]HORIBA, Ltd. and [2]Univ. of Hyogo (Japan)*

P-2-9
Characterization of Patterned Oxide Buried in Bonded Silicon-on-Insulator Wafers by Near-Infrared Scattering Topography and Microscopy
X. Wu[1,2], J. Uchikoshi[1], T. Hirokane[1], R. Yamada[1], K. Arima[1] and M. Morita[1], *[1]Osaka Univ. and [2]Xi'an Jiaotong Univ. (Japan)*

P-2-10
Simulation and fabrication of embedded capacitors in the multilayer printed circuit board
H. W. You and J. H. Koh, *Kwangwoon Univ. (Korea)*

P-2-11
Non-destructive extraction of width bias variations for deep sub-micron interconnect lines
M. C. Tang, M. F. Wang, T. Cheng, D. Chen, C. S. Yeh and S. C. Chien, *UMC (Taiwan)*

P-2-13
SAW Bumpless Bonding at Low Temperature in Ambient Air
Y. H. Wang[1], T. Sato[2], T. Sugiura[2] and T. Suga[1], *[1]Univ. of Tokyo and [2]Samsung Yokohama Research Inst. (Japan)*

P-2-14
Void Free Room Temperature Silicon Direct Bonding by Sequential Plasma Activated Process
C. Wang, E. Higurashi and T. Suga, *Univ. of Tokyo (Japan)*

P3
CMOS Devices /Device Physics
(23 Papers)

P-3-1
Impact of Zr/Hf Ratio on Reliability of $HfZrO_x$ Gate Dielectric
J. C. Liao[1], Y. K. Fang[1], Y. T. Hou[2], W. H. Tseng[2], J. Y. Yang[2], P. F. Hsu[2], Y. S. Chao[2], K. C. Lin[2], K. T. Huang[2], T. L. Lee[2] and M. S. Liang[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd., (Taiwan)*

P-3-2
Current Transportation Mechanism of HfO_2 Gate Dielectrics with Silicon Surface Fluorine Implantation (SSFI) in CMOS Application
W. C. Wu[1], C. S. Lai[2], T. M. Wang[2], J. C. Wang[3], M. W. Ma[1] and T. S. Chao[1], *[1]National Chiao Tung Univ., [2]Chang Gung Univ. and [3]Nanya Tech. Corp. (Taiwan)*

P-3-4
Performance Comparison of Ultra-thin FD-SOI Inversion-, Intrinsic- and Accumulation-Mode MOSFETs
R. Kuroda[1,2], A. Teramoto[1], S. Sugawa[1] and T. Ohmi[1], *[1]Tohoku Univ. and [2]JSPS Research Fellow(DC1) (Japan)*

P-3-5
In-situ Comparison of Si/High-K and Si/SiO_2 interface properties in FD SOI MOSFETs operated at low temperature
L. Pham-Nguyen[1,2], C. Fenouillet-Beranger[3], S. Cristoloveanu[1], A. Vandooren[2], M. Orlowski[2] and G. Ghibaudo[1], *[1]IMEP, [2]Freescale Semiconductors and [3]STMicroelectronics (France)*

P-3-6
Impact of Gate Overlap on the Performance of Schottky Barrier MOSFETs including GIBL Effect
L. Zeng, Z. L. Xia, G. Du, J. F. Kang, R. Q. Han and X. Y. Liu, *Peking Univ. (China)*

P-3-7
SiGe Recessed Source-Drain (RSD) Stressors for PMOS: Effect of Device Integration Flow and Increased Ge Content on Electrical Performance
V. Machkaoutsan[1], P. Verheyen[2], P. Tomasini[3], G. Eneman[2,4,5], R. Loo[2], P. Absil[2], S. G. Thomas[3], J. P. Lu[6], J. W. Weijtmans[7] and R. Wise[7], *[1]ASM Belgium N.V., [2]IMEC, [3]ASM America Inc., [4]Catholic Univ. of Leuven, [5]Fund for scientific research Flanders, [6]Texas Instruments assignee to IMEC and [7]Texas Instruments (Belgium)*

P-3-8
Combined Effects of an Epitaxial Ge Channel and Si Substrate on Ge-on-Si MOS Capacitors and Field Effect Transistors
J. Oh[1], P. Majhi[1], H. Lee[2,4], S. H. Lee[2], S. Banerjee[2], P. Kalra[3], R. Harris[1], H. H. Tseng[1] and R. Jammy[1], *[1]SEMATECH, [2]Univ. of Texas at Austin, [3]Univ. of California Berkeley and [4]Chungnam National Univ. (USA)*

P-3-9
Investigation of Impact Ionization in Strained-Si nMOSFETs
T. K. Kang[1], Y. H. Sa[1], P. C. Huang[2], S. L. Wu[1] and S. J. Chang[2], *[1]Cheng Shiu Univ. and [2]National Cheng Kung Univ. (Taiwan)*

P-3-10
Impact of Strain on Ballistic Current in Si n-i-n Structures
H. Minari and N. Mori, *Osaka Univ. (Japan)*

P-3-11
Effect of STI Stress Enhanced Boron Diffusion on Leakage and Vcc_min of Sub-65nm node Low-Power SRAM
T. H. Lee[1], Y. K. Fang[1], T. Lin[1], E. Hsu[2], T. Sheng[2], C. L. Kuo[2], O. Cheng[2] and S. C. Chien[2], *[1]National Cheng Kung Univ. and [2]UMC (Taiwan)*

P-3-12
Impacts of SiN Deposition Conditions on NMOSFETs
C. S. Lu[1], K. H. Chan[1], H. C. Lin[1,2] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

P-3-13
The Effect of Etch Stop Layer Stress on Negative Bias Temperature Instability of Deep Submicron p-MOSFETs
M. S. Chen[1], Y. K. Fang[1], T. H. Lee[1], C. T. Lin[1], J. Ko[2], Y. K. Sheu[2], T. L. Shen[2] and W. L. Liao[2], *[1]National Cheng Kung Univ. and [2]UMC (Taiwan)*

P-3-14
New Observation of NBTI Degradation and Recovery Effect of Plasma Nitrided Oxide in Nano Scale PMOSFETs
I. S. Han[1], H. H. Ji[2], T. G. Goo[1], O. S. You[1], W. H. Choi[1], M. K. Na[1], Y. G. Kim[2], S. H. Park[2], H. S. Lee[2], Y. S. Kang[2], D. B. Kim[2] and H. D. Lee[1], *[1]Chnugnam National Univ. and [2]MagnaChip Semiconductor Inc. (Korea)*

P-3-16
Effects of hot carriers on DC and RF performances of deep submicron PMOSFET for low-power and high frequency applications
M. C. Tang[1], Y. K. Fang[1], D. Chen[2], C. S. Yeh[2] and S. C. Chien[2], *[1]National Cheng Kung Univ. and [2]UMC (Taiwan)*

P-3-18
Investigation of Random Dopant Fluctuation for Multi-Gate MOSFETs Using Analytical Solution of 3-D Poisson's Equation
Y. S. Wu and P. Su, *National Chiao Tung Univ. (Taiwan)*

P-3-19
Accurate Extraction of Mobility, Effective Channel Length and Source/Drain Resistance in 60 nm MOSFETs
J. Kim, J. Lee, Y. Yun, B. G. Park, J. D. Lee and H. Shin, *Seoul National Univ. (Korea)*

P-3-20
Determining the Gate-Finger Width for the Minimum Gate Resistance in RF MOSFETs
Y. Jeong, I. M. Kang, J. Lee and H. Shin, *Seoul National Univ. (Korea)*

P-3-21
Non-Quasi-Static Small-Signal Model of RF MOSFETs Valid up to 110 GHz
I. M. Kang, Y. Yoon, J. D. Lee and H. Shin, *Seoul National Univ. (Korea)*

P-3-22
Spatial Distribution of Channel Thermal Noise in Short-Channel MOSFETs
J. Jeon, Y. Yun, B. G. Park, J. D. Lee and H. Shin, *Seoul National Univ. (Korea)*

P-3-23
Impacts of Body Contact Structures on SOI NMOSFET DC, RF and $1/f$ Noise Characteristics
R. Yang[1,2], Y. Z. Xiong[1], J. L. Shi[1], H. Qian[2], J. F. Li[2], J. Fu[1], W. Y. Loh[1], M. B. Yu[1], G. Q. Lo[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]IMECAS (Singapore)*

P-3-24
Mechanism and Reliability Index of Hot-Carrier Degradation in LDMOS Transistors
K. S. Tian[1], J. F. Chen[1], W. C. Wang[1], S. Y. Chen[1], K. M. Wu[2], J. R. Lee[1], C. M. Liu[2] and S. L. Hsu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*

P-3-25
Anomalous Hot-Carrier-Induced On-Resistance Degradation in High-Voltage LDMOS Transistors
S. Y. Chen[1], J. F. Chen[1], K. M. Wu[2], J. R. Lee[1], C. M. Liu[2] and S. L. Hsu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*

P-3-26
Analysis of Temperature Effects on the High-Frequency Characteristics of RF LDMOS Transistors
H. H. Hu[1], K. M. Chen[2], G. W. Huang[2], C. Y. Chang[1], Y. C. Lu[3], Y. C. Yang[3] and E. Cheng[3], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]UMC (Taiwan)*

P4
Advanced Memory Technology
(7 Papers)

P-4-1
Effect of nano-grain on the memory characteristics of high-κ HfAlO charge trapping layers for nano-scale non-volatile memory device applications
T. Y. Wang[1], S. Maikap[2], P. J. Tzeng[3], D. Panda[2], L. S. Lee[3], M. J. Tsai[3] and J. R. Yang[1], *[1]National Taiwan Univ., [2]Chang Gung Univ. and [3]Industrial Tech. Research Inst. (Taiwan)*

P-4-2
An Improved Low Voltage Programming Scheme Using Forward Bias Assisted Drain Avalanche Induced Hot Electron Injection on P-Channel EEPROMs
Y. H. Huang and S. S. Chung, *National Chiao Tung Univ. (Taiwan)*

P-4-3
Electronic characteristics of charge trapping memory using Al_2O_3 dielectric
Y. J. Seo[1], K. C. Kim[1], H. D. Kim[1], M. S. Joo[2], Y. T. Kim[2], S. H. Pyi[2], H. Y. Cho[3] and T. G. Kim[1], *[1]Korea Univ., [2]Hynix Semiconductor Inc. and [3]Dongguk Univ. (Korea)*

P-4-4
Low temperature Poly-Si TFT nonvolatile memory devices with In_2O_3 nano-particles embedded in polyimide
H. M. Koo[1], D. U. Lee[2], S. P. Kim[2], E. K. Kim[2], J. Jung[3] and W. J. Cho[1], *[1]Kwangwoon Univ., [2]Hanyang Univ. and [3]Sejong Univ. (Korea)*

P-4-5
Si Quantum Dot TFT Nonvolatile Memory for System-On-Panel Applications
W. Yong[1], M. B. Yu[2], R. Yang[2], W. Y. Loh[2], J. Fu[1,2], C. Zhu[1], G. Q. Lo[2], N. Balasubramanian[2] and D. L. Kwong[2], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

P-4-6
Effect of $Ni_{1-x}Pt_x$ Alloy Electrode on the Improved Resistive Switching Characteristics of NiO Thin Films
C. B. Lee, B. S. Kang, M. J. Lee, S. E. Ahn, G. Stefanovich, W. Xianyu, K. H. Kim, H. Yin, Y. Park and I. K. Yoo, *Samsung Advanced Inst. of Tech. (Korea)*

P-4-7
Resistance Switching of HfO_2 Film and Its Application to Non-Volatile Memory
J. Lee, I. S. Park, J. Park, K. J. Jung, S. Lee and J. Ahn, *Hanyang Univ. (Korea)*

P5
Advanced Circuits and Systems
(10 Papers)

P-5-1
Delay-Compensation Flip-Flops for Timing-Error Tolerant Circuit Design
K. Hirose, Y. Manzawa, M. Goshima and S. Sakai, *Univ. of Tokyo (Japan)*

P-5-2
Tungsten Through-Si Via (TSV) Technology for Three-Dimensional LSIs
H. Kikuchi[1], Y. Yamada[1], A. M. Ali[1,2], J. Liang[1], T. Fukushima[1], T. Tanaka[1] and M. Koyanagi[1], *[1]Tohoku Univ. and [2]Assiut Univ. (Japan)*

P-5-4
CMOS Voltage Reference Based on the Threshold Voltage of a MOSFET
K. Ueno, T. Hirose, T. Asai and Y. Amemiya, *Hokkaido Univ. (Japan)*

P-5-5
High-Q Resonator on Thin-Film Substrate for mm-wave System-on-Package (SOP)
S. Song and K. Seo, *Seoul National Univ. (Korea)*

P-5-6
Through-Only De-embedding for On-Chip Symmetric Devices
Y. Goto and M. Fujishima, *Univ. of Tokyo (Japan)*

P-5-7
Wideband CMOS Transimpedance Amplifier Design Using Transformer-Peaking Technique
J. D. Jin and S. S. H. Hsu, *National Tsing Hua Univ. (Taiwan)*

P-5-8
A Compact and Power-Efficient Implementation of Rank Order Filters Using Time-Domain Digital Computation Technique
L. T. Nguyen, K. Ito and T. Shibata, *Univ. of Tokyo (Japan)*

P-5-9
A Compact Bell-Shaped Analog Matching Cell Module for Digital-Memory-Based Associative Processors
T. T. Bui and T. Shibata, *Univ. of Tokyo (Japan)*

P-5-10
UWB Transmission Characteristics of Bow-tie Antennas on Si
S. Kubota, X. Xiao, K. Kimoto and T. Kikkawa, *Hiroshima Univ. (Japan)*

P-5-11
A Compact Balanced Filter on Thin Film Substrate for mmWave application
C. S. Yoo[1,2], J. M. Maeng[1], S. S. Song[1], H. S. Lee[3], W. S. Lee[2], N. K. Kang[2] and K. S. Seo[1], *[1]Seoul National Univ., [2]Korea Electronics Tech. Inst. and [3]Samsung Electronics Co., Ltd. (Korea)*

P6
Compound Semiconductor Circuits, Electron Devices and Device Physics
(9 Papers)

P-6-1
Dependence of Carrier Lifetime in InAlAs/InGaAs HEMTs on Gate-to-Source Voltage
H. Taguchi, T. Sato, M. Oura, T. Iida and Y. Takanashi, *Tokyo Univ. of Sci. (Japan)*

P-6-2
Feasibility Study of ZnO-Based FBAR Devices for Mobile WiMAX Applications
L. Mai, J. Lee, V. Pham and G. Yoon, *Information and Communications Univ. (Korea)*

P-6-3
Optimum Rapid Thermal Activation for Mg-doped p-type GaN
M. Nagamori[1], S. Ito[1], H. Saito[1], K. Shiojima[1], S. Yamada[2], N. Shibata[2] and M. Kuzuhara[1], *[1]Univ. of Fukui and [2]Toyoda gosei Corp. (Japan)*

P-6-4
Effects of High-*k* Passivation Films on AlGaN/GaN HEMT
S. Yagi[1], M. Shimizu[1], H. Okumura[1], H. Ohashi[1], K. Arai[1], Y. Yano[2] and N. Akutsu[2], *[1]AIST and [2]Taiyo Nippon Sanso Corp. (Japan)*

P-6-5
High performance 50 nm $In_{0.65}Al_{0.35}As/In_{0.75}Ga_{0.25}As$ Metamorphic HEMTs with Si_3N_4 passivation on thin InGaAs/InP layer
S. J. Yeon, J. Seong, M. Park and K. Seo, *Seoul National Univ. (Korea)*

P-6-6
High-speed and Low-Power SCFL-Type NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology
H. Kim, S. Yeon and K. Seo, *Seoul National Univ. (Korea)*

P-6-8
High performance 70 nm $In_{0.8}$ GaP/$In_{0.4}$ AlAs/$In_{0.35}$ GaAs Metamorphic HEMT With Pd Schottky Contacts
S. Kim, Y. Koh and K. Seo, *Seoul National Univ. (Korea)*

P-6-9
The Impact of Mixed-mode Electrical Stress on High-Frequency and RF Power Characteristics of SiGe HBTs
S. Y. Huang[1], C. C. Hung[1], W. S. Liao[1], C. Y. Lin[1], C. W. Fan[1], C. Y. Tzeng[1], V. Liang[1], K. M. Chen[2] and C. Y. Chang[3], *[1]UMC, [2]National Nano Device Labs. and [3]National Chiao Tung Univ. (Taiwan)*

P-6-10
Hydrogen-Sensing Behaviors of an InAlAs-Based Schottky Diode with a Pt Catalytic Thin Film
C. W. Hung, H. I. Chen, T. P. Chen, T. H. Tsai and W. C. Liu, *National Cheng Kung Univ. (Taiwan)*

P7
Photonic Devices and Device Physics
(13 Papers)

P-7-1
InGaAs/InP p-i-n Photodiode with Extrinsic Pad Isolation Structure
M. Kim, *Kongju National Univ. (Korea)*

P-7-2
Anomalous Electroluminescence Phenomena in InGaN/GaN Multiple Quantum Well Light-emitting Diodes with Electron Tunneling Layer
H. Y. Chen[1], Y. F. Chen[1], W. T. Su[1], K. Y. Cheng[1], J. C. Wang[1], H. T. Shen[1], T. E. Nee[1] and Y. F. Wu[2], *[1]Chang Gung Univ. and [2]Tech. and Sci. Inst. of Northern Taiwan (Taiwan)*

P-7-3
Quaternary AlInGaN Solar Blind UV Detectors with Photo-CVD SiO_2 Cap Layers
C. H. Chen, *Cheng Shiu Univ. (Taiwan)*

P-7-4
Steep On-Off Ratio of Photocurrent through Metal-Oxide-Semiconductor Tunneling Structures
R. Yamada, H. Hashimoto, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ. (Japan)*

P-7-6
GaN Metal-Semiconductor-Metal Photodetectors with an un-activated Mg-doped GaN Cap Layer
P. C. Chang[1], Y. C. Wang[2], K. H. Lee[2], C. L. Yu[2] and S. J. Chang[2], *[1]Nan Jeon Inst. of Tech. and [2]National Cheng Kung Univ. (Taiwan)*

P-7-7
Ion Beam Deposition of Quantum Dots from Colloidal Solution
Y. Tani, S. Kobayashi and H. Kawazoe, *HOYA Corp. (Japan)*

P-7-8
A High Performance Photodetector Suitable for Visible Light and Near IR Applications
K. S. Lai, J. C. Huang and K. Y. J. Hsu, *National Tsing Hua Univ. (Taiwan)*

P-7-9
Experimental and Theoretical Examination of Field Emission in Surface Conduction Electron-Emitter Displays
H. Y. Lo[1], Y. Li[1], C. H. Tsai[1], H. Y. Chao[1], F. M. Pan[1], M. C. Chiang[2] and C. N. Mo[2], *[1]National Chiao Tung Univ. and [2]Chunghwa Picture Tubes, Ltd. (Taiwan)*

P-7-12
Dispersion relations of localized surface plasmon polaritons in a plasmonic thermal emitter
Y. H. Ye, M. W. Tsai, C. Y. Chen, J. W. Jiang, Y. T. Chang and S. C. Lee, *National Taiwan Univ. (Taiwan)*

P-7-13
A study of deposition single crystal SiCN thin film on porous silicon for ultraviolet light detecting applications
T. H. Chou[1], Y. K. Fang[1], T. W. Kuo[1], D. H. Jaw[2], F. S. Lai[2], J. F. Huang[2] and J. S. Shie[2], *[1]National Cheng Kung Univ. and [2]Wufeng Inst. of Tech. (Taiwan)*

P-7-14
Mechanism investigation of $(NH_4)_2S_x$ -treated III — V compounds multi-junction solar cell
L. W. Lai, J. T. Chen and C. T. Lee, *National Cheng Kung Univ. (Taiwan)*

P-7-15
GaN Ultraviolet MSM Photodetectors by capping a Low-Temperature AlN Layer
K. H. Lee[1], P. C. Chang[2], Y. C. Wang[1], C. L. Yu[1] and S. J. Chang[1], *[1]National Cheng Kung Univ. and [2]Nan Jeon Inst. of Tech. (Taiwan)*

P-7-16
GaInNAs/GaAs p-i-n Photodetector with Multiquantum Well Structure
Y. F. Chen[1], W. C. Chen[1], R. W. Chuang[1], Y. K. Su[1] and H. L. Tsai[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*

P8
Advanced Material Synthesis and Crystal Growth Technology
(17 Papers)

P-8-1
Self organized Micro Cones on Si substrate by Microwave Plasma Chemical Vapor Deposition
M. Moriya, Y. Matsumoto, Y. Mizugaki, T. Kobayashi and K. Usami, *Univ. of Electro-Communications (Japan)*

P-8-2
Facile Fabrication of Gold Nanoparticle -Titanium Oxide Multilayer Assemblies by Surface Sol-Gel Processes
T. Kawahara, T. Arakawa, T. Akiyama and S. Yamada, *Kyushu Univ. (Japan)*

P-8-3
Vanadium Dioxide Films Deposited on SiO_2- and Al_2O_3-coated Si Substrates Using Reactive RF-Magnetron Sputter Deposition Technique
S. J. Yun, J. W. Lim, B. G. Chae and H. T. Kim, *Electronics and Telecommunications Research Inst. (Korea)*

P-8-4
Lateral Recrystallized Si Thin Films with Large Tensile Strain for High Performance Thin Film Transistors
S. Fujii, S. Kuroki, Z. Xiaoli, M. Numata, K. Kotani and T. Ito, *Tohoku Univ. (Japan)*

P-8-5
High-Performance LTPS-TFTs Fabricated by Continuous Wave Laser Annealing
C. C. Tsai[1], K. F. Wei[1], Y. J. Lee[2], J. L. Wang[1], I. C. Lee[1] and H. C. Cheng[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

P-8-6
Growth of GaNAs films with As_2 source in atomic hydrogen-assisted molecular beam epitaxy
A. Takata, R. Oshima and Y. Okada, *Univ. of Tsukuba (Japan)*

P-8-7
High Quality Crack-Free GaN-Based Epitaxy on Patterned Si(111) Substrate
S. J. Lee, G. H. Bak, S. R. Jeon, S. H. Lee, S. Kim, S. H. Jeong and J. H. Baek, *KOPTI (Korea)*

P-8-8
MOVPE Growth of M-Plane GaN Using $LiAlO_2$ Substrates
Y. K. Su, A. T. Cheng, W. C. Lai and Y. Z. Chen, *National Cheng Kung Univ. (Taiwan)*

P-8-9
The Elimination of Inversion Domains in MBE-GaN Grown Using Low Temperature Nitridation
J. C. Chang, T. H. Yang, S. G. Shen, Y. C. Chen, J. T. Ku and C. Y. Chang, *Nation Chiao Tung Univ. (Taiwan)*

P-8-10
Growth and Characterization of GaN Nano-column Grown on Gallium Coated Si by Molecular Beam Epitaxy
K. Santhakumar[1], D. W. Kim[1], D. H. Kang[1], D. W. Kim[2] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Chungnam National Univ. (Korea)*

P-8-11
Electron transport at InGaN/electrolyte interface and its application to water photolysis using visible light
S. Usui[1], T. Narumi[1], J. Tokue[1], N. Kobayashi[1], J. Yamamoto[2], Y. Ban[2] and K. Wakao[2], *[1]Univ. of Electro-Communications and [2]Nippon EMC. Ltd. (Japan)*

P-8-12
Fabrication and Characterization of $In_xGa_{1-x}N$ Quantum Dots using NNAD Growth Technique
D. H. Kang[1], D. W. Kim[1], S. H. Lee[1], S. J. Lee[2], J. S. Kim[1], K. Santhakumar[1] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Korea Photonics Tech. Inst. (Korea)*

P-8-13
Growth of InN on patterned sapphire substrates and its characterization
H. Song, D. H. Kang, J. C. Song, E. S. Jang, I. H. Lee, K. Santhakumar, D. W. Kim and C. R. Lee, *Chonbuk National Univ. (Korea)*

P-8-14
Fabrication and characteristics of the low resistivity p-type ZnO thin films by nitrogen ion implantation
S. Y. Tsai[1], Y. M. Lu[2] and M. H. Hon[1], *[1]National Cheng Kung Univ. and [2]National Univ. of Tainan (Taiwan)*

P-8-15
Stability of Phosphorus-doped *p*-ZnO thin films
J. K. Kim[1,2], J. W. Lim[2], H. T. Kim[2], S. H. Kim[2] and S. J. Yun[1,2], *[1]Univ. of Sci. and Tech. and [2]Electronics and Telecommunications Research Inst. (Korea)*

P-8-16
Properties of Zinc Oxide Films Cosputtered with Various Aluminum Contents at Room Temperature
D. S. Liu[1], C. W. Sheu[1], F. C. Tsai[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ. (Taiwan)*

P-8-17
Activation of Nitrogen-acceptors in Al-N Codoped Zinc Oxide Films Prepared by Radio Frequency Magnetron Cosputtering Technology
D. S. Liu[1], C. Y. Wu[1], C. S. Shei[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ. (Taiwan)*

P9
Physics and Applications of Novel Functional Materials and Devices
(14 Papers)

P-9-1
Control of electrostatic coupling observed for Si double quantum dot structures
G. Yamahata[1], Y. Tsuchiya[1,3], S. Oda[1,3] and H. Mizuta[1,2,3], *[1]Tokyo Tech., [2]Univ. of Southampton and [3]SORST-JST (Japan)*

P-9-2
Electrically detected exciton photo-absorption in semiconductor double quantum dot
K. Takahashi[1], K. Kono[1], S. Tarucha[2], H. Kosaka[2,3] and K. Ono[1,4], *[1]RIKEN, [2]Univ. of Tokyo, [3]Tohoku Univ. and [4]CREST-JST (Japan)*

P-9-3
Transient Behavior of Germanium Quantum-dot Resonant Tunneling Diode
W. T. Lai and P. W. Li, *National Central Univ. (Taiwan)*

P-9-4
Magneto-capacitance measurement of a selectively doped n-AlGaAs/GaAs heterojunction with InGaAs quantum dots
T. Kawazu[1] and H. Sakaki[1,2], *[1]NIMS and [2]Toyota Technological Inst. (Japan)*

P-9-5
Fabrication of InGaN/GaN Multiple Quantum Wells Nanopillars by Focused Ion Beam Milling
S. E. Wu, T. H. Hsueh, C. P. Liu, J. K. Sheu, W. C. Lai and S. J. Chang, *National Cheng Kung Univ. (Taiwan)*

P-9-6
A Physics-based Compact Model for I-MOS Transistors
C. Shen[1], E. H. Toh[1], J. Lin[1], C. H. Heng[1], D. Sylvester[2], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Univ. of Michigan (Singapore)*

P-9-7
Development of a Seebeck Coefficient Prediction Simulator Using Tight-Binding Quantum Chemical Molecular Dynamics
H. Tsuboi, K. Ogiya, A. Chutia, Z. Zhu, C. Lv, R. Sahnoun, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*

P-9-8
Programmable VO_2 temperature sensor controlled by a constant voltage
B. J. Kim, Y. W. Lee, S. Choi, B. G. Chae, S. J. Yun and H. T. Kim, *Electronics and Telecommunications Research Inst. (Korea)*

P-9-9
Chemical Bonding Self-Organizations in Non-crystalline Hf Si Oxynitride Dielectrics: Low Direct Tunneling and Defect Levels Comparable to SiO_2
S. Lee[1], H. Seo[1], G. Lucovsky[1] and J. C. Phillips[2], *[1]North Carolina Statre Univ. and [2]Rutgers Univ. (USA)*

P-9-10
Novel Vacuum Encapsulation Applied for Improving Short-Channel Immunity on Poly-Si Thin Film Transistors
T. C. Liao[1], C. Y. Wu[1], S. W. Tu[1], F. T. Chien[2], W. K. Lin[1], J. C. Liu[1], H. W. Chen[1], C. C. Lin[1] and H. C. Cheng[1], *[1]National Chiao Tung Univ. and [2]Feng Chia Univ. (Taiwan)*

P-9-11
A Quasi-planar Thin Film Field Emission Diode
K. C. Lin, H. W. Chen, R. L. Lai, C. P. Juan, Y. Y. Hsu and H. C. Cheng, *National Chiao Tung Univ. (Taiwan)*

P-9-12
Dopant Dependency of Nickel Silicide and Its Improvement Utilizing Ni-Pd(5%) on SOI Substrate for Nano-scale CMOSFET
S. Y. Jung[1], Y. Y. Zhang[1], Z. Zhong[1], S. G. Li[1], K. Y. Park[1], Y. C. Kim[2], G. W. Lee[1], J. S. Wang[1] and H. D. Lee[1], *[1]Chungnam National Univ. and [2]Korea Univ. of Tech. and Education (Korea)*

P-9-13
Abrupt metal insulator transition of TiO_2 and $Al_xTi_{1-x}O_y$ thin films
J. W. Lim, S. J. Yun, Y. W. Lee, B. J. Kim and H. T. Kim, *ETRI (Korea)*

P-9-14
Current and Speed Enhancements at 90nm Node through Package Strain
W. S. Liao[1], S. Y. Huang[1], T. Shih[1] and C. W. Liu[2], *[1]UMC and [2]National Taiwan Univ. (Taiwan)*

P10
Organic Materials Science, Device Physics, and Applications
(10 Papers)

P-10-1
Applications of PVA/PAA proton exchange membrane in fuel cell
P. C. Kuo, D. S. Wu, L. L. Wang, M. Y. Shia and H. H. Yu, *National Formosa Univ. (Taiwan)*

P-10-2
Novel Sub-10nm Polymer Thin Film Resistance Switching Device
D. Lee, S. Choi, M. Ree and O. Kim, *Pohang Univ. of Sci. and Tech. (Korea)*

P-10-3
Electrical Conducting Properties of Amorphous Carbon Nanowhiskers Studied by In Situ High-Resolution Transmission Electron Microscopy
R. Kato[1], K. Miyazawa[2] and T. Kizuka[1], *[1]Univ. of Tsukuba and [2]NIMS (Japan)*

P-10-4
Lateral Carrier Transport in Pentacene Polycrystalline Films-Hole Transport Barrier and Effective Mass in Crystals –
R. Matsubara, N. Ohashi, M. Sakai, K. Kudo and M. Nakamura, *Chiba Univ. (Japan)*

P-10-5
Low-Voltage Operation of Organic Thin Film Transistors by using Dual Gate Dielectrics
S. B. Kong and C. K. Song, *Dong-A Univ. (Korea)*

P-10-6
Fabrication and characterization of poly (3-hexylthiophene)-based field-effect transistors with silsesquioxane gate insulators
K. Tomatsu[1], T. Hamada[1,4], T. Nagase[1,4], T. Kobayashi[1,4], S. Murakami[2,4], K. Matsukawa[3,4] and H. Naito[1,4], *[1]Osaka Prefecture Univ., [2]TRI-Osaka, [3]Osaka Municipal Technical Research Inst. and [4]JST (Japan)*

P-10-7
Organic Thin Film Transistors fabricated by All Solution Processes
S. K. Ahn and C. K. Song, *Dong-A Univ. (Korea)*

P-10-8
Fully Self-Aligned Organic Field-Effect Transistors
K. Nomura, S. Naka and H. Okada, *Univ. of Toyama (Japan)*

P-10-9
Observation of Carrier Behavior in Organic Field Effect Transistor with Electroluminescence under AC Electric Field
Y. Ohshima, H. Kohn, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

P-10-10
The Study of Organic Light Emitting Diode with a Doped Electron Transport Layer
C. C. Hou, R. S. Shieh, S. H. Su, C. M. Wu and M. Yokoyama, *I-Shou Univ. (Taiwan)*

P11
Micro/Nano Electromechanical and Bio-Systems (Devices)
(10 Papers)

P-11-1
Development of Power Supply System for Three-Dimensionally Staked Retinal Prosthesis Chip
K. Komiya, R. Kobayashi, T. Kobayashi, K. Sato, T. Fukushima, H. Tomita, H. Kurino, T. Tanaka, M. Tamai and M. Koyanagi, *Tohoku Univ. (Japan)*

P-11-2
Immobilization of Protein Molecules on Step-Controlled Sapphire Surfaces and Characterization of the Adhesion Forces
R. Aoki[1], T. Arakawa[1], T. Oya[1] and T. Ogino[1,2], *[1]Yokohama National Univ. and [2]CREST-JST (Japan)*

P-11-3
Tracking of Cell Adhesion Process to Self-Assembled Monolayer of Alkanethiols with Various Functional Groups
Y. Arima and H. Iwata, *Kyoto Univ. (Japan)*

P-11-4
Self-spreading Behavior of Supported Lipid Bilayer through Single Sub-100-nm Gap
Y. Kashimura, J. Durao, K. Furukawa and K. Torimitsu, *NTT Corp. (Japan)*

P-11-5
A Novel High-k Y_2O_3 Sensing Membrane for pH-ISFET
T. M. Pan, K. M. Liao, J. C. Lin, C. H. Cheng, Z. W. Lin and C. J. Chang, *Chang Gung Univ. (Taiwan)*

P-11-6
The Development of Oligonucleotide Micro Array Detecting System
J. Z. Tsai, C. J. Chen, K. H. Shiue, Z. C. Liu, W. Y. Chen and Y. M. Hsin, *National Central Univ. (Taiwan)*

P-11-7
Vibration Evaluation and Gas Transfer of Distilled Water and Bovine Blood in Intravascular Lung Assist Device using PZT Actuator
G. B. Kim[1], C. U. Hong[1], M. H. Kim[1], S. J. Kim[2] and H. S. Kang[1], *[1]Chonbuk National Univ. and [2]Iksan National Collage (Korea)*

P-11-9
Effect of Rise Time on Atmospheric Plasma generated using Micro-triode
J. Kim, K. Kim, S. Jin and Y. Kim, *Hong-ik Univ. (Korea)*

P-11-10
Pulsating Tension Fatigue Testing of Single and Poly-Crystalline Silicon Microstructures for Silicon MEMS
T. Namazu, Y. Nagai and S. Inoue, *Univ. of Hyogo (Japan)*

P-11-11
Novel inorganic pH-insensitive membrane prepared by post N_2O plasma treatment on conventional Si_3N_4/SiO_2 stack layer for REFET application
T. C. Wang[1], T. F. Lu[1], C. H. Chin[1], C. E. Lue[1], C. M. Yang[1], Y. C. Fang[2], L. Hsu[2], H. C. Wang[2] and C. S. Lai[1], *[1]Chang Gung Univ. and [2]Chung-Shan Inst. (Taiwan)*

P12
Spintronic Materials and Devices
(3 papers)

P-12-1
Hydrogenation Induced Room-Temperature Ferromagnetism in Co-doped ZnO Nanocrystals
Y. Wang, L. Sun, Y. Li, Y. Zhang, D. Han, L. Liu, J. Kang, X. Zhang and R. Han, *Peking Univ. (China)*

P-12-2
Design of Reconfigurable Logic Circuits based on Single-Layer Magnetic-Tunnel-Junction Elements
S. Lee, G. Lee, H. Lee, S. Lee and H. Shin, *Ewha W. Univ. (Korea)*

P-12-3
Appearance of Variable-Range-Hopping Conduction and Enhanced Spin Dependent Transport by Low Temperature Heat Treatment for Magnetite Nanoparticle Sinter
H. Kobori[1], K. Ohnishi[1], A. Sugimura[1] and T. Taniguchi[2], *[1]Konan Univ. and [2]Osaka Univ. (Japan)*

P13
Applications of Nanotubes and Nanowires
(11 paper)

P-13-1
ZnO Nanowire-Based CO Sensors Prepared at Various Temperatures
T. J. Hsueh[1], S. J. Chang[1], C. L. Hsu[2] and I. C. Chen[3], *[1]National Cheng Kung Univ., [2]National Univ. of Tainan and [3]Industrial Tech. Research Inst. (Taiwan)*

P-13-2
Effects of Cu Catalyst and Water Vapor on the Growth of Ge-GeO_x Core-Shell Nanowires via the Carbothermal Reduction of GeO2 Powders
W. L. Lo, T. J. Hsu and W. T. Lin, *National Cheng Kung Univ. (Taiwan)*

P-13-3
Band-Gap Tuning of an Individual Single-Walled Carbon Nanotube with Uniaxial Strain
H. Maki[1], T. Sato[1] and K. Ishibashi[2], *[1]Keio Univ. and [2]RIKEN (Japan)*

P-13-4
Synthesis of VO_2 Nanowire and Observation of the Metal-Insulator Transition
S. Choi, B. J. Kim, Y. W. Lee, S. J. Yun and H. T. Kim, *ETRI (Korea)*

P-13-5
Band Structure of Surface Terminated Silicon Nanowire
S. You, M. Gao and Y. Wang, *Tsinghua Univ. (China)*

P-13-6
CNT-FETs with High Modulated Drain Current utilizing Size-classified Fe Particles as a Catalyst
I. Soga[1,2], M. Norimatsu[1,2], D. Kondo[1,2], Y. Yamaguchi[1,2,3], S. Sato[1,2], T. Iwai[1,2,3] and Y. Awano[1,2,3], *[1]Fujitsu Labs. Ltd., [2]Fujitsu Ltd. and [3]CREST-JST (Japan)*

P-13-7
Design of Vertical Nanowire FETs
L. E. Wernersson, *Lund Univ. (Sweden)*

P-13-8
In Situ Transmission Electron Microscopy of Deformation of Crystalline C_{60} Nanotubes
K. Saito[1], R. Kato[1], K. Miyazawa[2] and T. Kizuka[1], *[1]Univ. of Tsukuba and [2]NIMS (Japan)*

P-13-9
Growth of vertical GaN Nano-Column on Au Droplet/Si (111) Substrate using Pulsed Flow MOCVD Method
J. C. Song[1], S. H. Lee[1], H. Song[1], S. J. Lee[2], J. S. Kim[1], K. Santhakumar[1] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Korea Photonics Tech. Inst. (Korea)*

P-13-10
Internal Structure of Vertically Aligned Single-Walled Carbon Nanotube Arrays
E. Einarsson, T. Yamamoto, Y. Ikuhara and S. Maruyama, *Univ. of Tokyo (Japan)*

P-13-11
Control of Electric Conduction of Carbon Nanowalls
W. Takeuchi[1], M. Ura[1], Y. Tokuda[2], M. Hiramatsu[3], H. Kano[4] and M. Hori[1], *[1]Nagoya Univ., [2]Aichi Inst. of Tech., [3]Meijo Univ. and [4]NU Eco-Engineering Co., Ltd. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-5: Junction
(15:15-16:25)
Chairs: B. Mizuno (Ultimate Junction Technologies Inc.)
H. Fukutome (Fujitsu Labs. Ltd.)

15:15 A-5-1(Invited)
Study of Dopant Diffusion and Defect Evolution for Advanced Ultra Shallow Junctions based on Atomistic Modeling
T. Noda[1], W. Vandervorst[2], S. Felch[3], V. Parihar[3], C. Vrancken[2], S. Severi[2], T. Y. Hoffmann[2], A. Falpin[2], B. van Daele[2], T. Jannssens[2], H. Bender[2], P. Eyben[2], M. Niwa[1], R. Schreutelkamp[3], F. Nouri[3], P. P. Absil[2], M. Jurczak[2], K. De Meyer[2] and S. Biesemans[2], *[1]Matsushita Electric Industrial Co., Ltd., [2]IMEC and [3]AMAT (Japan)*

15:45 A-5-2
Electron Holography Characterization of Ultra-Shallow Junctions in 30-nm Gate-length MOS-FETs
N. Ikarashi[1], M. Oshida[1], M. Miyamura[1], M. Saitoh[1], A. Mineji[2] and S. Shishiguchi[2], *[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-5: Mobility Characterization
(15:15-16:35)
Chairs: Y. Kamakura (Osaka Univ.)
K. Takeuchi (NEC Corp.)

15:15 B-5-1
Experimental Study of Uniaxial Stress Effects on Coulomb-limited Electron and Hole Mobility in Si-MOSFETs
S. Kobayashi, M. Saitoh, Y. Nakabayashi and K. Uchida, *Toshiba Corp. (Japan)*

15:35 B-5-2
Physical Mechanism for Hole Mobility Enhancement in (110)-Surface Strained-Si/Strained-SiGe Structures with Anisotropic/Biaxial Strain
T. Mizuno[1,3], T. Irisawa[2], N. Hirashita[2], Y. Moriyama[2], T. Tezuka[2], N. Sugiyama[2] and S. Takagi[1,4], *[1]MIRAI-AIST, [2]MIRAI-ASET, [3]Kanagawa Univ. and [4]Univ. of Tokyo (Japan)*

Room 201A (C)

Area 12: Spintronic Materials and Devices

C-5: Symposium on Magnetic Tunnel Junctions and Beyond
(15:15-16:45)
Chairs: M. Tanaka (The Univ. of Tokyo)
K. Ando (AIST)

15:15 C-5-1(Invited)
Spin Transfer Torque RAM (STT-RAM) Technology
Y. Huai, Z. Diao, Y. Ding, A. Panchula, S. Wang, Z. Li, D. Apalkov, X. Luo, H. Nagai, A. Driskill-Smith and E. Chen, *Grandis, Inc. (USA)*

15:45 C-5-2(Invited)
Structural Study on CoFeB/MgO/CoFeB Magnetic Tunnel Junctions
K. Tsunekawa[1,2], Y. Choi[1], Y. Nagamine[1], H. Maehara[1], D. D. Djayaprawira[1], T. Takeuchi[2] and Y. Kitamoto[2], *[1]Canon ANELVA Corp. and [2]Tokyo Tech. (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

D-5: RF CMOS Circuits and Systems
(15:15-16:15)
Chairs: K. Masu (Tokyo Tech.)
T. Matsuoka (Osaka Univ.)

15:15 D-5-1(Invited)
RF CMOS Circuits-Overview and Perspective
T. Tsukahara, *Univ. of Aizu (Japan)*

15:45 D-5-2(Invited)
Compensation techniques for integrated analog device issues
A. Matsuzawa, *Tokyo Tech. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-5: Special Session: Photonic Crystals and Si Photonics III
(15:15-16:30)
Chairs: M. Tokushima (NEC Corp.)
O. Wada (Kobe Univ.)

15:15 E-5-1
Thermal Modulation of Group Delay of Pillar-Photonic-Crystal Waveguide
M. Tokushima, *NEC Corp. (Japan)*

15:30 E-5-2(Invited)
Plasmonic Crystals and Nanophotonic Sensing Devices
T. A. Kelf[1], Y. Sugawara[2], R. M. Cole[3], N. M. B. Perney[3], J. J. Baumberg[3], M. E. Abdelsalam[3] and P. N. Bartlett[3], *[1]Hokkaido Univ., [2]FUJIFILM Corp. and [3]Univ. of Southampton (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-5: Group-IV Semiconductors II
(15:15-16:30)
Chairs: K. Nishi (NEC Corp.)
H. Yamaguchi (NTT Basic Research Labs.)

15:15 F-5-1(Invited)
Bottom-up approach for the nanopatterning of Si(001)
R. Koch, *Johannes Kepler Univ. (Austria)*

15:45 F-5-2
Plasma Deposition of HfO_2 and TiO_2 onto Plasma-Nitrided Ge Surfaces
S. Lee[1], G. Lucovsky[1], J. P. Long[1] and J. Lüning[2], *[1]North Carolina State Univ. and [2]Stanford Synchrotron Research Lab. (USA)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-5: High-Speed Devices and ICs II
(15:15-16:15)
Chairs: S. Kuroda (Eudyna Devices Inc.)
K. Maezawa (Univ. of Toyama)

15:15 G-5-1
A 7.6-ps Pulse Generator Using 0.13-μm InP-based HEMTs for Ultra Wide-Band Impulse Radio Systems
Y. Nakasha[1], Y. Kawano[1], T. Suzuki[1], T. Ohki[2], T. Takahashi[1], K. Makiyama[1], T. Hirose[2] and N. Hara[1], *[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd. (Japan)*

15:30 G-5-2
Novel MOBILE Circuits Using 3 RTDs Operating up to 12.5 Gb/s
H. Kim, N. Jeon and K. Seo, *Seoul National Univ. (Korea)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-5: Nanowire Growth and Devices I
(15:15-16:30)
Chairs: J. Motohisa (Hokkaido Univ.)
T. Fukui (Hokkaido Univ.)

15:15 H-5-1(Invited)
III-V semiconductor hetero-structure nanowires by selective area MOVPE
T. Fukui, S. Hara and J. Motohisa, *Hokkaido Univ. (Japan)*

15:45 H-5-2
InP Nodes in GaP-based Free-standing Nanowires on Si(111)
K. Tateno, G. Zhang, T. Sogawa and H. Nakano, *NTT Corp. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-5: PRAM
(15:15-16:25)
Chairs: M. Moniwa (Renesas Technology Corp.)
I. Asano (Elpida Memory, Inc.)

15:15 J-5-1(Invited)
Current Status and Future View of Phase Change Memory
Y. Matsui, *Hitachi, Ltd. (Japan)*

15:45 J-5-2
Three-Dimensional Electro-Thermal Compact Model for Reset Operation of Phase Change Memories
A. Sakai, K. Sonoda, M. Moniwa, K. Ishikawa, O. Tsuchiya and Y. Inoue, *Renesas Tech. Corp. (Japan)*

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 12: Spintronic Materials and Devices**		**Area 7: Photonic Devices and Device Physics**
16:05 A-5-3 $Si_{1-x}Ge_x$/Si Selective Etch with HCl for Thin Si-Channel Transistors Integration N. Loubet[1], S. Denorme[1], A. Pouydebasque[2], F. Leverd[1], P. Gouraud[1], C. Tallaron[1], T. Skotnicki[1] and D. Dutartre[1], *[1]STMicroelectronics and [2]NXP Semiconductors (France)*	**15:55 B-5-3** Behavior of Low-Temperature Phonon-Limited Electron Mobility of Double-Gate Field-Effect Transistor with (111) Si Surface Channel T. Yamamura, S. Sato and Y. Omura, *Kansai Univ. (Japan)*	**16:15 C-5-3(Invited)** Giant TMR in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions S. Ikeda[1], J. Hayakawa[2,1], Y. M. Lee[1,3], K. Miura[2,1], R. Sasaki[1], F. Matsukura[1], T. Meguro[1] and H. Ohno[1], *[1]Tohoku Univ., [2]Hitachi, Ltd. and [3]Fujitsu Labs. Ltd. (Japan)*		**16:00 E-5-3** Application of Surface-Plasmon Antenna to Near-Infrared Photodetectors for Optical Communication D. Okamoto, J. Fujikata, K. Nishi and K. Ohashi, *NEC Corp. (Japan)*
	16:15 B-5-4 Mobility Degradation in (110)-Oriented Ultra-thin Body Double-Gate pMOSFETs with SOI Thickness of less than 5nm K. Shimizu and T. Hiramoto, *Univ. of Tokyo (Japan)*			**16:15 E-5-4** Cavity mode in trilayer Ag/SiO_2/Au plasmonic thermal emitter M. W. Tsai, Y. W. Jiang, C. Y. Chen, Y. H. Ye and S. C. Lee, *National Taiwan Univ. (Taiwan)*

Break

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 13: Applications of Nanotubes and Nanowires**		**Area 4: Advanced Memory Technology**
16:00 F-5-3 A Novel Process-Compatible Floating Channel Crystallization Technique to Fabricate High-Performance Poly-Si TFTs C. W. Chang[1], J. W. Lee[2], C. L. Chang[1] and T. F. Lei[1], *[1]National Chiao Tung Univ. and [2]TSMC (Taiwan)*	**15:45 G-5-3** Ultra-Short Pulse Generators Using Resonant Tunneling Diodes and Their Integration with Antennas on Ceramic Substrates N. Kamegai[1], S. Kishimoto[1], K. Maezawa[2], T. Mizutani[1], H. Andoh[3], K. Akamatsu[4] and H. Nakata[4], *[1]Nagoya Univ., [2]Univ. of Toyama, [3]Toyota National College of Tech. and [4]Nippon Mining & Metals Co., Ltd. (Japan)*	**16:00 H-5-3** CMOS Compatible Si-Nanowire Inverter Logic Gate for Low Power Applications N. Singh, K. D. Buddharaju, S. C. Rustagi, S. H. G. Teo, A. Agarwal, L. Y. Wong, L. J. Tang, C. H. Tung, J. Yu, G. Q. Lo, N. Balasubramanian and D. L. Kwong, *Inst. of Microelectronics (Singapore)*		**16:05 J-5-3** Comprehensive HSPICE Model of Phase Change Memory Cell for Static and Transient Programming D. S. Chao[1, 2], Y. K. Chen[3], Y. B. Liao[3], M. H. Chiang[3], C. Lien[2], M. J. Kao[1] and M. J. Tsai[1], *[1]EOL/ITRI, [2]National Tsing Hua Univ. and [3]National Ilan Univ. (Taiwan)*
16:15 F-5-4 Low Temperature Ultra-thin Hafnium Oxide Dielectrics by Sputtering of Hf Metal on Tilted Substrate Followed by Nitric Acid Oxidation then Anodization Compensation in D. I. Water C. H. Chang and J. G. Hwu, *National Taiwan Univ. (Taiwan)*	**16:00 G-5-4** High Tuning-Range VCO Using a Gated Tunnel Diode M. Ärlelid, M. Nilsson, G. Astromskas, E. Lind and L. E. Wernersson, *Lund Univ. (Sweden)*	**16:15 H-5-4** Silicon Nanowire Schottky Barrier NMOS Transistors E. J. Tan[1,2,3], K. L. Pey[1], N. Singh[2], G. Q. Lo[2], D. Z. Chi[3], K. M. Hoe[2], P. S. Lee[1] and G. D. Cui[1], *[1]Nanyang Technological Univ., [2]Inst. of Microelectronics and [3]Inst.of Materials Research and Engineering (Singapore)*		

Break

Thursday, September 20

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-6: Reliability-II
(16:45-18:05)
Chairs: K. Shiraishi (Univ. of Tsukuba)
Y. Nara (Selete)

16:45 A-6-1
Effects of O_2 Plasma Treatment on the Reliabilities of Metal Gate/High-k Dielectric MOSFETs
K. T. Lee[1,5], C. Y. Kang[2], R. Choi[2], S. C. Song[2], B. H. Lee[2,3], H. D. Lee[4,5] and Y. H. Jeong[1], *[1]Pohang Univ. of Sci. and Tech., [2]SEMATECH, [3]IBM, [4]Chungnam National Univ. and [5]Univ. of Taxas at Austin (Korea)*

17:05 A-6-2
The origin of slow and fast trapping under Bias Temperature Instability in HfSiO MOSFET
M. Jo[1], H. Park[1], M. Chang[1], H. S. Jung[2], J. H. Lee[2] and H. Hwang[1], *[1]GIST and [2]Samsung Electronics Co., Ltd. (Korea)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-6: Device Technology
(16:45-18:05)
Chairs: K. Shibahara (Hiroshima Univ.)
H. C. Lin (National Chiao Tung Univ.)

16:45 B-6-1
Modeling of Floating-Body Effect in SOI-MOSFET with Complete Surface-Potential Description
T. Murakami, M. Ando, N. Sadachika and M. Miura-Mattausch, *Hiroshima Univ. (Japan)*

17:05 B-6-2
Device Performance and Reliability Considerations of Biaxially Strained Si by Wafer-Bonding-Technology
W. Y. Loh[1], D. S. H. Chan[2], D. Y. J. Choo[1,2], S. M. Koh[1,2], R. Yang[1], X. W. Zhang[1], C. Cai[3], G. Q. Lo[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics, [2]National Univ. of Singapore and [3]IHPC (Singapore)*

Room 201A (C)

Area 12: Spintronic Materials and Devices

C-6: Symposium on Magnetic Tunnel Junctions and Beyond
(17:00-18:00)
Chairs: K. Ando (AIST)
M. Tanaka (Univ. of Tokyo)

17:00 C-6-1(Invited)
Giant TMR and future nonvolatile memory
S. S. P. Parkin, *IBM (USA)*

17:30 C-6-2(Invited)
Spin Injection and Transport in Ferromagnet/semiconductor Structures
C. J. Palmstrom, *Univ. of Minnesota (USA)*

Room 201B (D)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-6: Detectors and Sensors
(16:45-18:00)
Chairs: M. Gotoda (Mitsubishi Electric Corp.)
M. Sugawara (Fujitsu Labs. Ltd.)

16:45 E-6-1
In(Ga)As Quantum Rings for Terahertz Detectors
J. H. Dai, J. H. Lee, Y. L. Lin and S. C. Lee, *National Taiwan Univ. (Taiwan)*

17:00 E-6-2
Design of a spin-coherent photo detector for high-fidelity and high-yield photon-spin quantum state transfer
Y. Rikitake[1,2], H. Imamura[1,2] and H. Kosaka[1,3], *[1]CREST-JST, [2]AIST and [3]Tohoku Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-6: Group-IV Semiconductors III
(16:45-17:45)
Chairs: R. Koch (Johannes Kepler Univ.)
S. Shimomura (Ehime Univ.)

16:45 F-6-1
MBE-grown $Ge_{1-x}C_x$ nanocrystals by using a novel bio-nanoprocess due to protein "ferritin"
Y. Nakama, J. Ohta and M. Nunoshita, *NAIST (Japan)*

17:00 F-6-2
Enhancement of crystal growth rate of Bio-Nano Crystallization by Pulsed Rapid Thermal Annealing
M. Ochi[1], Y. Nanjo[1], Y. Sugawara[1], Y. Uraoka[1], T. Fuyuki[1], M. Okuda[2] and I. Yamashita[1,2], *[1]NAIST and [2]Matsushita Electric Industrial Co., Ltd. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-6: Process and Characterization
(16:45-18:00)
Chairs: A. Nakagawa (New Japan Radio Co., Ltd.)
K. J. Chen (Hong Kong Univ. of Sci. and Tech.)

16:45 G-6-1
Dynamic response of interface state charges in GaN MIS structures
K. Ooyama[1,2], H. Kato[1], M. Miczek[1] and T. Hashizume[1], *[1]Hokkaido Univ. and [2]Sumitomo Metal Mining (Japan)*

17:00 G-6-2
Temperature dependence of current-voltage characteristics for AlGaN-based vertical conducting diodes
A. Nishikawa, K. Kumakura and T. Makimoto, *NTT Corp. (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-6: Nanowire Growth and Devices II
(16:45-17:45)
Chairs: K. Tateno (NTT)
K. Ishibashi (RIKEN)

16:45 H-6-1
Poly-Si Nanowire Thin-Film Transistors with Inverse-T Gate
H. H. Hsu[1], H. C. Lin[1,2], J. F. Huang[1] and C. J. Su[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

17:00 H-6-2
Strained Ge-rich SiGe Nanowire pFETs with High-k/Metal Gate Fabricated using Germanium Condensation Technique
Y. Jiang[1,2], N. Singh[1], D. S. H. Chan[2], T. Y. Liow[1,2], W. Y. Loh[1], S. Balakumar[1], Y. Sun[1], G. Q. Lo[1] and D. L. Kwong[1,2], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore (Singapore)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-6: ReRAM
(16:45-17:55)
Chairs: K. Ito (NEC Corp.)
Y. Shimamoto (Hitachi Ltd.)

16:45 J-6-1(Invited)
Current Development Status and Future Challenge of Metal Oxide RRAM Technologies
N. Awaya, *Sharp Corp. (Japan)*

17:15 J-6-2
Elucidation of ReRAM Mechanism and Improvement of Memory Characteristics by HPHA
D. Seong, D. Lee, S. Oh, M. Pyun and H. Hwang, *GIST (Korea)*

Thursday, September 20

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

17:25 A-6-3
A Comparative Study of Plasma Source-Dependent Charging Polarity in MOSFETs with High-k and SiO_2 Gate Dielectrics
K. Eriguchi[1], M. Kamei[1], D. Hamada[1], K. Okada[2] and K. Ono[1], *[1]Kyoto Univ. and [2]MIRAI-AIST (Japan)*

17:45 A-6-4
Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs
N. Mise, T. Matsuki, T. Watanabe, T. Robata, T. Morooka, T. Eimori and Y. Nara, *Selete (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

17:25 B-6-3
LDMOS Model for Device and Circuit Optimization
M. Yokomichi, M. Miyake, T. Kajiwara, N. Sadachika, A. Yumisaki, H. J. Mattausch and M. Miura-Mattausch, *Hiroshima Univ. (Japan)*

17:45 B-6-4
A New Insulated Gate Bipolar Transistor Structure employing an Embedded Over-current Protection Device
I. H. Ji [1], K. H. Cho[1], Y. H. Choi[1], S. S. Kim[2], K. H. Oh[2], C. M. Yun[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Fairchild Semiconductor (Korea)*

Room 201A (C)

Room 201B (D)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

17:15 E-6-3
Functional Enhancement of Metal-Semiconductor-Metal (MSM) Infrared Photodetectors on Heteroepitaxial SiGe-on-Si Using the Anodic Oxidation/Passivation Method
R. W. Chuang[1], Z. L. Liao[1], H. T. Chiang[1] and N. Usami[2], *[1]National Cheng Kung Univ. and [2]Tohoku Univ. (Taiwan)*

17:30 E-6-4
A MSM Photodetector on p-type GaN for UV Image system
H. B. Lee, H. I. Cho, J. H. Lee and S. H. Hahm, *Kyungpook National Univ. (Korea)*

17:45 E-6-5
MOVPE Prepared ZnO/Si Heterojunction Diodes with Dual Functions: Light-Emission and UV Photo-Detection
J. D. Ye[1], S. L. Gu[2], X. W. Sun[1,3], G. Q. Lo[1], D. L. Kwong[1] and Y. D. Zheng[2], *[1]Inst. of Microelectronics, [2]Nanjing Univ. and [3]Nanyang Technological Univ. (Singapore)*

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"

Thursday, September 20

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

17:15 F-6-3
Compositionally Bi-layered Formation of Interfacial Voids in a Porous Anodic Alumina Template Directly Formed on Si
H. S. Seo[1], Y. G. Jung[1], S. W. Jee[1], J. M. Yang[2] and J. H. Lee[1], *[1]Hanyang Univ. and [2]National Nanofab Center (Korea)*

17:30 F-6-4
Computational Chemistry Study of Diamond-like Carbon: Functions and Structure Control by Frictional Force
Y. Morita, T. Shibata, T. Onodera, R. Sahnoun, M. Koyama, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

17:15 G-6-3
Investigations of Metal/Insulator/AlGaN/GaN Structures by Capacitance-Voltage Measurements and Auger Chemical Profiling
B. Adamowicz[1], M. Miczek[1,2], T. Hashizume[2], A. Klimasek[1], P. Bobek[1] and J. Żywicki[3], *[1]Silesian Univ. of Tech., [2]Hokkaido Univ. and [3]High-Tech International Services Inc. (Poland)*

17:30 G-6-4
Shuttle Activation Annealing of Implanted Al in 4H-SiC
T. Watanabe, R. Hattori, M. Imaizumi and T. Oomori, *Mitsubishi Electric Corp. (Japan)*

17:45 G-6-5
Silicon oxide Gate Dielectric on N-Type 4H-SiC Prepared by Low Thermal Budget Anodization Method
K. C. Chuang and J. G. Hwu, *National Taiwan Univ. (Taiwan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

17:15 H-6-3
High quality $Si_{1-x}Ge_x$ nanowire and its application to MOSFET integrated with HfO_2/TaN/Ta gate stack
W. F. Yang[1], S. J. Lee[1], S. J. Whang[1], S. Y. Lim[1], B. J. Cho[1] and D. L. Kwong[2], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

17:30 H-6-4
Epitaxial insertion of Au_5Si nanodiscs during the growth of silicon nanowires
H. D. Um, Y. G. Jung, H. S. Seo, K. T. Park and J. H. Lee, *Hanyang Univ. (Korea)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

17:35 J-6-3
Gd doping improved resistive switching characteristics of TiO_2-based resistive memory devices
L. F. Liu, J. F. Kang, H. Tang, N. Xu, Y. Wang, X.. Y. Liu, X. Zhang and R. Q. Han, *Peking Univ. (China)*

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
A-7 : Metal Gate-Ⅱ (9:00-10:30) Chairs: T. Nabatame (ASET) K. Shiraishi (Univ. of Tsukuba)	B-7 : Stress Enhancement Technologies (9:00-10:20) Chairs: F. Boeuf (STMicroelectronics) H. Wakabayashi (Sony Corp.)	C-7 : Interconnects for RF and Mixed Signal Application (9:00-10:30) Chairs: Y. Hayashi (NEC Corp.) M. Matsuura (Renesas Technology Corp.)	D-7 : Nano-Bio Devices Ⅰ (9:00-10:30) Chairs: T. Nishimoto (Shimadzu Corp.) H. Tabata (Univ. of Tokyo)	E-7 : All-Optical Light Control (9:00-10:30) Chairs: R. Akimoto (AIST) Y. Lee (Hitachi, Ltd.)
9:00 A-7-1 (Invited) Schottky Barrier and Stability of Metal/ High-k Interfaces; Theoretical View T. Nakayama, *Chiba Univ. (Japan)*	**9:00 B-7-1** NMOS Current Enhancement and Layout Dependency Improvement by Using Atomic Layer Deposition SIN Spacer H. Nagai, K. Ookoshi, H. Morioka, T. Mori, M. Kojima, Y. Takao, M. Kase and K. Hashimoto, *Fujitsu Ltd. (Japan)*	**9:00 C-7-1** Impacts of Cu/TaN Electrode on the Electrical Properties of Metal-insulator-metal (Ba,Sr)TiO_3 Thin-film Capacitors W. F. Wu[1], K. C. Tsai[1,2], C. G. Chao[2], J. T. Lee[2], W. C. Chang[3], T. K. Kang[3], G. S. Jheng[4] and J. Y. Lin[4], *[1]National Nano Device Labs., [2]National Chiao Tung Univ., [3]Feng Chia Univ. and [4]National Yunlin Univ. of Sci. and Tec. (Taiwan)*	**9:00 D-7-1 (Invited)** Si based Planer Type Ion-channel Biosensor and Its Applications T. Urisu[1,2], H. Uno[2], T. Asano[2], M. Y. Li[1], R. Tero[1,2] and K. Ishii[3], *[1]Inst. for Molecular Sci., [2]Graduate Univ. for Advanced Studies and [3]Chubu Univ. (Japan)*	**9:00 E-7-1 (Invited)** GaN-Based High-Speed Intersubband Optical Switches N. Iizuka[1], K. Kaneko[1], N. Suzuki[1], C. Kumtornkittikul[2], T. Shimizu[2], M. Sugiyama[2] and Y. Nakano[2], *[1]Toshiba Corp. and [2]Univ. of Tokyo (Japan)*
9:30 A-7-2 Anomalous positive V_{fb} shift in $HfAlO_x$ MOS gate stacks W. Wang[1], K. Akiyama[2], W. Mizubayashi[1], M. Ikeda[2], H. Ota[1], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, AIST, [2]MIRAI-ASET, AIST and [3]Univ. of Tokyo (Japan)*	**9:20 B-7-2** In-situ Doped Embedded-SiGe Source/Drain Technique for 32 nm-node pMOSFET H. Okamoto, A. Hokazono, K. Adachi, N. Yasutake, H. Itokawa, S. Okamoto, M. Kondo, H. Tsujii, T. Ishida, N. Aoki, M. Fujiwara, S. Kawanaka, A. Azuma and Y. Toyoshima, *Toshiba Corp. (Japan)*	**9:20 C-7-2** Fully Analytical Modeling of Cu Interconnects Up to 110 GHz J. D. Jin[1], S. S. H. Hsu[1], T. J. Yeh[2], M. T. Yang[2] and S. Liu[2], *[1]National Tsing Hua Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*	**9:30 D-7-2** An immunosensor based on N-doped multiwalled carbon nanotubes S. A. Contera, H. J. Burch, M. de Planque, K. Voitchovsky and J. F. Ryan, *Univ. of Oxford (UK)*	**9:30 E-7-2** Characterization of Narrow Mesa Width Waveguide for All Optical Switching Device Based on Intersubband Transition in II-VI Based Quantum Wells K. Akita, R. Akimoto, C. Guangwei, T. Hasama and H. Ishikawa, *AIST (Japan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**		**Area 4: Advanced Memory Technology**
F-7 : Material Characterization (9:00-10:15) Chairs: K. Kobayashi (Waseda Univ.) T. Iwai (Fujitsu Labs. Ltd.)	G-7 : Emerging Devices (9:00-10:30) Chairs: T. Hashizume (Hokkaido Univ.) R. Hattori (Mitsubishi Electric Corp.)	H-7 : Organic Transistor Ⅰ (9:00-10:30) Chairs: T. Minakata (Asahi-KASEI Corp.) K. Fujita (Kyushu Univ.)		J-7 : DRAM Ⅱ (9:00-10:20) Chairs: I. Asano (Elpida Memory, Inc.) M. Moniwa (Renesas Technology Corp.)
9:00 F-7-1 (Invited) In-Situ X-Ray Diffraction during Semiconductor Nanostructure Growth M. Takahasi, *JAEA (Japan)*	**9:00 G-7-1 (Invited)** Growth of InAs Channel HEMT Structure on Si substrate and It's Possible Application for Low Power Logic E. Y. Chang, H. Yamaguchi, Y. C. Lin, M. Ueki, Y. Hirayama and C. Y. Chang, *National Chiao Tung Univ. (Taiwan)*	**9:00 H-7-1 (Invited)** Jet-pinted Polymer Transistor Display Backplanes R. A. Street, A. C. Arias and J. H. Daniel, *Palo Alto Research Center (USA)*		**9:00 J-7-1** Ru/TiO_2/ZrO_2/TiN (RIT-TiO_2/ZrO_2) Capacitor Structure for the 50nm DRAM Device and beyond J. S. Lim, K. C. Kim, K. H. Lee, J. H. Choi, Y. S. Tak, W. D. Kim, J. Y. Kim, K. Cho, Y. Kim, J. H. Chung, Y. S. Kim, S. T. Kim and W. Han, *Samsung Electronics Co.,Ltd. (Korea)*
9:30 F-7-2 *In situ* Analysis for Initial Formation Process of Gold Nanoparticles in Discharge in Aqueous Solution C. Miron[1], M. A. Bratescu[2], T. Ishizaki[1], N. Saito[1] and O. Takai[2], *[1]Nagoya Univ. and [2]EcoTopia Sci. Inst. (Japan)*	**9:30 G-7-2** N-channel MOSFETs with *In-situ* Silane-Passivated Gallium Arsenide Channel and CMOS-Compatible Palladium-Germanium Contacts H. C. Chin[1], M. Zhu[1], K. M. Hoe[2], G. S. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*	**9:30 H-7-2** Frequency Dependence of Displacement Current and Channel Current in Pentacene Thin-Film Transistors S. Suzuki, Y. Yasutake and Y. Majima, *Tokyo Tech. (Japan)*		**9:20 J-7-2** Electrical Properties of TiO/LaTiO/TiO Stacked Thin Films H. Hara[1], M. Tanioku[2], M. Yamato[1] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Elpida Memory, Inc. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

9:50 A-7-3
Effect of Ultra-thin Al_2O_3 Insertion on Fermi-level Pinning at Metal/Ge Interface
T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

10:10 A-7-4
Systematic studies on Fermi level pining of Hf-based high-k gate stacks
K. Shiraishi[1,2], Y. Akasaka[3,1,7], G. Nakamura[3,7], M. Kadoshima[3], H. Watanabe[4], K. Ohmori[5], T. Chikyow[6], K. Yamabe[1], Y. Nara[3], Y. Ohji [3] and K. Yamada[5], *[1]Univ. of Tsukuba, [2]CREST-JST, [3]SELETE, [4]Osaka Univ., [5]Waseda Univ., [6]NIMS and [7]Tokyo Electron Inc. (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

9:40 B-7-3
Principal Guideline of Stress Design for Ion Enhancement in Advanced MOSFET Structure with Dual Stress Liner Technique
M. Nishikawa[1], H. Nomura[1], T. Miyashita[2], M. Kojima[1], Y. Takao[1] and K. Hashimoto[1], *[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd. (Japan)*

10:00 B-7-4
Study of Stress from Discontinuous SiN Liner for Fully-Silicided Gate Process
T. Yamashita[1,2], Y. Nishida[1], T. Okagaki[1], Y. Miyagawa[1], J. Yugami[1], H. Oda[1], Y. Inoue[1] and K. Shibahara[2], *[1]Renesas Tech. Corp. and [2]Hiroshima Univ. (Japan)*

10:20 B-7-5
Strained N-channel FinFETs with High-stress Nickel Silicide-Carbon Contacts and Integration with FUSI Metal Gate Technology
T. Y. Liow[1,2], R. T. P. Lee[1], K. M. Tan[1], M. Zhu[1], K. M. Hoe[2], G. S. Samudra[1], N. Balasubramanian[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

9:40 C-7-3
A Small Area, 3-Dimensional On-chip Inductors for High-speed Signal Processing under Low Power Supply Voltages
K. Hijioka, A. Tanabe, Y. Amamiya and Y. Hayashi, *NEC Corp. (Japan)*

10:00 C-7-4 (Invited)
Wiring technology for analog and mixed signal LSIs
A. Matsuzawa, *Tokyo Tech. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

9:45 D-7-3
Reverse Electroporation with Carbon Nanotubes-loaded Electrode for Highly Efficient Gene Transfer
Y. Inoue[1], H. Fujimoto[1], T. Ogino[2] and H. Iwata[1], *[1]Kyoto Univ. and [2]Yokohama National Univ. (Japan)*

10:00 D-7-4
Rapid and High Sensitive Detection of Bacteria Sensor using a Porous Ion Exchange Film
K. Miyano[1], H. Aoki[1], S. Hotta[1], N. Fujiwara[2], D. Yano[3], K. Sano[3], K. Yamanaka[3], C. Kimura[1] and T. Sugino[1], *[1]Osaka Univ., [2]TRI-Osaka and [3]Organo Corp. (Japan)*

10:15 D-7-5
Ion-Sensitive Field Effect Transistor Based on Silicon and Zinc Oxide for DNA Sensor
M. Seki, T. Uno, M. Noguchi and H. Tabata, *Univ. of Tokyo (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

9:45 E-7-3
Saturation characteristics simulation of Intersubband absorption for [(CdS/ZnSe/BeTe)/(ZnSe/BeTe)] coupled quantum wells
G. W. Cong, R. Akimoto, K. Akita, T. Hasama and H. Ishikawa, *AIST (Japan)*

10:00 E-7-4
Magneto-Optical (Cd,Mn)Te/(Cd,Zn)Te Quantum Well Waveguide with Broadband Operation Optical Isolator
M. C. Debnath, V. Zayets and K. Ando, *AIST (Japan)*

10:15 E-7-5
Passive Optical Alignment with High Accuracy for Low-Loss Optical Interposer
M. Fujiwara[1,2], S. Terada[1], Y. Shirato[1], H. Owari[1], K. Watanabe[1], M. Matsuyama[1], K. Takahama[1], T. Mori[1], K. Miyao[1], K. Choki[1], T. Fukushima[2], T. Tanaka[2] and M. Koyanagi[2], *[1]Sumitomo Bakelite Co., Ltd and [2]Tohoku Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:45 F-7-3
Scanning Surface Hall Potentiometry on Semiconductor Wafers
Y. Hidaka, D. Maruyama, J. Uchikoshi, M. Morita and K. Arima, *Osaka Univ. (Japan)*

10:00 F-7-4
Investigation of FePt Nano-Dots Fabricated by Self-Assembled Nano-Dot Deposition Method Using X-ray Photoelectron Spectroscopy
M. Murugesan[1], J. C. Bea[1], C. K. Yin[2], H. Nohira[3], E. Ikenaga[4], T. Hattori[3], M. Nishijima[2], T. Fukushima[2], T. Tanaka[2], M. Miyao[5] and M. Koyanagi[2], *[1]JST, [2]Tohoku Univ., [3]Musashi Inst. of Tech., [4]JASRI and [5]Kyushu Univ. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

9:45 G-7-3
Improved electrical characteristics of $Pt/Gd_2O_3/GaAs$ MOS capacitors with surface preparation procedures
C. C. Cheng[1], C. H. Chien[1,2], G. L. Luo[2], C. K. Tseng[1], H. C. Chiang[1], C. H. Yang[2] and C. Y. Chang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

10:00 G-7-4
Performance and Stability of ZnO/ZnMgO Hetero-MIS FETs
S. Sasa, T. Hayafuji, M. Kawasaki, K. Koike, M. Yano and M. Inoue, *Osaka Inst. of Tech. (Japan)*

10:15 G-7-5
The Effect of Rapid Thermal Annealing on the Electrical Characteristics of ZnO TFTs
K. Remashan, D. K. Hwang, S. J. Park and J. H. Jang, *GIST (Korea)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

9:45 H-7-3
Analysis of charge accumulation in pentacene field effect transistor with ferroelectric gate insulator on the basis of Maxwell-Wagner model
R. Tamura, S. Yoshita, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

10:00 H-7-4
An Analytic Current-Voltage Equation for Top-contact OTFTs Including the Effects of Variable Series Resistance
K. D. Jung, B. J. Kim, Y. C. Kim, B. G. Park, H. Shin and J. D. Lee, *Seoul National Univ. (Korea)*

10:15 H-7-5
Potential Fluctuation within a Crystalline Domain in Pentacene Thin Film Transistors and its Origin
N. Ohashi, H. Tomii, R. Matsubara, M. Sakai, K. Kudo and M. Nakamura, *Chiba Univ. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

9:40 J-7-3
Nitrogen Profile Study for SiON Gate Dielectrics of Advanced DRAM
S. Murakawa[1,2], M. Takeuchi[3], M. Honda[3], S. Ishizuka[3], T. Nakanishi[3], Y. Hirota[3], T. Sugawara[1], Y. Tanaka[1], Y. Akasaka[1], A. Teramoto[2], S. Sugawa[2] and T. Ohmi[2], *[1]Tokyo Electron Ltd., [2]Tohoku Univ. and [3]Tokyo Electron AT Ltd. (Japan)*

10:00 J-7-4
Effect of Boron-Nitride Formation at the Interface of Diffusion Barrier in Tungsten Polymetal Gate Stacks on Gate Interfacial Resistance
M. G. Sung, K. Y. Lim, Y. S. Kim, H. J. Cho, S. R. Lee, S. A. Jang, M. S. Joo, J. H. Lee, T. Y. Kim, T. O. Youn, J. H. Kim, G. O. Kim, Y. T. Hwang, H. S. Yang, J. C. Ku and J. W. Kim, *Hynix Semiconductor Inc. (Korea)*

Friday, September 21

Room 101 (A) | Room 102 (B) | Room 201A (C) | Room 201B (D) | Room 202A (E)

Break

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-8 : High-k/Metal Gate Transistor
(10:45-12:05)
Chairs: H. Fukutome (Fujitsu Labs. Ltd.)
Y. Tsunashima (Toshiba Corp.)

10:45 A-8-1
Production-Worthy HfSiON Gate Dielectric Fabrication Enabling EOT Scalability Down to 0.86 nm and Excellent Reliability by Polyatomic Layer Chemical Vapor Deposition Technique
D. Ishikawa[1], S. Kamiyama[1], A. Sano[2], S. Horii[2], T. Aoyama[1] and Y. Nara[1], *[1]Selete and [2]Hitachi Kokusai Electric Inc. (Japan)*

11:05 A-8-2
Tinv Scaling and Jg Reducing for nMOSFET with $HfSi_x/HfO_2$ Gate Stack by Interfacial Layer Formation Using Ozone Water Treatment Process
I. Oshiyama[1], K.Tai[1], T. Hirano[1], S. Yamaguchi[1], K. Tanaka[1], Y. Hagimoto[1], T. Uemura[1], T. Ando[1], K. Watanabe[1], R. Yamamoto[1], S. Kanda[1], J. Wang[1], Y. Tateshita[1], H. Wakabayashi[1], Y. Tagawa[1], M. Tsukamoto[1], H. Iwamoto[1], M. Saito[1], M. Oshima[2], S. Toyoda[2], N. Nagashima[1] and S. Kadomura[1], *[1]Sony Corp. and [2]Univ. of Tokyo (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-8 : Modeling and Simulation
(10:45-12:25)
Chairs: A. Hokazono (Toshiba Corp.)
Y. Momiyama (Fujitsu Labs. Ltd.)

10:45 B-8-1
Capacitive Parameter Extraction for Nanometer-Size Field-Effect Transistors
H. Inokawa[1], A. Fujiwara[2], K. Nishiguchi[2] and Y. Ono[2], *[1]Shizuoka Univ. and [2]NTT Corp. (Japan)*

11:05 B-8-2
Study of Parasitic Resistance Behavior and Its Extraction Method on Deeply Scaled MOSFETs
H. Tsujii, A. Hokazono, M. Fujiwara, S. Kawanaka, A. Azuma, N. Aoki and Y. Toyoshima, *Toshiba Corp. (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-8 : Interconnect Reliability
(10:45-12:15)
Chairs: K. Ueno (Shibaura Inst. of Technology)
M. Kodera (Toshiba Corp.)

10:45 C-8-1 (Invited)
Stress Migration Phenomenon in Narrow Copper Interconnects
T. Nakamura and T. Suzuki, *Fujitsu Labs. Ltd. (Japan)*

11:15 C-8-2
Improvement of Adhesion at the Interface between Low-k Spin-on Dielectric and underlying SiCO Barrier by Plasma Treatments
Y. Takigawa, S. Nakao, M. Shiohara, N. Oda and S. Ogawa, *Selete (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

D-8 : Nano-Bio Devices Ⅱ
(10:45-12:15)
Chairs: I. Yamashita (Nara Inst. of Sci. and Tech.)
S. Antoranz Contera (Univ. of Oxford)

10:45 D-8-1 (Invited)
Bio-Nano Approaches to Fabrication of Quantum Dot Floating Gate Flash Memories
S. K. Banerjee[1], S. Tang[1], C. Mao[2], J. Sarkar[1], H. Liu[1], D. Shahrjerdi[1], C. H. Lee[1] and J. D. Trent[3], *[1]Univ. of Texas at Austin, [2]Univ. of Oklahoma and [3]NASA Ames Research Center (USA)*

11:15 D-8-2
Floating Gate MOS Capacitor with High-Density Nanodots Array Produced by Protein Supramolecule
K. Yamada[1,2], S. Yoshii[1], S. Kumagai[1], A. Miura[2], Y. Uraoka[2], T. Fuyuki[2] and I. Yamashita[1,2,3], *[1]Matsushita Electric Industrial Co., Ltd., [2]NAIST and [3]CREST-JST (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-8 : Lasers and LEDs
(10:45-12:15)
Chairs: M. Ezaki (Toshiba Corp.)
M.Gotoda (Mitsubishi Electric Corp.)

10:45 E-8-1 (Invited)
Widely Tunable Integrated DBR Laser Array with Fast Wavelength Switching
S. Tsuji[1,2], H. Arimoto[1,2], T. Tsuchiya[1,2], T. Kitatani[1,2], K. Shinoda[1,2], T. Otoshi[1] and M. Aoki[1,2], *[1]Hitachi, Ltd. and [2]OITDA (Japan)*

11:15 E-8-2
High Density Two Dimensional LED Arrays Using Single Crystal Semiconductor Thin Films
T. Suzuki, H. Fujiwara, T. Sagimori, T. Igari, H. Furuta, Y. Nakai, I. Abiko, M. Sakuta and M. Ogihara, *Oki Digital Imaging Corp. (Japan)*

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Room 202B (F) | Room 303 (G) | Room 304 (H) | Room 405 (I) | Room 406 (J)

Break

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

H-8 : Organic Transistor Ⅱ
(10:45-12:15)
Chairs: K. Nomoto (Sony Corp.)
K. Kudo (Chiba Univ.)

10:45 H-8-1
Hall effect measurements of polycrystalline pentacene TFTs with double gate structures
Y. Takamatsu, T. Sekitani and T. Someya, *Univ. of Tokyo (Japan)*

11:00 H-8-2
Probing of channel formation in organic field effect transistors by optical second harmonic generation measurement
E. Lim, H. S. Lee, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

I-8 : Novel Nanostructure Devices
(10:45-12:00)
Chairs: M. Watanabe (Tokyo Tech.)
H. Mizuta (Tokyo Tech.)

10:45 I-8-1
Self-Assembling Formation of Ni Nanodots on SiO_2 Induced by Remote H_2 -plasma Treatment and Their Electrical Charging Characteristics
K. Makihara, K. Shimanoe, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

11:00 I-8-2
Reduction of a Ferritin Core Embedded in Silicon Oxide Film for An Application to Floating Gate Memory
T. Matsumura[1], A. Miura[1], Y. Uraoka[1], T. Fuyuki[1], S. Yoshii[2] and I. Yamashita[1,2,3], *[1]NAIST, [2]Matsushita Electric Industrial Co., Ltd. and [3]CREST-JST (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

J-8 : FeRAM/MRAM
(10:45-12:05)
Chairs: T. Eshita (Fujitsu Ltd.)
H. Jeong (Samsung Electronics Co. Ltd.)

10:45 J-8-1
Improvement of Thermal Stability of MRAM Device with SiN Protective Film Deposited by HDP CVD
K. Suemitsu[1], Y. Kawano[2], H. Utsumi[1], H. Honjo[1], R. Nebashi[1], S. Saito[1], N. Ohshima[1], T. Sugibayashi[1], H. Hada[1], T. Nohisa[2], T. Shimazu[2], M. Inoue[2] and N. Kasai[1], *[1]NEC Corp. and [2]Mitsubishi Heavy Industries, Ltd. (Japan)*

11:05 J-8-2
Two-Dimensional Electron Gas Switching in an Ultra Thin Epitaxial ZnO Layer on a Ferroelectric Gate Structure
Y. Kaneko, H. Tanaka, Y. Kato and Y. Shimada, *Matsushita Electric Industrial Co., Ltd. (Japan)*

Friday, September 21

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

11:25 A-8-3
Highly anufacturable CMOSFETs with Single High-k (HfLaO) and Dual Metal Gate Integration Process
X. P. Wang[1,2,3], M. F. Li[1,2,4], H. Y. Yu[3], J. J. Yang[1], C. X. Zhu[1], W. S. Hwang[1], W. Y. Loh[2], A. Y. Du[2], J. D. Chen[1,2], A. Chin[5], S. Biesemans[3], G. Q. Lo[2] and D. L. Kwong[2], *[1]National Univ. of Singapore, [2]Inst. of Microelectronics, [3]IMEC, [4]Fudan Univ. and [5]National Chiao Tung Univ. (Singapore)*

11:45 A-8-4
Highly Manufacturable and Cost-effective Single Ta_xC / $Hf_xZr_{(1-x)}O_2$ Gate CMOS Bulk Platform for LP Applications at the 45nm Node and Beyond
M. Müller[1,4], C. Hobbs[2], A. Zauner[1], S. Barnola[5], T. Salvetat[5], S. Lhostis[3], S. Couderc[3], P. Perreau[5], D.H. Triyoso[2], M. Raymond[2], E. Luckowski[2], M. Rafik[3], A. Cathignol[3], G. Ribes[3], D. Fleury[3], K. Romanjek[1], S. Pokrant[1], S. Jullian[1], P. Morin[3], M. Aminpur[2], P. Gouraud[3], C. Laviron[5], S. Zoll[3], P. Garnier[1] and F. Salvetti[1], *[1]NXP Semiconductors, [2]Freescale, [3]STMicroelectronics, [4]NXP Semiconductors Research and [5]CEA-LETI (France)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

11:25 B-8-3
Two-step Inverse Modeling for Estimation of Channel Impurity Pile-up
T. Nagumo[1], K. Takeuchi[1], Y. Akiyama[2] and M. Hane[1], *[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)*

11:45 B-8-4
Discrete-Dopant-Fluctuated Threshold Voltage Roll-Off in Sub-16nm Bulk FinFETs
Y. Li, C. H. Hwang, H. M. Huang and T. C. Yeh, *National Chiao Tung Univ. (Taiwan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

11:35 C-8-3
Effect of temperature and film thickness on resistivity of CoWP
J. Gambino[1], F. Chen[1], S. Mongeon[1], D. Meatyard[1], E. Adams[1], P. Dehaven[1], C. Cabral[2] and I. Ivanov[3], *[1]IBM, [2]IBM T. J. Watson Research Center and [3]Blue29, LLC (USA)*

11:55 C-8-4
Highly Reliable Cu Interconnect using Low Hydrogen Silicon Nitride Film Deposited at Low Temperature for Cu-Diffusion Barrier
T. Murata, K. Kono, Y. Tsunemine, M. Fujisawa, M. Matsuura, K. Asai and M. Kojima, *Renesas Tech. Corp. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

11:45 D-8-4
Microfluidic Amperometric Biochips Based on Carbon Nanotube Arrayed Electrodes
Y. Tsujita[1], K. Maehashi[1], K. Matsumoto[1], H. Kwon[2], Y. Takamura[2] and E. Tamiya[1], *[1]Osaka Univ. and [2]JAIST (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

11:30 E-8-3
Improvement of Kink-Free Light Output for Fiber Pump Semiconductor Lasers
N. Shomura and T. Numai, *Ritsumeikan Univ. (Japan)*

11:45 E-8-4
Multiwavelength emitting InGaN/GaN quantum well grown on V-shaped GaN $(1\bar{1}01)$ microfacet
J. W. Ju[1], L. W. Jang[1], S. J. Lee[2], J. H. Baek[2] and I. H. Lee[1], *[1]Chonbuk National Univ. and [2]Korea Photonics Tech. Inst. (Korea)*

Room 202B (F)

Room 303 (G)

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

11:15 H-8-3
Study of Pentacene-Based Organic Thin Film Transistor with PMMA as Insulator
T. S. Huang, Y. K. Su and B. C. Wang, *National Cheng Kung Univ. (Taiwan)*

11:30 H-8-4
Transient Current Characteristics of Organic Field Effect Transistors with Polymer and Inorganic Gate Insulators
K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, T. Kodzasa and T. Kamata, *AIST (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

11:15 I-8-3
Characterization of Multistep Electron Charging and Discharging of Silicon-Quantum-Dots Floating Gate by Applying Pulsed Gate Biases
R. Matsumoto, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

11:30 I-8-4
Photon Position Detector Consisting of Single-Electron Devices
A. K. Kikombo[1], M. Tabe[2] and Y. Amemiya[1], *[1]Hokkaido Univ. and [2]Shizuoka Univ. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

11:25 J-8-3
Manufacturable High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process
K. R. Udayakumar[1], T. S. Moise[1], S. R. Summerfelt[1], K. Boku[1], J. Rodriguez[1], K. Remack[1], J. Gertas[1], M. Arendt[1], G. Shinn[1], J. Eliason[2], R. Bailey[2] and P. Staubs[2], *[1]Texas Instruments Inc. and [2]Ramtron International Corp. (USA)*

11:45 J-8-4
Endurance Characterization of Ferroelectric Cell in 64Mb FRAM Device By Analyzing the Space Charge Concentration
E. S. Lee, Y. M. Kang, D. J. Jung, H. H. Kim, Y. K. Hong, J. H. Park, S. K. Kang, J. H. Kim, H. S. Kim, W. W. Jung, W. S. Ahn, J. Y. Jung, J. Y. Kang, D. Y. Choi, H. K. Goh, S. Y. Kim, S. Y. Lee and H. S. Jeong, *Samsung Electronics Co., Ltd. (Korea)*

Friday, September 21

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

Room 102 (B)

Area 3: CMOS Devices/Device Physics

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

12:00 D-8-5
Fabrication of single electron transistor using cage-shaped protein supramolecule
S. Kumagai[1], S. Yoshii[1], N. Matsukawa[1], R. Tsukamoto[3], K. Nishio[1] and I. Yamashita[1,2,3], *[1]Matsushita Electric Industrial Co., Ltd, [2]NAIST and [3]Core Research for Evolutional Sci. and Tech. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

12:00 E-8-5
Realization of 340nm-band high-power (>7mW) InAlGaN quantum well UV-LED with p-type InAlGaN
S. Fujikawa[1], T. Takano[1,2], Y. Kondo[1,2] and H. Hirayama[1], *[1]RIKEN and [2]Matsushita Electric Works, Ltd. (Japan)*

Friday, September 21

Room 202B (F)

Room 303 (G)

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

11:45 H-8-5
Mobility Improvement of Pentacene Thin Film Transistors by Introduction of H_2 during Evaporation
T. Yokoyama, C. B. Park, Y. Kikuchi, T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

12:00 H-8-6
Evidence of Electron Trapping Center at Pentacene/SiO_2 Interface
C. B. Park, T. Yokoyama, T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

11:45 I-8-5
Improved Photoconduction Effects of Nanometer-Sized Si Dot Multilayers
Y. Hirano[1], S. Yamazaki[2] and N. Koshida[2], *[1]NHK Sci. and Technical Research Labs. and [2]Tokyo Univ. of Agriculture and Tech. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

Lunch

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-9 : FUSI
(13:15-14:55)
Chairs: T. Tatsumi (NEC Corp.)
T. Nabatame (ASET)

13:15 A-9-1
Practical Solutions to Enhance EWF Tunability of Ni FUSI Gates on HfO_2
X. P. Wang[1,2,3], J. J. Yang[1], H. Y. Yu[3], M. F. Li[1,2,4], J. D. Chen[1], R. L. Xie[1], C. X. Zhu[1], A. Y. Du[2], P. C. Lim[5], A. Lim[1,2], Y. Y. Mi[5], D. M. Y. Lai[5], W. Y. Loh[2], S. Biesemans[3], G. Q. Lo[2] and D. L. Kwong[2], *[1]National Univ. of Singapore, [2]Inst. of Microelectronic, [3]IMEC, [4]Fudan Univ. and [5]Inst. of Materials Research and Engineering (Singapore)*

13:35 A-9-2
Effectiveness of Aluminum Incorporation in Nickel Silicide and Nickel Germanide Metal Gates for Work Function Reduction
A. E. J. Lim[1], R. T. P. Lee[1], A. T. Y. Koh[1], G. S. Samudra[1], D. L. Kwong[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-9 : Post Planar CMOS
(13:15-14:55)
Chairs: A. Hokazono (Toshiba Corp.)
H. Sayama (Renesas Technology Corp.)

13:15 B-9-1
Wide-Range V_{th} Controllable SOTB (Silicon on Thin BOX) Integrated with Bulk CMOS Featuring Fully Silicided NiSi Gate Electrode
T. Ishigaki[1], R. Tsuchiya[1], Y. Morita[1], N. Sugii[1], S. Kimura[1], T. Iwamatsu[2], T. Ipposhi[2], Y. Inoue[2] and T. Hiramoto[3], *[1]Hitachi, Ltd., [2]Renesas Tech. Corp. and [3]Univ. of Tokyo (Japan)*

13:35 B-9-2
Additivity between sSOI- and CESL-induced nMOSFETs Performance Boosts
F. Andrieu[1], F. Allain[1], C. Buj-Dufournet[1], O. Faynot[1], F. Rochette[1], M. Cassé[1], V. Delaye[1], F. Aussenac[1], L. Tosti[1], P. Maury[1], L. Vandroux[1], N. Daval[2], I. Cayrefourcq[2] and S. Deleonibus[1], *[1]CEA-LETI MINATEC and [2]SOITEC (France)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-9 : Low-k and Airgap
(13:15-15:05)
Chairs: J. Koike (Tohoku Univ.)
J. Gambino (IBM)

13:15 C-9-1 (Invited)
Low-k/Cu Integration Consistent from 90 nm thru 32 nm
T. Nogami, *IBM (USA)*

13:45 C-9-2
Influences of Skeletal Structure and Porosity on Dielectric and Mechanical Properties of Porous Organosilica Low-k Films
S. Takada , N. Hata, Y. Seino and T. Yoshino, *AIST (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

D-9 : Spectroscopy for Bio Sensing
(13:15-14:45)
Chairs: K. Ajito (NTT)
M. Niwano (Tohoku Univ.)

13:15 D-9-1 (Invited)
THz and microwave biochip
C. K. Sun, *National Taiwan Univ. (Taiwan)*

13:45 D-9-2
In-Situ Detection and Classification of DNA by Porous Alumina Filter in Conjugation with Infrared Absorption Spectroscopy
R. Yamaguchi, A. Hirano, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-9 : LEDs
(13:15-15:00)
Chairs: Y. Lee (Hitachi Ltd.)
M. Ezaki (Toshiba Corp.)

13:15 E-9-1
High-Brightness Ultraviolet LEDs on Si Using Quaternary InAlGaN Multi-Quantum-Wells with High Indium Contents
Y. Fukushima, Y. Takase, M. Usuda, K. Orita, T. Ueda and T. Tanaka, *Matsushita Electric Industrial Co., Ltd. (Japan)*

13:30 E-9-2
Effect of Multiquantum Barriers on Carrier Transport Mechanism of InGaN/GaN Multiple Quantum Well Light-emitting Diodes
W. T. Su[1], Y. F. Chen[1], H. Y. Chen[1], J. C. Wang[1], H. T. Shen[1], T. E. Nee[1] and Y. F. Wu[2], *[1]Chang Gung Univ. and [2]Tech. and Sci. Inst. of Northern Taiwan (Taiwan)*

Lunch

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

F-9 : Characterization
(13:15-14:55)
Chairs: S. Miyazaki (Hiroshima Univ.)
H. Hwang (Gwangju Inst. of Science & Engineering)

13:15 F-9-1
Advanced Characterization of High-k Gate Stack by Internal Photo Emission (IPE): Interfacial Dipole and Band Diagram in $Al/Hf(Si)O_2/Si$ MOS Structure
J. Widiez, K. Kita, T. Nishimura and A. Toriumi, *Univ. of Tokyo (Japan)*

13:35 F-9-2
Characterization of the $Sc_2O_3La_2O_3$ High-κ Gate Stack by STM
Y. C. Ong[1], D. S. Ang[1], S. J. O' Shea[2], K. L. Pey[1], T. Kawanago[3], K. Kakushima[3] and H. Iwai[3], *[1]Nanyang Technological Univ., [2]Inst. of Material Research and Engineering and [3]Tokyo Tech. (Singapore)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

G-9 : Imaging Technology
(13:15-14:35)
Chairs: H. Yamauchi (Samsung Electronics Co., Ltd.)
T. Matsuoka (Osaka Univ.)

13:15 G-9-1
Real-Time Variable-Resolution and Dynamic Range Boosting CMOS Image Sensor
J. J. Wang, C. J. Lin and Y. C. King, *National Tsing Hua Univ. (Taiwan)*

13:35 G-9-2
High Sensitivity Dynamic Range Enhanced CMOS Imager with Noise Suppression
S. Adachi[1], W. Lee[2], N. Akahane[2], H. Oshikubo[1], K. Mizobuchi[1] and S. Sugawa[2], *[1]Texas Instruments Japan and [2]Tohoku Univ. (Japan)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

H-9 : Organic Transistor Ⅲ
(13:15-14:45)
Chairs: T. Kamata (AIST)
T. Someya (Univ. of Tokyo)

13:15 H-9-1 (Invited)
Vertical Type Organic Transistors for Flexible Opto-electric Devices
K. Kudo, *Chiba Univ. (Japan)*

13:45 H-9-2
Highly Reliable Bottom-Contact Pentacene TFTs with a Poly(*p*-chloroxylylene) Layer Selectively Grown on a Gate-Insulator
R. Yasuda[1], N. Hirai[1], I. Yagi[1], K. Nomoto[1], J. Kasahara[1], T. Minari[2], K. Tsukagoshi[2] and Y. Aoyagi[2], *[1]Sony Corp. and [2]RIKEN (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

I-9 : Quantum Dots and Qubits
(13:15-15:00)
Chairs: T. Usuki (Univ. of Tokyo)
K. Ono (RIKEN)

13:15 I-9-1 (Invited)
Scanning Probe Measurements on Semiconductor Nanostructures
T. Ihn, A. Gildemeister, A. Pioda, S. Kicin and K. Ensslin, *ETH Zurich (Switzerland)*

13:45 I-9-2
Spin-conserved Single-electron Transport between Zeeman Sublevels in a Few-electron Quantum Dot
T. Fujisawa[1,2], G. Shinkai[1,2] and T. Hayashi[1], *[1]NTT Corp. and [2]Tokyo Tech (Japan)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

J-9 : Carbon Nanotube Devices and Growth Ⅰ
(13:15-15:00)
Chairs: Y. Ochiai (JST)
Y. Ohno (Nagoya Univ.)

13:15 J-9-1 (Invited)
Digital Circuits with Carbon Nanotube Transistors
A. Raychowdhury[1,2], J. Kurtin[1], K. Roy[2], V. De[1] and A. Keshavarzi[1], *[1]Intel Corp. and [2]Purdue Univ. (USA)*

13:45 J-9-2 (Invited)
Advances in Carbon Nanotube Devices and Circuits
Y. M. Lin, Z. Chen, J. Appenzeller, P. M. Solomon and P. Avouris, *IBM (USA)*

Friday, September 21

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

13:55 A-9-3
Impacts of Fluorine and Nitrogen Incorporation on NiSi Induced Junction Leakage on Si(110) Substrate
M. Tsuchiaki and A. Nishiyama, *Toshiba Corp. (Japan)*

14:15 A-9-4
Phase and Composition Control of Ni-FUSI gates by N_2 I/I with Double Ni-silicidation
K. Yamamoto[1], S. Sakashita[2], Y. Sato[1], M. Inoue[2], M. Anma[2], T. Oosuka[1] and J. Yugami[2], *[1]Matsushita Electric Industrial Co., Ltd. and [2]Renesas Tech. Corp. (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

13:55 B-9-3
Novel Extended-Pi Shaped Silicon-Germanium (eII-SiGe) Source/Drain Stressors for Strain and Performance Enhancement in P-Channel FinFETs
K. M. Tan[1], T. Y. Liow[1,2], R. T. P. Lee[1], M. Zhu[1], K. M. Hoe[2], C. H. Tung[2], N. Balasubramanian[2], G. S. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

14:15 B-9-4
Impact of Gradual Source/Drain Impurity Profiles on Performance of Germanium Channel Double-Gated pMISFETs
T. Yamamoto[1], M. Harada[1], N. Taoka[2], Y. Yamashita[1], N. Sugiyama[1] and S. Takagi[2,3], *[1]MIRAI-ASET, [2]MIRAI-AIST and [3]Univ. of Tokyo (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

14:05 C-9-3
Properties of Methyl Boron Nitride Film for Next Generation Low-K Interconnection
S. Tokuyama, M. K. Mazumder, D. Watanabe, C. Kimura, H. Aoki and T. Sugino, *Osaka Univ. (Japan)*

14:25 C-9-4
Effects of Silylation on Electrical and Mechanical Characteristics of Mesoporous Pure Silica Zeolite Films
T. Seo[1], T. Yoshino[2], N. Ohnuki[2], Y. Seino[2], N. Hata[2] and T. Kikkawa[1,2], *[1]Hiroshima Univ. and [2]AIST (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

14:00 D-9-3
CMOS Optical Polarization Analyzer Chip for µTAS
T. Tokuda, S. Sato, M. Nunoshita and J. Ohta, *NAIST (Japan)*

14:15 D-9-4
Label-Free Immunosensing for α-Fetoprotein in Human Plasma using Surface Plasmon Resonance
K. Kawano[1], Y. Teramura[2], M. Oda[3], T. Suzuki[2], H. Kotera[2] and H. Iwata[2], *[1]CREATE-JST, [2]Kyoto Univ. and [3]TERAMECS CO., LTD (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

13:45 E-9-3
MOCVD Growth of GaN-Based LEDs with Naturally Formed Nano-pyramids
C. E. Lee, C. H. Chiu, M. H. Lo, H. W. Huang, T. C. Lu, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ. (Taiwan)*

14:00 E-9-4
A Novel Sn-based Metal Substrate Technology for the Fabrication of Vertical-Structure GaN-Based High Power Light-Emitting Diodes
H. Y. Kuo[1], S. J. Wang[1], K. M. Uang[2], S. L. Chen[1], T. M. Chen[1,2], P. R. Wang[1], C. C. Tsai[1] and H. Kuan[3], *[1]National Cheng Kung Univ., [2]WuFeng Inst. of Tech. and [3]Far East Univ. (Taiwan)*

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

13:55 F-9-3
Origin of Structural Phase Transformation of SiO_2-doped HfO_2
K. Tomida, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

14:15 F-9-4
Characteristics of Pure Ge_3N_4 Dielectric Layers Formed by High-Density Plasma Nitridation
K. Kutsuki, G. Okamoto, T. Hosoi, T. Shimura, K. Yasutake and H. Watanabe, *Osaka Univ. (Japan)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

13:55 G-9-3
A Moving-Object-Localization Hardware Algorithm Employing OR-Amplification of Pixel Activities
Y. Niki, Y. Manzawa, S. Kametani and T. Shibata, *Univ. of Tokyo (Japan)*

14:15 G-9-4
New Reconfigurable Memory Architecture for Parallel Image Processing LSI with Three-Dimensional Structure
S. Kodama, D. Amano, T. Sugimura, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. (Japan)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

14:00 H-9-3
Fabrication of Soluble Semiconductor Thin Film Transistor with Printed Electrodes using h-PDMS Stamp
J. Jo[1], T. M. Lee[1], D. S. Kim[1], K. Y. Kim[1], E. S. Lee[1], K. Y. Park[2] and M. Esashi[3], *[1]KIMM, [2]ITEP and [3]Tohoku Univ. (Korea)*

14:15 H-9-4
Double-Shot Inkjet Printing of Organic Charge-Transfer Compounds
M. Hiraoka[1], T. Hasegawa[1], T. Yamada[1], Y. Takahashi[1], S. Horiuchi[1] and Y. Tokura[1,2], *[1]AIST and [2]Univ. of Tokyo (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

14:00 I-9-3
Fano-Kondo effect in three quantum dots aiming at charge qubit measurement
T. Tanamoto, Y. Nishi and S. Fujita, *Toshiba Corp. (Japan)*

14:15 I-9-4
Study of Single-Charge Polarization on two Charge Qubits Integrated onto a Double Single-Electron Transistor Readout
Y. Kawata[1,3], S. Nishimoto[1], Y. Tsuchiya[1,3], S. Oda[1,3] and H. Mizuta[1,2,3], *[1]Tokyo Tech., [2]Univ. of Southampton and [3]SORST-JST (Japan)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

14:15 J-9-3
A Triple Quantum Dot in a Single Wall Carbon Nanotube
K. Grove-Rasmussen[1,2], H. I. Jørgensen[2], T. Hayashi[1], P. E. Lindelof[2] and T. Fujisawa[1], *[1]NTT Corp. and [2]Univ. of Copenhagen (Japan)*

14:30 J-9-4
Electric Property Control of Carbon Nanotubes by Defects
S. Suzuki[1], J. Hashimoto[1,2], T. Ogino[2] and Y. Kobayashi[1], *[1]NTT Corp. and [2]Yokohama National Univ. (Japan)*

Friday, September 21

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

14:35 A-9-5
CMP-less Co-Integration of Tunable Ni-TOSI CMOS for Low Power Digital and Analog Applications
G. Bidal[1,5], M. Müller[1], S. Denorme[2], D. Aimé[3], M. Rafik[2], A. Cathignol[2], G. Ribes[2], S. Pokrant[1], P. Gouraud[2], T. Kormann[1], G. Chabanne[3], C. Blanc[3], S. Bonnetier[3], D. Barge[1], C. Laviron[4], A. Tarnowka[1], G. Ghibaubo[5], F. Boeuf[2] and T. Skotnicki[2], *[1]NXP Semiconductors, [2]STMicroelectronics, [3]Freescale, [4]CEA-LETI and [5]IMEP (France)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

14:35 B-9-5
A Double-Gate Tunneling Field-Effect Transistor with Silicon-Germanium Source for High-Performance, Low Standby Power, and Low Power Technology Applications
E. H. Toh, G. H. Wang, L. Chan, D. Sylvester, C. H. Heng, G. Samudra and Y. C. Yeo, *National Univ. of Singapore (Singapore)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

14:45 C-9-5
Determination of mechanical properties of porous silica low-k films on Si substrates using orientation dependence of surface acoustic wave
T. Takimura, N. Hata, S. Takada and T. Yoshino, *AIST (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

14:30 D-9-5
In-Situ Surface Infrared Study of DNA Attachment and Hybridization at Si Surfaces
A. Hirano, K. Tanaka, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

14:15 E-9-5
The Aluminum Packaging for LED using Selectively Anodizing Method
K. M. Kim[1], S. H. Shin[2], Y. K. Lee[2], S. M. Choi[2] and Y. S. Kwon[1], *[1]KAIST and [2]Samsung Electro-Mechanics (Korea)*

14:30 E-9-6
The Fabrication of the Circular Ring Laser Resonators by Excimer Laser Assisted Etching at Cryogenic Temperature
M. C. Shih and S. C. Wang, *National Univ. of Kaohsiung (Taiwan)*

14:45 E-9-7
Red emission from ZnO-based double heterojunction diode
T. Ohashi, K. Yamamoto, A. Nakamura and J. Temmyo, *Shizuoka Univ. (Japan)*

Friday, September 21

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

14:35 F-9-5
Surface Treatment of Ge(001) Surface by Radical Nitridation
H. Kondo, M. Fujita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

14:30 H-9-5
Fabrication of Flexible OTFT-backplanes for Active Matrix Electrophoretic Display
M. W. Lee and C. K. Song, *Dong-A Univ. (Korea)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

14:30 I-9-5
Formation and control of 2-qubits exciton state in a coupled quantum dots
K. Goshima[1,2], K. Komori[1,2] and T. Sugaya[1,2], *[1]AIST and [2]CREST-JST (Japan)*

14:45 I-9-6
Decoherence of nuclear spins in a GaAs quantum well probed by a submicron scale all-electrical NMR device
T. Ota[1,2], N. Kumada[1], G. Yusa, [1,3,4], S. Miyashita[5], T. Fujisawa[1] and Y. Hirayama[1,2,4], *[1]NTT Corp., [2]SORST-JST, [3]PRESTO-JST, [4]Tohoku Univ. and [5]NTT-AT (Japan)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

14:45 J-9-5
Single charge sensitivity of single-walled carbon nanotube single-hole transistor
T. Kamimura[1,2], Y. Ohno[1,2] and K. Matsumoto[1,2,3], *[1]Osaka Univ., [2]CREST-JST and [3]AIST (Japan)*

Room 101 (A)

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-10 : Noise and RF
(15:15-17:05)
Chairs: D. Hisamoto (Hitachi Ltd.)
K. Takeuchi (NEC Corp.)

15:15 B-10-1 (Invited)
RTN Effects in Scaled Flash Memory Arrays
A. S. Spinelli, C. M. Compagnoni, R. Gusmeroli, M. Ghidotti and A. L. Lacaita, *Politecnico di Milano (Italy)*

15:45 B-10-2
Analysis of Random Telegraph Signal Noise in Dual and Single Oxide Device And Its Application to CMOS Image Sensor Readout Circuit
H. Lee, Y. Yoon, J. Jeon and H. Shin, *Seoul National Univ. (Korea)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-10 : Nanoscale Characterization
(15:25-16:25)
Chairs: N. Hata (NEDO)
S. Ogawa (Selete)

15:25 C-10-1
Characterization of Line-edge Roughness in Cu/low-k Interconnect Pattern
A. Yamaguchi[1], D. Ryuzaki[1], K. Takeda[1], J. Yamamoto[1], H. Kawada[2] and T. Iizumi[2], *[1]Hitachi, Ltd. and [2]Hitachi High-Technologies Corp. (Japan)*

15:45 C-10-2
Nano-Scale Stress Field Evaluation with Shallow Trench Isolation Structure Assessed by Cathodoluminescence, Raman Spectroscopy, and Finite Element Method Analyses
M. Kodera[1], T. Iguchi[1], N. Tsuchiya[1], M. Tamura[2], S. Kakinuma[3], N. Naka[3] and S. Kashiwagi[3], *[1]Toshiba Corp., [2]Toshiba I. S. Corp. and [3]Horiba, Ltd. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

D-10 : μ-TAS and Medical Applications
(15:15-16:45)
Chairs: K. Sawada (Toyohashi Univ. of Technology)
H. Tabata (The Univ. of Tokyo)

15:15 D-10-1
One-Chip Integration of the Rapid Diagnosis Infectious Disease Chip Based on New Phenomena of DNA Trap and Denature in Nano-Gaps
S. Hashioka[1,2], K. Masu[1] and Y. Horiike[2], *[1]Tokyo Tech. and [2]NIMS (Japan)*

15:30 D-10-2
Droplet device for immunoassay detection
C. H. Chang, S. Hashioka, T. Chikyo and Y. Horiike, *NIMS (Japan)*

Room 202A (E)

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

F-10 : Advanced Process
(15:15-16:35)
Chairs: O. Faynot (CEA-LETI)
T. Tatsumi (NEC Corp.)

15:15 F-10-1
Dependence of Electrical Characteristics on Interfacial Structures of Epitaxial $NiSi_2$/Si Schottky Contacts Formed from Ni/Ti/Si System
O. Nakatsuka, A. Suzuki, S. Akimoto, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*

15:35 F-10-2
A Breakthrough Electronic Lithography Process Through Si Layer for Self Aligning Gates in Planar Double-Gate Transistors for 32nm Node And Below
R. Wacquez[1,2,4], P. Coronel[1], M. P. Samson[1,2], D. Delille[3], L. R. Clement[3], V. Delaye[2], L. Baud[2], N. Loubet[1], J. Bustos[1], A. Pouydebasque[3], B. Guillaumot[1,2], T. Ernst[2], P. Masson[4], J. P. Gouy[2] and T. Skotnicki[1], *[1]STMicroelectronics, [2]CEA-LETI, MINATEC, [3]NXP and [4]L2MP (France)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

G-10 : Connectivity
(15:15-16:35)
Chairs: M. Horiguchi (Renesas Technology Corp.)
T. Komuro (Agilent Technologies International Japan, Ltd.)

15:15 G-10-1
PCA-based Object Detection/Recognition Chip for Wireless Interconnected 3-D Integration
H. Ando, S. Kameda, D. Arizono, N. Fuchigami, K. Kaya, M. Sasaki and A. Iwata, *Hiroshima Univ. (Japan)*

15:35 G-10-2
Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link
A. Kumar, N. Miura and T. Kuroda, *Keio Univ. (Japan)*

Room 304 (H)

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

I-10 : Novel Devices
(15:15-16:45)
Chairs: Y. Uraoka (Nara Inst. of Science and Technology)
B. G. Park (Seoul National Univ.)

15:15 I-10-1
High Performance Germanium Quantum-dot Single-hole Transistors with Self-aligned Electrodes
S. H. Hsu, W. T. Lai and P. W. Li, *National Central Univ. (Taiwan)*

15:30 I-10-2
Single Electron-based Flexible Multi-valued Exclusive-OR Logic Gate
S. J. Kim, C. K. Lee, R. S. Chung, M. S. Kim, E. S. Park, S. J. Shin and J. B. Choi, *Chungbuk National Univ. (Korea)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

J-10 : Carbon Nanotube Devices and Growth Ⅱ
(15:15-16:30)
Chairs: S. Akita (Osaka Prefecture Univ.)
Y. Homma (Tokyo Univ. of Science)

15:15 J-10-1
New Measurement Method of Carbon Nanotube Energy Band Gap
M. Maeda[1,4], T. Kamimura[2,4], S. Iwasaki[2,4] and K. Matsumoto[2,3,4], *[1]Univ. of Tsukuba, [2]Osaka Univ., [3]AIST and [4]CREST-JST (Japan)*

15:30 J-10-2
Self-aligned Fabrication Process for Pd-Contacted and PMMA-Passivated Carbon Nanotube Field-Effect Transistors
L. Rispal, H. Yang, R. Heller, G. Hess, G. Tzschöckel and U. Schwalke, *Darmstadt Univ. of Tech. (Germany)*

Friday, September 21

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
	Area 3: CMOS Devices/Device Physics	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	
	16:05 B-10-3 Simultaneous Extraction of Locations and Energies of Two Independent Traps in Gate Oxide From Four-level RTS noise S. Yang, H. Lee and H. Shin, *Seoul National Univ. (Korea)*	**16:05 C-10-3** Channel Strain in Advanced CMOSFETs Measured Using Nano-Beam Electron Diffraction A. Toda[1], H. Nakamura[2], T. Fukai[2] and N. Ikarashi[1], *[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)*	**15:45 D-10-3** High-Throughput Fluorometric Assay of Enzymatic Reactions on a Microreactor Array Chip T. Ichiki[1,2], Y. Hosoi[1], J. Liu[1], T. Osawa[1], T. Akagi[1], M. Biyani[2] and N. Nemoto[2,3], *[1]Univ. of Tokyo, [2]CREATE-JST and [3]Janusys Corp. (Japan)*	
	16:25 B-10-4 Analog Performance of Asymmetric Schottky Tunneling Source nFET for RF and Mixed-Mode Application R. Jhaveri and J. C. S. Woo, *Univ. of California (USA)*		**16:00 D-10-4** Development of a multi-chip retinal stimulator for in vivo experiments toward retinal prosthesis T. Tokuda[1], R. Asano[1], Y. Terasawa[2], M. Nunoshita[1], K. Nakauchi[3], T. Fujikado[3], Y. Tano[3] and J. Ohta[1], *[1]NAIST, [2]NIDEK Co., Ltd. and [3]Osaka Univ. (Japan)*	

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**		**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
15:55 F-10-3 Contact Technology employing Nickel-Platinum Germanosilicide Alloys for P-Channel FinFETs with Silicon-Germanium Source and Drain Stressors R. T. P. Lee[1], K. M. Tan[1], A. E. J. Lim[1], T. Y. Liow[1], X. C. Chen[1], M. Zhu[1], A. T. Y. Koh[1], K. M. Hoe[3], S. Y. Chow[2], G. Q. Lo[3], G. S. Samudra[1], D. Z. Chi[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Inst. of Materials Research and Engineering and [3]Inst. of Microelectronics (Singapore)*	**15:55 G-10-3** Scaling Characteristics of Si On-chip Integrated Antennas K. Kimoto, N. Sasaki and T. Kikkawa, *Hiroshima Univ. (Japan)*		**15:45 I-10-3** Self-Aligned Dual-Gate Single-Electron Transistors (DG-SETs) S. Kang[1], D. H. Kim[2], I. H. Park[1], J. H. Kim[1], J. E. Lee[1], J. D. Lee[1] and B. G. Park[1], *[1]Seoul National Univ. and [2]Kookmin Univ. (Korea)*	**15:45 J-10-3** Individual Carbon Nanotubes as Nano-incandescent S. Akita[1,3] and Y. Nakayama[2,3], *[1]Osaka Prefecture Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)*
16:15 F-10-4 An Optimized Silicidation Technique for Source and Drain of FINFET K. Okuyama, A. Sugimura and H. Sunami, *Hiroshima Univ. (Japan)*	**16:15 G-10-4** A Fully Integrated SiGe Optical Receiver Using Differential Active Miller Capacitor for 4.25 Gb/s Fiber Channel Application J. C. Huang, K. S. Lai and K. Y. J. Hsu, *National Tsing Hua Univ. (Taiwan)*		**16:00 I-10-4** Design Control of Random Dopant-induced Multiple-Tunnel-Junction Arrays for Turnstile Operation D. Moraru, K. Yokoi, H. Ikeda and M. Tabe, *Shizuoka Univ. (Japan)*	**16:00 J-10-4** A Field-Emission Device with Novel Self-Focus Gate Structure H. W. Chen, K. C. Lin, C. P. Juan, Y. S. Leou, Y. Y. Hsu and H. C. Cheng, *National Chiao Tung Univ. (Taiwan)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
	Area 3: CMOS Devices/Device Physics	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	
	16:45 B-10-5 Frequency Dependence of Measured MOSFET Distortion Characteristic T. Minami[1], Y. Takeda[1], M. Miyake[1], M. Miura-Mattausch[1], H. J. Mattaush[1], T. Ohguro[2], T. Iizuka[2], M. Taguchi[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]STARC (Japan)*		**16:15 D-10-5** UWB Imaging for Early Breast Cancer Detection by Confocal Algorithm X. Xiao[1,2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Tianjin Univ. (Japan)*	
			16:30 D-10-6 Development of a CMOS-based Neural Imaging and Interface Device D. C. Ng, T. Mizuno, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, *NAIST (Japan)*	

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**		**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
			16:15 I-10-5 Acoustic Wave Manipulation by Phased Operation of Two-Dimensionally Arrayed Nanocrystalline Silicon Ultrasonic Emitters B. Gelloz, M. Sugawara and N. Koshida, *Tokyo Univ. of Agri. and Tech. (Japan)*	**16:15 J-10-5** Combinatorial Control of Catalyst Nanoparticles for Customized Production of Single- and Multi-Walled Carbon Nanotubes S. Noda, K. Hasegawa, H. Sugime, K. Kakehi, S. Maruyama and Y. Yamaguchi, *Univ. of Tokyo (Japan)*
			16:30 I-10-6 New Type Oxygen Sensor Using Micro-fabricated Layered Semiconductor Compound T. Nugroho, A. Ikeda, Y. Kakihara, H. Kuriyaki and Y. Kuroki, *Kyushu Univ. (Japan)*	

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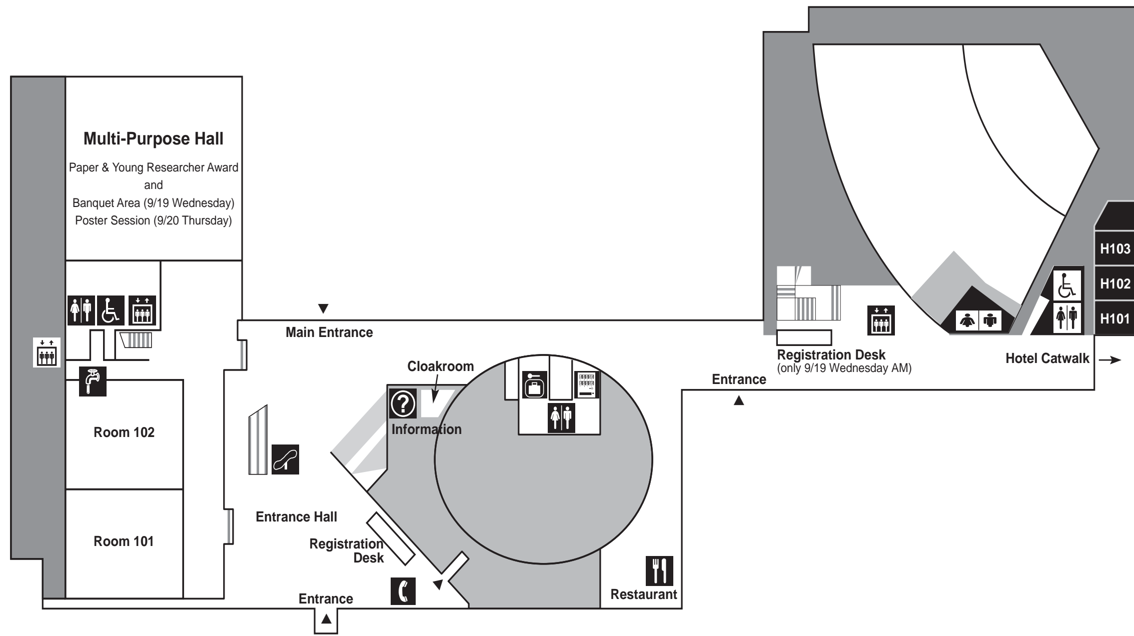
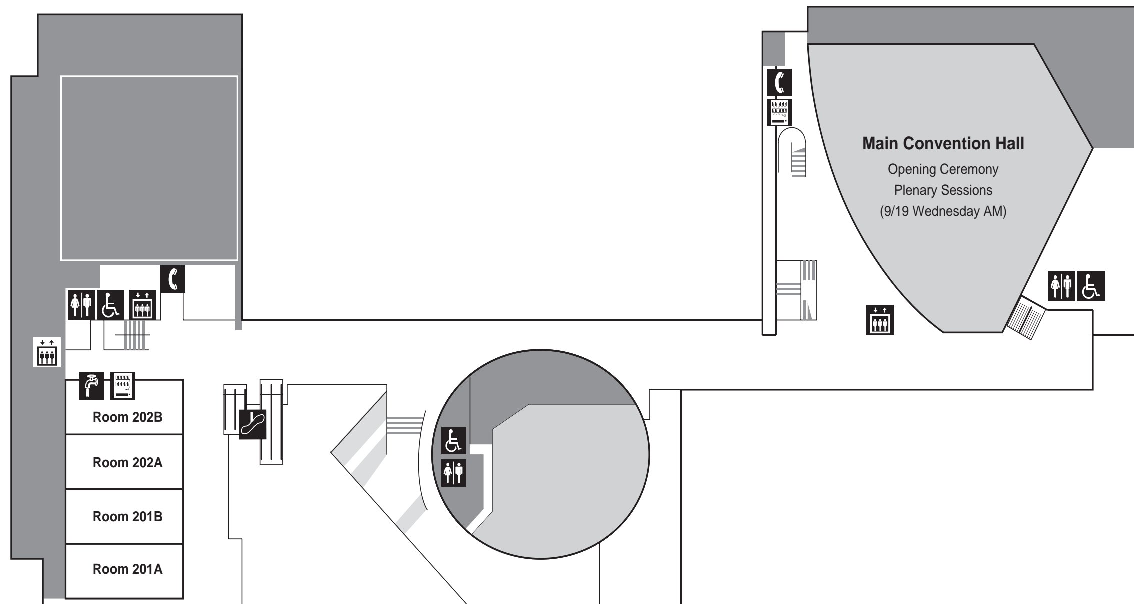
1F

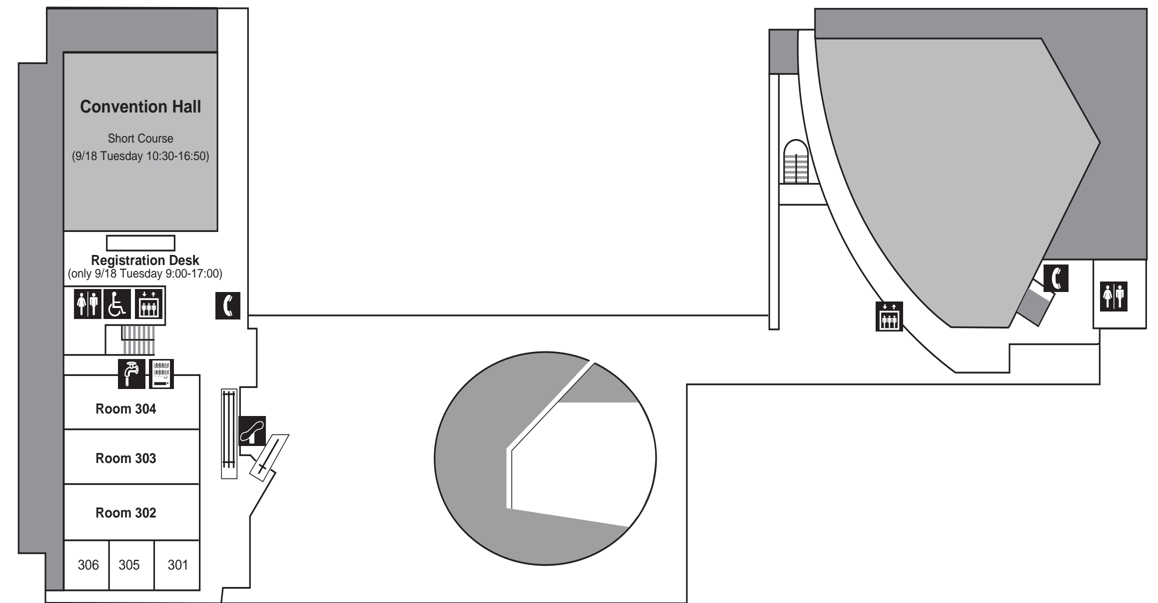


2F

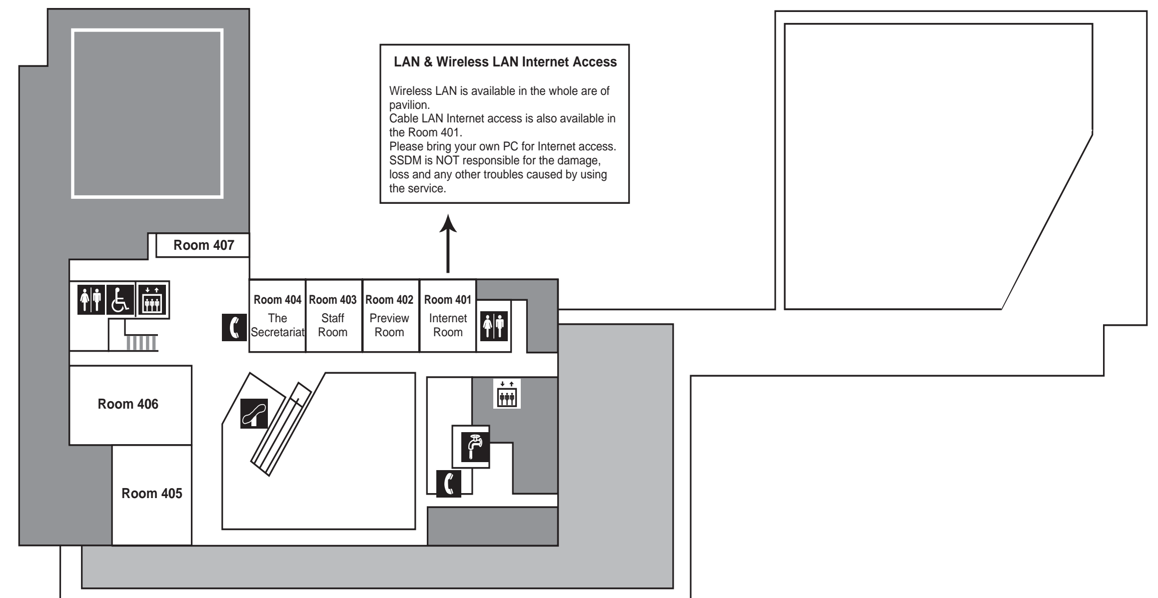


SSDM 2007 Floor Guide, International Congress Center EPOCHAL TSUKUBA

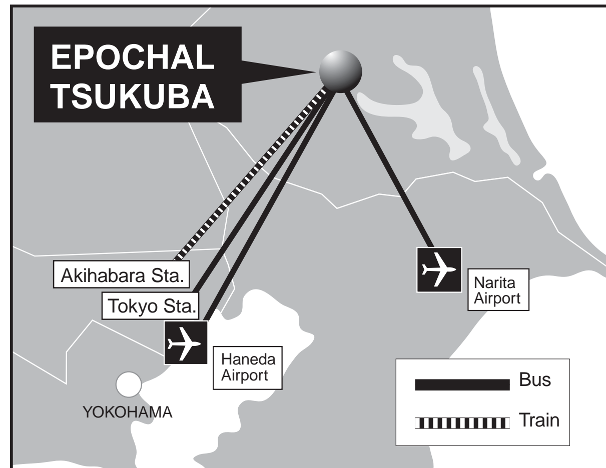
3F

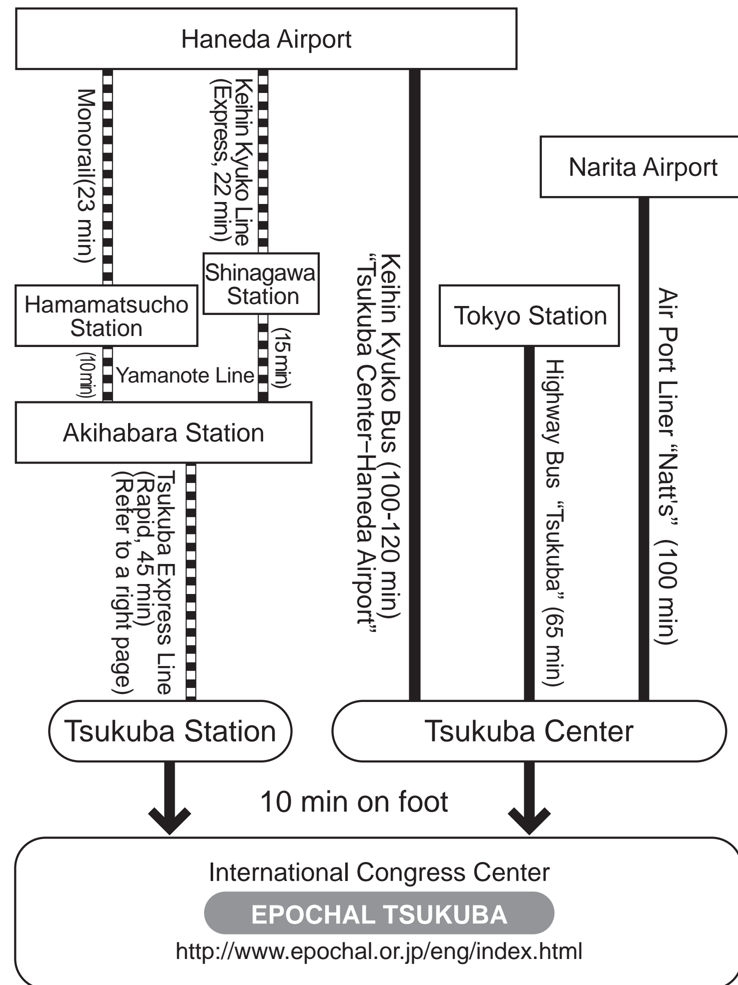


4F



ACCESS TO EPOCHAL TSUKUBA





Tsukuba Express Time Table (Weekdays)

To Tsukuba (@Akihabara Sta.)

Hour					
5	30	45			
6	05	20	43		
7	00	12	24	37	45
8	02	10	25	31	46
9	01	15	30	45	
10	00	15	30	45	
11	00	15	30	45	
12	00	15	30	45	
13	00	15	30	45	
14	00	15	30	45	
15	00	15	30	45	
16	00	15	30	45	52
17	00	17	30	40	
18	00	10	20	30	40
19	00	10	20	30	40
20	00	12	36		
21	00	12	36		
22	00	15	45		
23	00	15	30		

To Akihabara (@Tsukuba Sta.)

Hour					
5	07	28	42		
6	12	34	56	57	
7	12	26	27	42	56
8	12	26	32	47	
9	07	18	31	41	48
10	11	18	41	48	
11	11	18	41	48	
12	11	18	41	48	
13	11	18	41	48	
14	11	18	41	48	
15	11	18	30	41	48
16	11	18	39	52	
17	09	12	32	49	52
18	02	19	22	42	
19	02	20	25	38	57
20	01	18	24	49	
21	08	16	45		
22	08	15	40		
23	05	14			

Red: Rapid (45 min) **Blue: Section Rapid (52 min)** **Black: Local**