Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
A-7 : Metal Gate-Ⅱ (9:00-10:30) Chairs: T. Nabatame (ASET) K. Shiraishi (Univ. of Tsukuba)	B-7 : Stress Enhancement Technologies (9:00-10:20) Chairs: F. Boeuf (STMicroelectronics) H. Wakabayashi (Sony Corp.)	C-7 : Interconnects for RF and Mixed Signal Application (9:00-10:30) Chairs: Y. Hayashi (NEC Corp.) M. Matsuura (Renesas Technology Corp.)	D-7 : Nano-Bio Devices Ⅰ (9:00-10:30) Chairs: T. Nishimoto (Shimadzu Corp.) H. Tabata (Univ. of Tokyo)	E-7 : All-Optical Light Control (9:00-10:30) Chairs: R. Akimoto (AIST) Y. Lee (Hitachi, Ltd.)
9:00 A-7-1 (Invited) Schottky Barrier and Stability of Metal/ High-k Interfaces; Theoretical View T. Nakayama, *Chiba Univ. (Japan)*	**9:00 B-7-1** NMOS Current Enhancement and Layout Dependency Improvement by Using Atomic Layer Deposition SIN Spacer H. Nagai, K. Ookoshi, H. Morioka, T. Mori, M. Kojima, Y. Takao, M. Kase and K. Hashimoto, *Fujitsu Ltd. (Japan)*	**9:00 C-7-1** Impacts of Cu/TaN Electrode on the Electrical Properties of Metal-insulator-metal (Ba,Sr)TiO_3 Thin-film Capacitors W. F. Wu[1], K. C. Tsai[1,2], C. G. Chao[2], J. T. Lee[2], W. C. Chang[3], T. K. Kang[3], G. S. Jheng[4] and J. Y. Lin[4], *[1]National Nano Device Labs., [2]National Chiao Tung Univ., [3]Feng Chia Univ. and [4]National Yunlin Univ. of Sci. and Tec. (Taiwan)*	**9:00 D-7-1 (Invited)** Si based Planer Type Ion-channel Biosensor and Its Applications T. Urisu[1,2], H. Uno[2], T. Asano[2], M. Y. Li[1], R. Tero[1,2] and K. Ishii[3], *[1]Inst. for Molecular Sci., [2]Graduate Univ. for Advanced Studies and [3]Chubu Univ. (Japan)*	**9:00 E-7-1 (Invited)** GaN-Based High-Speed Intersubband Optical Switches N. Iizuka[1], K. Kaneko[1], N. Suzuki[1], C. Kumtornkittikul[2], T. Shimizu[2], M. Sugiyama[2] and Y. Nakano[2], *[1]Toshiba Corp. and [2]Univ. of Tokyo (Japan)*
9:30 A-7-2 Anomalous positive V_{fb} shift in $HfAlO_x$ MOS gate stacks W. Wang[1], K. Akiyama[2], W. Mizubayashi[1], M. Ikeda[2], H. Ota[1], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, AIST, [2]MIRAI-ASET, AIST and [3]Univ. of Tokyo (Japan)*	**9:20 B-7-2** In-situ Doped Embedded-SiGe Source/Drain Technique for 32 nm-node pMOSFET H. Okamoto, A. Hokazono, K. Adachi, N. Yasutake, H. Itokawa, S. Okamoto, M. Kondo, H. Tsujii, T. Ishida, N. Aoki, M. Fujiwara, S. Kawanaka, A. Azuma and Y. Toyoshima, *Toshiba Corp. (Japan)*	**9:20 C-7-2** Fully Analytical Modeling of Cu Interconnects Up to 110 GHz J. D. Jin[1], S. S. H. Hsu[1], T. J. Yeh[2], M. T. Yang[2] and S. Liu[2], *[1]National Tsing Hua Univ. and [2]Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)*	**9:30 D-7-2** An immunosensor based on N-doped multiwalled carbon nanotubes S. A. Contera, H. J. Burch, M. de Planque, K. Voitchovsky and J. F. Ryan, *Univ. of Oxford (UK)*	**9:30 E-7-2** Characterization of Narrow Mesa Width Waveguide for All Optical Switching Device Based on Intersubband Transition in II-VI Based Quantum Wells K. Akita, R. Akimoto, C. Guangwei, T. Hasama and H. Ishikawa, *AIST (Japan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 10: Organic Materials Science, Device Physics, and Applications**		**Area 4: Advanced Memory Technology**
F-7 : Material Characterization (9:00-10:15) Chairs: K. Kobayashi (Waseda Univ.) T. Iwai (Fujitsu Labs. Ltd.)	G-7 : Emerging Devices (9:00-10:30) Chairs: T. Hashizume (Hokkaido Univ.) R. Hattori (Mitsubishi Electric Corp.)	H-7 : Organic Transistor Ⅰ (9:00-10:30) Chairs: T. Minakata (Asahi-KASEI Corp.) K. Fujita (Kyushu Univ.)		J-7 : DRAM Ⅱ (9:00-10:20) Chairs: I. Asano (Elpida Memory, Inc.) M. Moniwa (Renesas Technology Corp.)
9:00 F-7-1 (Invited) In-Situ X-Ray Diffraction during Semiconductor Nanostructure Growth M. Takahasi, *JAEA (Japan)*	**9:00 G-7-1 (Invited)** Growth of InAs Channel HEMT Structure on Si substrate and It's Possible Application for Low Power Logic E. Y. Chang, H. Yamaguchi, Y. C. Lin, M. Ueki, Y. Hirayama and C. Y. Chang, *National Chiao Tung Univ. (Taiwan)*	**9:00 H-7-1 (Invited)** Jet-pinted Polymer Transistor Display Backplanes R. A. Street, A. C. Arias and J. H. Daniel, *Palo Alto Research Center (USA)*		**9:00 J-7-1** $Ru/TiO_2/ZrO_2/TiN$ ($RIT\text{-}TiO_2/ZrO_2$) Capacitor Structure for the 50nm DRAM Device and beyond J. S. Lim, K. C. Kim, K. H. Lee, J. H. Choi, Y. S. Tak, W. D. Kim, J. Y. Kim, K. Cho, Y. Kim, J. H. Chung, Y. S. Kim, S. T. Kim and W. Han, *Samsung Electronics Co.,Ltd. (Korea)*
9:30 F-7-2 *In situ* Analysis for Initial Formation Process of Gold Nanoparticles in Discharge in Aqueous Solution C. Miron[1], M. A. Bratescu[2], T. Ishizaki[1], N. Saito[1] and O. Takai[2], *[1]Nagoya Univ. and [2]EcoTopia Sci. Inst. (Japan)*	**9:30 G-7-2** N-channel MOSFETs with *In-situ* Silane-Passivated Gallium Arsenide Channel and CMOS-Compatible Palladium-Germanium Contacts H. C. Chin[1], M. Zhu[1], K. M. Hoe[2], G. S. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*	**9:30 H-7-2** Frequency Dependence of Displacement Current and Channel Current in Pentacene Thin-Film Transistors S. Suzuki, Y. Yasutake and Y. Majima, *Tokyo Tech. (Japan)*		**9:20 J-7-2** Electrical Properties of TiO/LaTiO/TiO Stacked Thin Films H. Hara[1], M. Tanioku[2], M. Yamato[1] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Elpida Memory, Inc. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

9:50 A-7-3
Effect of Ultra-thin Al_2O_3 Insertion on Fermi-level Pinning at Metal/Ge Interface
T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

10:10 A-7-4
Systematic studies on Fermi level pining of Hf-based high-k gate stacks
K. Shiraishi[1,2], Y. Akasaka[3,1,7], G. Nakamura[3,7], M. Kadoshima[3], H. Watanabe[4], K. Ohmori[5], T. Chikyow[6], K. Yamabe[1], Y. Nara[3], Y. Ohji [3] and K. Yamada[5], *[1]Univ. of Tsukuba, [2]CREST-JST, [3]SELETE, [4]Osaka Univ., [5]Waseda Univ., [6]NIMS and [7]Tokyo Electron Inc. (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

9:40 B-7-3
Principal Guideline of Stress Design for Ion Enhancement in Advanced MOSFET Structure with Dual Stress Liner Technique
M. Nishikawa[1], H. Nomura[1], T. Miyashita[2], M. Kojima[1], Y. Takao[1] and K. Hashimoto[1], *[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd. (Japan)*

10:00 B-7-4
Study of Stress from Discontinuous SiN Liner for Fully-Silicided Gate Process
T. Yamashita[1,2], Y. Nishida[1], T. Okagaki[1], Y. Miyagawa[1], J. Yugami[1], H. Oda[1], Y. Inoue[1] and K. Shibahara[2], *[1]Renesas Tech. Corp. and [2]Hiroshima Univ. (Japan)*

10:20 B-7-5
Strained N-channel FinFETs with High-stress Nickel Silicide-Carbon Contacts and Integration with FUSI Metal Gate Technology
T. Y. Liow[1,2], R. T. P. Lee[1], K. M. Tan[1], M. Zhu[1], K. M. Hoe[2], G. S. Samudra[1], N. Balasubramanian[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

9:40 C-7-3
A Small Area, 3-Dimensional On-chip Inductors for High-speed Signal Processing under Low Power Supply Voltages
K. Hijioka, A. Tanabe, Y. Amamiya and Y. Hayashi, *NEC Corp. (Japan)*

10:00 C-7-4 (Invited)
Wiring technology for analog and mixed signal LSIs
A. Matsuzawa, *Tokyo Tech. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

9:45 D-7-3
Reverse Electroporation with Carbon Nanotubes-loaded Electrode for Highly Efficient Gene Transfer
Y. Inoue[1], H. Fujimoto[1], T. Ogino[2] and H. Iwata[1], *[1]Kyoto Univ. and [2]Yokohama National Univ. (Japan)*

10:00 D-7-4
Rapid and High Sensitive Detection of Bacteria Sensor using a Porous Ion Exchange Film
K. Miyano[1], H. Aoki[1], S. Hotta[1], N. Fujiwara[2], D. Yano[3], K. Sano[3], K. Yamanaka[3], C. Kimura[1] and T. Sugino[1], *[1]Osaka Univ., [2]TRI-Osaka and [3]Organo Corp. (Japan)*

10:15 D-7-5
Ion-Sensitive Field Effect Transistor Based on Silicon and Zinc Oxide for DNA Sensor
M. Seki, T. Uno, M. Noguchi and H. Tabata, *Univ. of Tokyo (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

9:45 E-7-3
Saturation characteristics simulation of Intersubband absorption for [(CdS/ZnSe/BeTe)/(ZnSe/BeTe)] coupled quantum wells
G. W. Cong, R. Akimoto, K. Akita, T. Hasama and H. Ishikawa, *AIST (Japan)*

10:00 E-7-4
Magneto-Optical (Cd,Mn)Te/(Cd,Zn)Te Quantum Well Waveguide with Broadband Operation Optical Isolator
M. C. Debnath, V. Zayets and K. Ando, *AIST (Japan)*

10:15 E-7-5
Passive Optical Alignment with High Accuracy for Low-Loss Optical Interposer
M. Fujiwara[1,2], S. Terada[1], Y. Shirato[1], H. Owari[1], K. Watanabe[1], M. Matsuyama[1], K. Takahama[1], T. Mori[1], K. Miyao[1], K. Choki[1], T. Fukushima[2], T. Tanaka[2] and M. Koyanagi[2], *[1]Sumitomo Bakelite Co., Ltd and [2]Tohoku Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:45 F-7-3
Scanning Surface Hall Potentiometry on Semiconductor Wafers
Y. Hidaka, D. Maruyama, J. Uchikoshi, M. Morita and K. Arima, *Osaka Univ. (Japan)*

10:00 F-7-4
Investigation of FePt Nano-Dots Fabricated by Self-Assembled Nano-Dot Deposition Method Using X-ray Photoelectron Spectroscopy
M. Murugesan[1], J. C. Bea[1], C. K. Yin[2], H. Nohira[3], E. Ikenaga[4], T. Hattori[3], M. Nishijima[2], T. Fukushima[2], T. Tanaka[2], M. Miyao[5] and M. Koyanagi[2], *[1]JST, [2]Tohoku Univ., [3]Musashi Inst. of Tech., [4]JASRI and [5]Kyushu Univ. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

9:45 G-7-3
Improved electrical characteristics of Pt/Gd_2O_3/GaAs MOS capacitors with surface preparation procedures
C. C. Cheng[1], C. H. Chien[1,2], G. L. Luo[2], C. K. Tseng[1], H. C. Chiang[1], C. H. Yang[2] and C. Y. Chang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

10:00 G-7-4
Performance and Stability of ZnO/ZnMgO Hetero-MIS FETs
S. Sasa, T. Hayafuji, M. Kawasaki, K. Koike, M. Yano and M. Inoue, *Osaka Inst. of Tech. (Japan)*

10:15 G-7-5
The Effect of Rapid Thermal Annealing on the Electrical Characteristics of ZnO TFTs
K. Remashan, D. K. Hwang, S. J. Park and J. H. Jang, *GIST (Korea)*

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

9:45 H-7-3
Analysis of charge accumulation in pentacene field effect transistor with ferroelectric gate insulator on the basis of Maxwell-Wagner model
R. Tamura, S. Yoshita, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

10:00 H-7-4
An Analytic Current-Voltage Equation for Top-contact OTFTs Including the Effects of Variable Series Resistance
K. D. Jung, B. J. Kim, Y. C. Kim, B. G. Park, H. Shin and J. D. Lee, *Seoul National Univ. (Korea)*

10:15 H-7-5
Potential Fluctuation within a Crystalline Domain in Pentacene Thin Film Transistors and its Origin
N. Ohashi, H. Tomii, R. Matsubara, M. Sakai, K. Kudo and M. Nakamura, *Chiba Univ. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

9:40 J-7-3
Nitrogen Profile Study for SiON Gate Dielectrics of Advanced DRAM
S. Murakawa[1,2], M. Takeuchi[3], M. Honda[3], S. Ishizuka[3], T. Nakanishi[3], Y. Hirota[3], T. Sugawara[1], Y. Tanaka[1], Y. Akasaka[1], A. Teramoto[2], S. Sugawa[2] and T. Ohmi[2], *[1]Tokyo Electron Ltd., [2]Tohoku Univ. and [3]Tokyo Electron AT Ltd. (Japan)*

10:00 J-7-4
Effect of Boron-Nitride Formation at the Interface of Diffusion Barrier in Tungsten Polymetal Gate Stacks on Gate Interfacial Resistance
M. G. Sung, K. Y. Lim, Y. S. Kim, H. J. Cho, S. R. Lee, S. A. Jang, M. S. Joo, J. H. Lee, T. Y. Kim, T. O. Youn, J. H. Kim, G. O. Kim, Y. T. Hwang, H. S. Yang, J. C. Ku and J. W. Kim, *Hynix Semiconductor Inc. (Korea)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Break				
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
A-8 : High-k/Metal Gate Transistor (10:45-12:05) Chairs: H. Fukutome (Fujitsu Labs. Ltd.) Y. Tsunashima (Toshiba Corp.)	B-8 : Modeling and Simulation (10:45-12:25) Chairs: A. Hokazono (Toshiba Corp.) Y. Momiyama (Fujitsu Labs. Ltd.)	C-8 : Interconnect Reliability (10:45-12:15) Chairs: K. Ueno (Shibaura Inst. of Technology) M. Kodera (Toshiba Corp.)	D-8 : Nano-Bio Devices Ⅱ (10:45-12:15) Chairs: I. Yamashita (Nara Inst. of Sci. and Tech.) S. Antoranz Contera (Univ. of Oxford)	E-8 : Lasers and LEDs (10:45-12:15) Chairs: M. Ezaki (Toshiba Corp.) M.Gotoda (Mitsubishi Electric Corp.)
10:45 A-8-1 Production-Worthy HfSiON Gate Dielectric Fabrication Enabling EOT Scalability Down to 0.86 nm and Excellent Reliability by Polyatomic Layer Chemical Vapor Deposition Technique D. Ishikawa[1], S. Kamiyama[1], A. Sano[2], S. Horii[2], T. Aoyama[1] and Y. Nara[1], *[1]Selete and [2]Hitachi Kokusai Electric Inc. (Japan)*	**10:45 B-8-1** Capacitive Parameter Extraction for Nanometer-Size Field-Effect Transistors H. Inokawa[1], A. Fujiwara[2], K. Nishiguchi[2] and Y. Ono[2], *[1]Shizuoka Univ. and [2]NTT Corp. (Japan)*	**10:45 C-8-1 (Invited)** Stress Migration Phenomenon in Narrow Copper Interconnects T. Nakamura and T. Suzuki, *Fujitsu Labs. Ltd. (Japan)*	**10:45 D-8-1 (Invited)** Bio-Nano Approaches to Fabrication of Quantum Dot Floating Gate Flash Memories S. K. Banerjee[1], S. Tang[1], C. Mao[2], J. Sarkar[1], H. Liu[1], D. Shahrjerdi[1], C. H. Lee[1] and J. D. Trent[3], *[1]Univ. of Texas at Austin, [2]Univ. of Oklahoma and [3]NASA Ames Research Center (USA)*	**10:45 E-8-1 (Invited)** Widely Tunable Integrated DBR Laser Array with Fast Wavelength Switching S. Tsuji[1,2], H. Arimoto[1,2], T. Tsuchiya[1,2], T. Kitatani[1,2], K. Shinoda[1,2], T. Otoshi[1] and M. Aoki[1,2], *[1]Hitachi, Ltd. and [2]OITDA (Japan)*
11:05 A-8-2 Tinv Scaling and Jg Reducing for nMOSFET with $HfSi_x/HfO_2$ Gate Stack by Interfacial Layer Formation Using Ozone Water Treatment Process I. Oshiyama[1], K.Tai[1], T. Hirano[1], S. Yamaguchi[1], K. Tanaka[1], Y. Hagimoto[1], T. Uemura[1], T. Ando[1], K. Watanabe[1], R. Yamamoto[1], S. Kanda[1], J. Wang[1], Y. Tateshita[1], H. Wakabayashi[1], Y. Tagawa[1], M. Tsukamoto[1], H. Iwamoto[1], M. Saito[1], M. Oshima[2], S. Toyoda[2], N. Nagashima[1] and S. Kadomura[1], *[1]Sony Corp. and [2]Univ. of Tokyo (Japan)*	**11:05 B-8-2** Study of Parasitic Resistance Behavior and Its Extraction Method on Deeply Scaled MOSFETs H. Tsujii, A. Hokazono, M. Fujiwara, S. Kawanaka, A. Azuma, N. Aoki and Y. Toyoshima, *Toshiba Corp. (Japan)*	**11:15 C-8-2** Improvement of Adhesion at the Interface between Low-k Spin-on Dielectric and underlying SiCO Barrier by Plasma Treatments Y. Takigawa, S. Nakao, M. Shiohara, N. Oda and S. Ogawa, *Selete (Japan)*	**11:15 D-8-2** Floating Gate MOS Capacitor with High-Density Nanodots Array Produced by Protein Supramolecule K. Yamada[1,2], S. Yoshii[1], S. Kumagai[1], A. Miura[2], Y. Uraoka[2], T. Fuyuki[2] and I. Yamashita[1,2,3], *[1]Matsushita Electric Industrial Co., Ltd., [2]NAIST and [3]CREST-JST (Japan)*	**11:15 E-8-2** High Density Two Dimensional LED Arrays Using Single Crystal Semiconductor Thin Films T. Suzuki, H. Fujiwara, T. Sagimori, T. Igari, H. Furuta, Y. Nakai, I. Abiko, M. Sakuta and M. Ogihara, *Oki Digital Imaging Corp. (Japan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Break				
		Area 10: Organic Materials Science, Device Physics, and Applications	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 4: Advanced Memory Technology**
		H-8 : Organic Transistor Ⅱ (10:45-12:15) Chairs: K. Nomoto (Sony Corp.) K. Kudo (Chiba Univ.)	I-8 : Novel Nanostructure Devices (10:45-12:00) Chairs: M. Watanabe (Tokyo Tech.) H. Mizuta (Tokyo Tech.)	J-8 : FeRAM/MRAM (10:45-12:05) Chairs: T. Eshita (Fujitsu Ltd.) H. Jeong (Samsung Electronics Co. Ltd.)
		10:45 H-8-1 Hall effect measurements of polycrystalline pentacene TFTs with double gate structures Y. Takamatsu, T. Sekitani and T. Someya, *Univ. of Tokyo (Japan)*	**10:45 I-8-1** Self-Assembling Formation of Ni Nanodots on SiO_2 Induced by Remote H_2 -plasma Treatment and Their Electrical Charging Characteristics K. Makihara, K. Shimanoe, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*	**10:45 J-8-1** Improvement of Thermal Stability of MRAM Device with SiN Protective Film Deposited by HDP CVD K. Suemitsu[1], Y. Kawano[2], H. Utsumi[1], H. Honjo[1], R. Nebashi[1], S. Saito[1], N. Ohshima[1], T. Sugibayashi[1], H. Hada[1], T. Nohisa[2], T. Shimazu[2], M. Inoue[2] and N. Kasai[1], *[1]NEC Corp. and [2]Mitsubishi Heavy Industries, Ltd. (Japan)*
		11:00 H-8-2 Probing of channel formation in organic field effect transistors by optical second harmonic generation measurement E. Lim, H. S. Lee, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*	**11:00 I-8-2** Reduction of a Ferritin Core Embedded in Silicon Oxide Film for An Application to Floating Gate Memory T. Matsumura[1], A. Miura[1], Y. Uraoka[1], T. Fuyuki[1], S. Yoshii[2] and I. Yamashita[1,2,3], *[1]NAIST, [2]Matsushita Electric Industrial Co., Ltd. and [3]CREST-JST (Japan)*	**11:05 J-8-2** Two-Dimensional Electron Gas Switching in an Ultra Thin Epitaxial ZnO Layer on a Ferroelectric Gate Structure Y. Kaneko, H. Tanaka, Y. Kato and Y. Shimada, *Matsushita Electric Industrial Co., Ltd. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

11:25 A-8-3
Highly anufacturable CMOSFETs with Single High-k (HfLaO) and Dual Metal Gate Integration Process
X. P. Wang[1,2,3], M. F. Li[1,2,4], H. Y. Yu[3], J. J. Yang[1], C. X. Zhu[1], W. S. Hwang[1], W. Y. Loh[2], A. Y. Du[2], J. D. Chen[1,2], A. Chin[5], S. Biesemans[3], G. Q. Lo[2] and D. L. Kwong[2], *[1]National Univ. of Singapore, [2]Inst. of Microelectronics, [3]IMEC, [4]Fudan Univ. and [5]National Chiao Tung Univ. (Singapore)*

11:45 A-8-4
Highly Manufacturable and Cost-effective Single Ta_xC / $Hf_xZr_{(1-x)}O_2$ Gate CMOS Bulk Platform for LP Applications at the 45nm Node and Beyond
M. Müller[1,4], C. Hobbs[2], A. Zauner[1], S. Barnola[5], T. Salvetat[5], S. Lhostis[3], S. Couderc[3], P. Perreau[5], D.H. Triyoso[2], M. Raymond[2], E. Luckowski[2], M. Rafik[3], A. Cathignol[3], G. Ribes[3], D. Fleury[3], K. Romanjek[1], S. Pokrant[1], S. Jullian[1], P. Morin[3], M. Aminpur[2], P. Gouraud[3], C. Laviron[5], S. Zoll[3], P. Garnier[1] and F. Salvetti[1], *[1]NXP Semiconductors, [2]Freescale, [3]STMicroelectronics, [4]NXP Semiconductors Research and [5]CEA-LETI (France)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

11:25 B-8-3
Two-step Inverse Modeling for Estimation of Channel Impurity Pile-up
T. Nagumo[1], K. Takeuchi[1], Y. Akiyama[2] and M. Hane[1], *[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)*

11:45 B-8-4
Discrete-Dopant-Fluctuated Threshold Voltage Roll-Off in Sub-16nm Bulk FinFETs
Y. Li, C. H. Hwang, H. M. Huang and T. C. Yeh, *National Chiao Tung Univ. (Taiwan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

11:35 C-8-3
Effect of temperature and film thickness on resistivity of CoWP
J. Gambino[1], F. Chen[1], S. Mongeon[1], D. Meatyard[1], E. Adams[1], P. Dehaven[1], C. Cabral[2] and I. Ivanov[3], *[1]IBM, [2]IBM T. J. Watson Research Center and [3]Blue29, LLC (USA)*

11:55 C-8-4
Highly Reliable Cu Interconnect using Low Hydrogen Silicon Nitride Film Deposited at Low Temperature for Cu-Diffusion Barrier
T. Murata, K. Kono, Y. Tsunemine, M. Fujisawa, M. Matsuura, K. Asai and M. Kojima, *Renesas Tech. Corp. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

11:45 D-8-4
Microfluidic Amperometric Biochips Based on Carbon Nanotube Arrayed Electrodes
Y. Tsujita[1], K. Maehashi[1], K. Matsumoto[1], H. Kwon[2], Y. Takamura[2] and E. Tamiya[1], *[1]Osaka Univ. and [2]JAIST (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

11:30 E-8-3
Improvement of Kink-Free Light Output for Fiber Pump Semiconductor Lasers
N. Shomura and T. Numai, *Ritsumeikan Univ. (Japan)*

11:45 E-8-4
Multiwavelength emitting InGaN/GaN quantum well grown on V-shaped GaN ($1\bar{1}01$) microfacet
J. W. Ju[1], L. W. Jang[1], S. J. Lee[2], J. H. Baek[2] and I. H. Lee[1], *[1]Chonbuk National Univ. and [2]Korea Photonics Tech. Inst. (Korea)*

Room 202B (F)

Room 303 (G)

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

11:15 H-8-3
Study of Pentacene-Based Organic Thin Film Transistor with PMMA as Insulator
T. S. Huang, Y. K. Su and B. C. Wang, *National Cheng Kung Univ. (Taiwan)*

11:30 H-8-4
Transient Current Characteristics of Organic Field Effect Transistors with Polymer and Inorganic Gate Insulators
K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, T. Kodzasa and T. Kamata, *AIST (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

11:15 I-8-3
Characterization of Multistep Electron Charging and Discharging of Silicon-Quantum-Dots Floating Gate by Applying Pulsed Gate Biases
R. Matsumoto, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

11:30 I-8-4
Photon Position Detector Consisting of Single-Electron Devices
A. K. Kikombo[1], M. Tabe[2] and Y. Amemiya[1], *[1]Hokkaido Univ. and [2]Shizuoka Univ. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

11:25 J-8-3
Manufacturable High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process
K. R. Udayakumar[1], T. S. Moise[1], S. R. Summerfelt[1], K. Boku[1], J. Rodriguez[1], K. Remack[1], J. Gertas[1], M. Arendt[1], G. Shinn[1], J. Eliason[2], R. Bailey[2] and P. Staubs[2], *[1]Texas Instruments Inc. and [2]Ramtron International Corp. (USA)*

11:45 J-8-4
Endurance Characterization of Ferroelectric Cell in 64Mb FRAM Device By Analyzing the Space Charge Concentration
E. S. Lee, Y. M. Kang, D. J. Jung, H. H. Kim, Y. K. Hong, J. H. Park, S. K. Kang, J. H. Kim, H. S. Kim, W. W. Jung, W. S. Ahn, J. Y. Jung, J. Y. Kang, D. Y. Choi, H. K. Goh, S. Y. Kim, S. Y. Lee and H. S. Jeong, *Samsung Electronics Co., Ltd. (Korea)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

Room 102 (B)

Area 3: CMOS Devices/Device Physics

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

12:00 D-8-5
Fabrication of single electron transistor using cage-shaped protein supramolecule
S. Kumagai[1], S. Yoshii[1], N. Matsukawa[1], R. Tsukamoto[3], K. Nishio[1] and I. Yamashita[1,2,3], *[1]Matsushita Electric Industrial Co., Ltd, [2]NAIST and [3]Core Research for Evolutional Sci. and Tech. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

12:00 E-8-5
Realization of 340nm-band high-power (>7mW) InAlGaN quantum well UV-LED with p-type InAlGaN
S. Fujikawa[1], T. Takano[1,2], Y. Kondo[1,2] and H. Hirayama[1], *[1]RIKEN and [2]Matsushita Electric Works, Ltd. (Japan)*

Room 202B (F)

Room 303 (G)

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

11:45 H-8-5
Mobility Improvement of Pentacene Thin Film Transistors by Introduction of H_2 during Evaporation
T. Yokoyama, C. B. Park, Y. Kikuchi, T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

12:00 H-8-6
Evidence of Electron Trapping Center at Pentacene/SiO_2 Interface
C. B. Park, T. Yokoyama, T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

11:45 I-8-5
Improved Photoconduction Effects of Nanometer-Sized Si Dot Multilayers
Y. Hirano[1], S. Yamazaki[2] and N. Koshida[2], *[1]NHK Sci. and Technical Research Labs. and [2]Tokyo Univ. of Agriculture and Tech. (Japan)*

Room 406 (J)

Area 4: Advanced Memory Technology

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Lunch				
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
A-9 : FUSI (13:15-14:55) Chairs: T. Tatsumi (NEC Corp.) T. Nabatame (ASET)	B-9 : Post Planar CMOS (13:15-14:55) Chairs: A. Hokazono (Toshiba Corp.) H. Sayama (Renesas Technology Corp.)	C-9 : Low-k and Airgap (13:15-15:05) Chairs: J. Koike (Tohoku Univ.) J. Gambino (IBM)	D-9 : Spectroscopy for Bio Sensing (13:15-14:45) Chairs: K. Ajito (NTT) M. Niwano (Tohoku Univ.)	E-9 : LEDs (13:15-15:00) Chairs: Y. Lee (Hitachi Ltd.) M. Ezaki (Toshiba Corp.)
13:15 A-9-1 Practical Solutions to Enhance EWF Tunability of Ni FUSI Gates on HfO_2 X. P. Wang[1,2,3], J. J. Yang[1], H. Y. Yu[3], M. F. Li[1,2,4], J. D. Chen[1], R. L. Xie[1], C. X. Zhu[1], A. Y. Du[2], P. C. Lim[5], A. Lim[1,2], Y. Y. Mi[5], D. M. Y. Lai[5], W. Y. Loh[2], S. Biesemans[3], G. Q. Lo[2] and D. L. Kwong[2], *[1]National Univ. of Singapore, [2]Inst. of Microelectronic, [3]IMEC, [4]Fudan Univ. and [5]Inst. of Materials Research and Engineering (Singapore)*	**13:15 B-9-1** Wide-Range V_{th} Controllable SOTB (Silicon on Thin BOX) Integrated with Bulk CMOS Featuring Fully Silicided NiSi Gate Electrode T. Ishigaki[1], R. Tsuchiya[1], Y. Morita[1], N. Sugii[1], S. Kimura[1], T. Iwamatsu[2], T. Ipposhi[2], Y. Inoue[2] and T. Hiramoto[3], *[1]Hitachi, Ltd., [2]Renesas Tech. Corp. and [3]Univ. of Tokyo (Japan)*	**13:15 C-9-1 (Invited)** Low-k/Cu Integration Consistent from 90 nm thru 32 nm T. Nogami, *IBM (USA)*	**13:15 D-9-1 (Invited)** THz and microwave biochip C. K. Sun, *National Taiwan Univ. (Taiwan)*	**13:15 E-9-1** High-Brightness Ultraviolet LEDs on Si Using Quaternary InAlGaN Multi-Quantum-Wells with High Indium Contents Y. Fukushima, Y. Takase, M. Usuda, K. Orita, T. Ueda and T. Tanaka, *Matsushita Electric Industrial Co., Ltd. (Japan)*
13:35 A-9-2 Effectiveness of Aluminum Incorporation in Nickel Silicide and Nickel Germanide Metal Gates for Work Function Reduction A. E. J. Lim[1], R. T. P. Lee[1], A. T. Y. Koh[1], G. S. Samudra[1], D. L. Kwong[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*	**13:35 B-9-2** Additivity between sSOI- and CESL-induced nMOSFETs Performance Boosts F. Andrieu[1], F. Allain[1], C. Buj-Dufournet[1], O. Faynot[1], F. Rochette[1], M. Cassé[1], V. Delaye[1], F. Aussenac[1], L. Tosti[1], P. Maury[1], L. Vandroux[1], N. Daval[2], I. Cayrefourcq[2] and S. Deleonibus[1], *[1]CEA-LETI MINATEC and [2]SOITEC (France)*	**13:45 C-9-2** Influences of Skeletal Structure and Porosity on Dielectric and Mechanical Properties of Porous Organosilica Low-k Films S. Takada , N. Hata, Y. Seino and T. Yoshino, *AIST (Japan)*	**13:45 D-9-2** *In-Situ* Detection and Classification of DNA by Porous Alumina Filter in Conjugation with Infrared Absorption Spectroscopy R. Yamaguchi, A. Hirano, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*	**13:30 E-9-2** Effect of Multiquantum Barriers on Carrier Transport Mechanism of InGaN/GaN Multiple Quantum Well Light-emitting Diodes W. T. Su[1], Y. F. Chen[1], H. Y. Chen[1], J. C. Wang[1], H. T. Shen[1], T. E. Nee[1] and Y. F. Wu[2], *[1]Chang Gung Univ. and [2]Tech. and Sci. Inst. of Northern Taiwan (Taiwan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Lunch				
Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
F-9 : Characterization (13:15-14:55) Chairs: S. Miyazaki (Hiroshima Univ.) H. Hwang (Gwangju Inst. of Science & Engineering)	G-9 : Imaging Technology (13:15-14:35) Chairs: H. Yamauchi (Samsung Electronics Co., Ltd.) T. Matsuoka (Osaka Univ.)	H-9 : Organic Transistor Ⅲ (13:15-14:45) Chairs: T. Kamata (AIST) T. Someya (Univ. of Tokyo)	I-9 : Quantum Dots and Qubits (13:15-15:00) Chairs: T. Usuki (Univ. of Tokyo) K. Ono (RIKEN)	J-9 : Carbon Nanotube Devices and Growth Ⅰ (13:15-15:00) Chairs: Y. Ochiai (JST) Y. Ohno (Nagoya Univ.)
13:15 F-9-1 Advanced Characterization of High-k Gate Stack by Internal Photo Emission (IPE): Interfacial Dipole and Band Diagram in Al/Hf(Si)O_2/Si MOS Structure J. Widiez, K. Kita, T. Nishimura and A. Toriumi, *Univ. of Tokyo (Japan)*	**13:15 G-9-1** Real-Time Variable-Resolution and Dynamic Range Boosting CMOS Image Sensor J. J. Wang, C. J. Lin and Y. C. King, *National Tsing Hua Univ. (Taiwan)*	**13:15 H-9-1 (Invited)** Vertical Type Organic Transistors for Flexible Opto-electric Devices K. Kudo, *Chiba Univ. (Japan)*	**13:15 I-9-1 (Invited)** Scanning Probe Measurements on Semiconductor Nanostructures T. Ihn, A. Gildemeister, A. Pioda, S. Kicin and K. Ensslin, *ETH Zurich (Switzerland)*	**13:15 J-9-1 (Invited)** Digital Circuits with Carbon Nanotube Transistors A. Raychowdhury[1,2], J. Kurtin[1], K. Roy[2], V. De[1] and A. Keshavarzi[1], *[1]Intel Corp. and [2]Purdue Univ. (USA)*
13:35 F-9-2 Characterization of the $Sc_2O_3La_2O_3$ High-κ Gate Stack by STM Y. C. Ong[1], D. S. Ang[1], S. J. O' Shea[2], K. L. Pey[1], T. Kawanago[3], K. Kakushima[3] and H. Iwai[3], *[1]Nanyang Technological Univ., [2]Inst. of Material Research and Engineering and [3]Tokyo Tech. (Singapore)*	**13:35 G-9-2** High Sensitivity Dynamic Range Enhanced CMOS Imager with Noise Suppression S. Adachi[1], W. Lee[2], N. Akahane[2], H. Oshikubo[1], K. Mizobuchi[1] and S. Sugawa[2], *[1]Texas Instruments Japan and [2]Tohoku Univ. (Japan)*	**13:45 H-9-2** Highly Reliable Bottom-Contact Pentacene TFTs with a Poly(*p*-chloroxylylene) Layer Selectively Grown on a Gate-Insulator R. Yasuda[1], N. Hirai[1], I. Yagi[1], K. Nomoto[1], J. Kasahara[1], T. Minari[2], K. Tsukagoshi[2] and Y. Aoyagi[2], *[1]Sony Corp. and [2]RIKEN (Japan)*	**13:45 I-9-2** Spin-conserved Single-electron Transport between Zeeman Sublevels in a Few-electron Quantum Dot T. Fujisawa[1,2], G. Shinkai[1,2] and T. Hayashi[1], *[1]NTT Corp. and [2]Tokyo Tech (Japan)*	**13:45 J-9-2 (Invited)** Advances in Carbon Nanotube Devices and Circuits Y. M. Lin, Z. Chen, J. Appenzeller, P. M. Solomon and P. Avouris, *IBM (USA)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 7: Photonic Devices and Device Physics**
13:55 A-9-3 Impacts of Fluorine and Nitrogen Incorporation on NiSi Induced Junction Leakage on Si(110) Substrate M. Tsuchiaki and A. Nishiyama, *Toshiba Corp. (Japan)*	**13:55 B-9-3** Novel Extended-Pi Shaped Silicon-Germanium (eII-SiGe) Source/Drain Stressors for Strain and Performance Enhancement in P-Channel FinFETs K. M. Tan[1], T. Y. Liow[1,2], R. T. P. Lee[1], M. Zhu[1], K. M. Hoe[2], C. H. Tung[2], N. Balasubramanian[2], G. S. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*	**14:05 C-9-3** Properties of Methyl Boron Nitride Film for Next Generation Low-K Interconnection S. Tokuyama, M. K. Mazumder, D. Watanabe, C. Kimura, H. Aoki and T. Sugino, *Osaka Univ. (Japan)*	**14:00 D-9-3** CMOS Optical Polarization Analyzer Chip for μTAS T. Tokuda, S. Sato, M. Nunoshita and J. Ohta, *NAIST (Japan)*	**13:45 E-9-3** MOCVD Growth of GaN-Based LEDs with Naturally Formed Nano-pyramids C. E. Lee, C. H. Chiu, M. H. Lo, H. W. Huang, T. C. Lu, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ. (Taiwan)*
14:15 A-9-4 Phase and Composition Control of Ni-FUSI gates by N_2 I/I with Double Ni-silicidation K. Yamamoto[1], S. Sakashita[2], Y. Sato[1], M. Inoue[2], M. Anma[2], T. Oosuka[1] and J. Yugami[2], *[1]Matsushita Electric Industrial Co., Ltd. and [2]Renesas Tech. Corp. (Japan)*	**14:15 B-9-4** Impact of Gradual Source/Drain Impurity Profiles on Performance of Germanium Channel Double-Gated pMISFETs T. Yamamoto[1], M. Harada[1], N. Taoka[2], Y. Yamashita[1], N. Sugiyama[1] and S. Takagi[2,3], *[1]MIRAI-ASET, [2]MIRAI-AIST and [3]Univ. of Tokyo (Japan)*	**14:25 C-9-4** Effects of Silylation on Electrical and Mechanical Characteristics of Mesoporous Pure Silica Zeolite Films T. Seo[1], T. Yoshino[2], N. Ohnuki[2], Y. Seino[2], N. Hata[2] and T. Kikkawa[1,2], *[1]Hiroshima Univ. and [2]AIST (Japan)*	**14:15 D-9-4** Label-Free Immunosensing for α-Fetoprotein in Human Plasma using Surface Plasmon Resonance K. Kawano[1], Y. Teramura[2], M. Oda[3], T. Suzuki[2], H. Kotera[2] and H. Iwata[2], *[1]CREATE-JST, [2]Kyoto Univ. and [3]TERAMECS CO., LTD (Japan)*	**14:00 E-9-4** A Novel Sn-based Metal Substrate Technology for the Fabrication of Vertical-Structure GaN-Based High Power Light-Emitting Diodes H. Y. Kuo[1], S. J. Wang[1], K. M. Uang[2], S. L. Chen[1], T. M. Chen[1,2], P. R. Wang[1], C. C. Tsai[1] and H. Kuan[3], *[1]National Cheng Kung Univ., [2]WuFeng Inst. of Tech. and [3]Far East Univ. (Taiwan)*

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
13:55 F-9-3 Origin of Structural Phase Transformation of SiO_2-doped HfO_2 K. Tomida, K. Kita and A. Toriumi, *Univ. of Tokyo (Japan)*	**13:55 G-9-3** A Moving-Object-Localization Hardware Algorithm Employing OR-Amplification of Pixel Activities Y. Niki, Y. Manzawa, S. Kametani and T. Shibata, *Univ. of Tokyo (Japan)*	**14:00 H-9-3** Fabrication of Soluble Semiconductor Thin Film Transistor with Printed Electrodes using h-PDMS Stamp J. Jo[1], T. M. Lee[1], D. S. Kim[1], K. Y. Kim[1], E. S. Lee[1], K. Y. Park[2] and M. Esashi[3], *[1]KIMM, [2]ITEP and [3]Tohoku Univ. (Korea)*	**14:00 I-9-3** Fano-Kondo effect in three quantum dots aiming at charge qubit measurement T. Tanamoto, Y. Nishi and S. Fujita, *Toshiba Corp. (Japan)*	**14:15 J-9-3** A Triple Quantum Dot in a Single Wall Carbon Nanotube K. Grove-Rasmussen[1,2], H. I. Jørgensen[2], T. Hayashi[1], P. E. Lindelof[2] and T. Fujisawa[1], *[1]NTT Corp. and [2]Univ. of Copenhagen (Japan)*
14:15 F-9-4 Characteristics of Pure Ge_3N_4 Dielectric Layers Formed by High-Density Plasma Nitridation K. Kutsuki, G. Okamoto, T. Hosoi, T. Shimura, K. Yasutake and H. Watanabe, *Osaka Univ. (Japan)*	**14:15 G-9-4** New Reconfigurable Memory Architecture for Parallel Image Processing LSI with Three-Dimensional Structure S. Kodama, D. Amano, T. Sugimura, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. (Japan)*	**14:15 H-9-4** Double-Shot Inkjet Printing of Organic Charge-Transfer Compounds M. Hiraoka[1], T. Hasegawa[1], T. Yamada[1], Y. Takahashi[1], S. Horiuchi[1] and Y. Tokura[1,2], *[1]AIST and [2]Univ. of Tokyo (Japan)*	**14:15 I-9-4** Study of Single-Charge Polarization on two Charge Qubits Integrated onto a Double Single-Electron Transistor Readout Y. Kawata[1,3], S. Nishimoto[1], Y. Tsuchiya[1,3], S. Oda[1,3] and H. Mizuta[1,2,3], *[1]Tokyo Tech., [2]Univ. of Southampton and [3]SORST-JST (Japan)*	**14:30 J-9-4** Electric Property Control of Carbon Nanotubes by Defects S. Suzuki[1], J. Hashimoto[1,2], T. Ogino[2] and Y. Kobayashi[1], *[1]NTT Corp. and [2]Yokohama National Univ. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

14:35 A-9-5
CMP-less Co-Integration of Tunable Ni-TOSI CMOS for Low Power Digital and Analog Applications
G. Bidal[1,5], M. Müller[1], S. Denorme[2], D. Aimé[3], M. Rafik[2], A. Cathignol[2], G. Ribes[2], S. Pokrant[1], P. Gouraud[2], T. Kormann[1], G. Chabanne[3], C. Blanc[3], S. Bonnetier[3], D. Barge[1], C. Laviron[4], A. Tarnowka[1], G. Ghibaubo[5], F. Boeuf[2] and T. Skotnicki[2], *[1]NXP Semiconductors, [2]STMicroelectronics, [3]Freescale, [4]CEA-LETI and [5]IMEP (France)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

14:35 B-9-5
A Double-Gate Tunneling Field-Effect Transistor with Silicon-Germanium Source for High-Performance, Low Standby Power, and Low Power Technology Applications
E. H. Toh, G. H. Wang, L. Chan, D. Sylvester, C. H. Heng, G. Samudra and Y. C. Yeo, *National Univ. of Singapore (Singapore)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

14:45 C-9-5
Determination of mechanical properties of porous silica low-k films on Si substrates using orientation dependence of surface acoustic wave
T. Takimura, N. Hata, S. Takada and T. Yoshino, *AIST (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

14:30 D-9-5
In-Situ Surface Infrared Study of DNA Attachment and Hybridization at Si Surfaces
A. Hirano, K. Tanaka, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

14:15 E-9-5
The Aluminum Packaging for LED using Selectively Anodizing Method
K. M. Kim[1], S. H. Shin[2], Y. K. Lee[2], S. M. Choi[2] and Y. S. Kwon[1], *[1]KAIST and [2]Samsung Electro-Mechanics (Korea)*

14:30 E-9-6
The Fabrication of the Circular Ring Laser Resonators by Excimer Laser Assisted Etching at Cryogenic Temperature
M. C. Shih and S. C. Wang, N*ational Univ. of Kaohsiung (Taiwan)*

14:45 E-9-7
Red emission from ZnO-based double heterojunction diode
T. Ohashi, K. Yamamoto, A. Nakamura and J. Temmyo, *Shizuoka Univ. (Japan)*

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

14:35 F-9-5
Surface Treatment of Ge(001) Surface by Radical Nitridation
H. Kondo, M. Fujita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

Room 304 (H)

Area 10: Organic Materials Science, Device Physics, and Applications

14:30 H-9-5
Fabrication of Flexible OTFT-backplanes for Active Matrix Electrophoretic Display
M. W. Lee and C. K. Song, *Dong-A Univ. (Korea)*

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

14:30 I-9-5
Formation and control of 2-qubits exciton state in a coupled quantum dots
K. Goshima[1,2], K. Komori[1,2] and T. Sugaya[1,2], *[1]AIST and [2]CREST-JST (Japan)*

14:45 I-9-6
Decoherence of nuclear spins in a GaAs quantum well probed by a submicron scale all-electrical NMR device
T. Ota[1,2], N. Kumada[1], G. Yusa, [1,3,4], S. Miyashita[5], T. Fujisawa[1] and Y. Hirayama[1,2,4], *[1]NTT Corp., [2]SORST-JST, [3]PRESTO-JST, [4]Tohoku Univ. and [5]NTT-AT (Japan)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

14:45 J-9-5
Single charge sensitivity of single-walled carbon nanotube single-hole transistor
T. Kamimura[1,2], Y. Ohno[1,2] and K. Matsumoto[1,2,3], *[1]Osaka Univ., [2]CREST-JST and [3]AIST (Japan)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
	Area 3: CMOS Devices/Device Physics	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	
	B-10 : Noise and RF (15:15-17:05) Chairs: D. Hisamoto (Hitachi Ltd.) K. Takeuchi (NEC Corp.)	C-10 : Nanoscale Characterization (15:25-16:25) Chairs: N. Hata (NEDO) S. Ogawa (Selete)	D-10 : μ-TAS and Medical Applications (15:15-16:45) Chairs: K. Sawada (Toyohashi Univ. of Technology) H. Tabata (The Univ. of Tokyo)	
	15:15 B-10-1 (Invited) RTN Effects in Scaled Flash Memory Arrays A. S. Spinelli, C. M. Compagnoni, R. Gusmeroli, M. Ghidotti and A. L. Lacaita, *Politecnico di Milano (Italy)*	**15:25 C-10-1** Characterization of Line-edge Roughness in Cu/low-k Interconnect Pattern A. Yamaguchi[1], D. Ryuzaki[1], K. Takeda[1], J. Yamamoto[1], H. Kawada[2] and T. Iizumi[2], *[1]Hitachi, Ltd. and [2]Hitachi High-Technologies Corp. (Japan)*	**15:15 D-10-1** One-Chip Integration of the Rapid Diagnosis Infectious Disease Chip Based on New Phenomena of DNA Trap and Denature in Nano-Gaps S. Hashioka[1,2], K. Masu[1] and Y. Horiike[2], *[1]Tokyo Tech. and [2]NIMS (Japan)*	
	15:45 B-10-2 Analysis of Random Telegraph Signal Noise in Dual and Single Oxide Device And Its Application to CMOS Image Sensor Readout Circuit H. Lee, Y. Yoon, J. Jeon and H. Shin, *Seoul National Univ. (Korea)*	**15:45 C-10-2** Nano-Scale Stress Field Evaluation with Shallow Trench Isolation Structure Assessed by Cathodoluminescence, Raman Spectroscopy, and Finite Element Method Analyses M. Kodera[1], T. Iguchi[1], N. Tsuchiya[1], M. Tamura[2], S. Kakinuma[3], N. Naka[3] and S. Kashiwagi[3], *[1]Toshiba Corp., [2]Toshiba I. S. Corp. and [3]Horiba, Ltd. (Japan)*	**15:30 D-10-2** Droplet device for immunoassay detection C. H. Chang, S. Hashioka, T. Chikyo and Y. Horiike, *NIMS (Japan)*	

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**		**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
F-10 : Advanced Process (15:15-16:35) Chairs: O. Faynot (CEA-LETI) T. Tatsumi (NEC Corp.)	G-10 : Connectivity (15:15-16:35) Chairs: M. Horiguchi (Renesas Technology Corp.) T. Komuro (Agilent Technologies International Japan, Ltd.)		I-10 : Novel Devices (15:15-16:45) Chairs: Y. Uraoka (Nara Inst. of Science and Technology) B. G. Park (Seoul National Univ.)	J-10 : Carbon Nanotube Devices and Growth Ⅱ (15:15-16:30) Chairs: S. Akita (Osaka Prefecture Univ.) Y. Homma (Tokyo Univ. of Science)
15:15 F-10-1 Dependence of Electrical Characteristics on Interfacial Structures of Epitaxial $NiSi_2$/Si Schottky Contacts Formed from Ni/Ti/Si System O. Nakatsuka, A. Suzuki, S. Akimoto, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ. (Japan)*	**15:15 G-10-1** PCA-based Object Detection/Recognition Chip for Wireless Interconnected 3-D Integration H. Ando, S. Kameda, D. Arizono, N. Fuchigami, K. Kaya, M. Sasaki and A. Iwata, *Hiroshima Univ. (Japan)*		**15:15 I-10-1** High Performance Germanium Quantum-dot Single-hole Transistors with Self-aligned Electrodes S. H. Hsu, W. T. Lai and P. W. Li, *National Central Univ. (Taiwan)*	**15:15 J-10-1** New Measurement Method of Carbon Nanotube Energy Band Gap M. Maeda[1,4], T. Kamimura[2,4], S. Iwasaki[2,4] and K. Matsumoto[2,3,4], *[1]Univ. of Tsukuba, [2]Osaka Univ., [3]AIST and [4]CREST-JST (Japan)*
15:35 F-10-2 A Breakthrough Electronic Lithography Process Through Si Layer for Self Aligning Gates in Planar Double-Gate Transistors for 32nm Node And Below R. Wacquez[1,2,4], P. Coronel[1], M. P. Samson[1,2], D. Delille[3], L. R. Clement[3], V. Delaye[2], L. Baud[2], N. Loubet[1], J. Bustos[1], A. Pouydebasque[3], B. Guillaumot[1,2], T. Ernst[2], P. Masson[4], J. P. Gouy[2] and T. Skotnicki[1], *[1]STMicroelectronics, [2]CEA-LETI, MINATEC, [3]NXP and [4]L2MP (France)*	**15:35 G-10-2** Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link A. Kumar, N. Miura and T. Kuroda, *Keio Univ. (Japan)*		**15:30 I-10-2** Single Electron-based Flexible Multi-valued Exclusive-OR Logic Gate S. J. Kim, C. K. Lee, R. S. Chung, M. S. Kim, E. S. Park, S. J. Shin and J. B. Choi, *Chungbuk National Univ. (Korea)*	**15:30 J-10-2** Self-aligned Fabrication Process for Pd-Contacted and PMMA-Passivated Carbon Nanotube Field-Effect Transistors L. Rispal, H. Yang, R. Heller, G. Hess, G. Tzschöckel and U. Schwalke, *Darmstadt Univ. of Tech. (Germany)*

Room 101 (A)

Room 102 (B)

Area 3: CMOS Devices/Device Physics

16:05 B-10-3
Simultaneous Extraction of Locations and Energies of Two Independent Traps in Gate Oxide From Four-level RTS noise
S. Yang, H. Lee and H. Shin, *Seoul National Univ. (Korea)*

16:25 B-10-4
Analog Performance of Asymmetric Schottky Tunneling Source nFET for RF and Mixed-Mode Application
R. Jhaveri and J. C. S. Woo, *Univ. of California (USA)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

16:05 C-10-3
Channel Strain in Advanced CMOSFETs Measured Using Nano-Beam Electron Diffraction
A. Toda[1], H. Nakamura[2], T. Fukai[2] and N. Ikarashi[1], *[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)*

Room 201B (D)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

15:45 D-10-3
High-Throughput Fluorometric Assay of Enzymatic Reactions on a Microreactor Array Chip
T. Ichiki[1,2], Y. Hosoi[1], J. Liu[1], T. Osawa[1], T. Akagi[1], M. Biyani[2] and N. Nemoto[2,3], *[1]Univ. of Tokyo, [2]CREATE-JST and [3]Janusys Corp. (Japan)*

16:00 D-10-4
Development of a multi-chip retinal stimulator for in vivo experiments toward retinal prosthesis
T. Tokuda[1], R. Asano[1], Y. Terasawa[2], M. Nunoshita[1], K. Nakauchi[3], T. Fujikado[3], Y. Tano[3] and J. Ohta[1], *[1]NAIST, [2]NIDEK Co., Ltd. and [3]Osaka Univ. (Japan)*

Room 202A (E)

Room 202B (F)

Area 1: Advanced Gate Stack/Si Processing Science

15:55 F-10-3
Contact Technology employing Nickel-Platinum Germanosilicide Alloys for P-Channel FinFETs with Silicon-Germanium Source and Drain Stressors
R. T. P. Lee[1], K. M. Tan[1], A. E. J. Lim[1], T. Y. Liow[1], X. C. Chen[1], M. Zhu[1], A. T. Y. Koh[1], K. M. Hoe[3], S. Y. Chow[2], G. Q. Lo[3], G. S. Samudra[1], D. Z. Chi[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Inst. of Materials Research and Engineering and [3]Inst. of Microelectronics (Singapore)*

16:15 F-10-4
An Optimized Silicidation Technique for Source and Drain of FINFET
K. Okuyama, A. Sugimura and H. Sunami, *Hiroshima Univ. (Japan)*

Room 303 (G)

Area 5: Advanced Circuits and Systems

15:55 G-10-3
Scaling Characteristics of Si On-chip Integrated Antennas
K. Kimoto, N. Sasaki and T. Kikkawa, *Hiroshima Univ. (Japan)*

16:15 G-10-4
A Fully Integrated SiGe Optical Receiver Using Differential Active Miller Capacitor for 4.25 Gb/s Fiber Channel Application
J. C. Huang, K. S. Lai and K. Y. J. Hsu, *National Tsing Hua Univ. (Taiwan)*

Room 304 (H)

Room 405 (I)

Area 9: Physics and Applications of Novel Functional Materials and Devices

15:45 I-10-3
Self-Aligned Dual-Gate Single-Electron Transistors (DG-SETs)
S. Kang[1], D. H. Kim[2], I. H. Park[1], J. H. Kim[1], J. E. Lee[1], J. D. Lee[1] and B. G. Park[1], *[1]Seoul National Univ. and [2]Kookmin Univ. (Korea)*

16:00 I-10-4
Design Control of Random Dopant-induced Multiple-Tunnel-Junction Arrays for Turnstile Operation
D. Moraru, K. Yokoi, H. Ikeda and M. Tabe, *Shizuoka Univ. (Japan)*

Room 406 (J)

Area 13: Applications of Nanotubes and Nanowires

15:45 J-10-3
Individual Carbon Nanotubes as Nano-incandescent
S. Akita[1,3] and Y. Nakayama[2,3], *[1]Osaka Prefecture Univ., [2]Osaka Univ. and [3]CREST-JST (Japan)*

16:00 J-10-4
A Field-Emission Device with Novel Self-Focus Gate Structure
H. W. Chen, K. C. Lin, C. P. Juan, Y. S. Leou, Y. Y. Hsu and H. C. Cheng, *National Chiao Tung Univ. (Taiwan)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
	Area 3: CMOS Devices/Device Physics	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	
	16:45 B-10-5 Frequency Dependence of Measured MOSFET Distortion Characteristic T. Minami[1], Y. Takeda[1], M. Miyake[1], M. Miura-Mattausch[1], H. J. Mattaush[1], T. Ohguro[2], T. Iizuka[2], M. Taguchi[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]STARC (Japan)*		**16:15 D-10-5** UWB Imaging for Early Breast Cancer Detection by Confocal Algorithm X. Xiao[1,2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Tianjin Univ. (Japan)*	
			16:30 D-10-6 Development of a CMOS-based Neural Imaging and Interface Device D. C. Ng, T. Mizuno, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, *NAIST (Japan)*	

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Area 1: Advanced Gate Stack/Si Processing Science	**Area 5: Advanced Circuits and Systems**		**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 13: Applications of Nanotubes and Nanowires**
			16:15 I-10-5 Acoustic Wave Manipulation by Phased Operation of Two-Dimensionally Arrayed Nanocrystalline Silicon Ultrasonic Emitters B. Gelloz, M. Sugawara and N. Koshida, *Tokyo Univ. of Agri. and Tech. (Japan)*	**16:15 J-10-5** Combinatorial Control of Catalyst Nanoparticles for Customized Production of Single- and Multi-Walled Carbon Nanotubes S. Noda, K. Hasegawa, H. Sugime, K. Kakehi, S. Maruyama and Y. Yamaguchi, *Univ. of Tokyo (Japan)*
			16:30 I-10-6 New Type Oxygen Sensor Using Micro-fabricated Layered Semiconductor Compound T. Nugroho, A. Ikeda, Y. Kakihara, H. Kuriyaki and Y. Kuroki, *Kyushu Univ. (Japan)*	