Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-3: Reliability-I
(9:00-10:30)
Chairs: J. Yugami (Renesas Tech. Corp.)
Y. Tsunashima (Toshiba Corp.)

9:00 A-3-1(Invited)
A Study of NBTI and PBTI (Charge Trapping) in High k Stacks with NiSi, TiN, Re Gates
S. Zafar, Y. H. Kim, V. Paruchuri, V. Narayanan, B. Doris, A. Callegari, J. Stathis and T. Ning, *IBM (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-3: CMOS Integration
(9:00-10:30)
Chairs: K. Shibahara (Hiroshima Univ.)
H. Wakabayashi (Sony Corp.)

9:00 B-3-1(Invited)
Low Standby Power CMOS Process Integration Scheme for 45-32 nm node
K. Imai, *NEC Electronics Corp. (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-3: Plasma Induced Damage of Low-k Materials
(9:00-10:30)
Chairs: S. Ogawa (Selete)
T. Tatsumi (Sony Corp.)

9:00 C-3-1(Invited)
Generation Mechanism of Etching Damages on Low-k SiOCH Films and Development of Novel Damage Evaluation Technique
M. Hori, *Nagoya Univ. (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

D-3: RF Components
(9:00-10:20)
Chairs: R. Fujimoto (Toshiba Corp.)
T. Hamasaki (Texas Instruments Japan Ltd.)

9:00 D-3-1
A 0.49-6.50 GHz Wideband LC-VCO with High-IRR in a 180 nm CMOS Technology
Y. Kobayashi, K. Ohashi, Y. Ito, H. Ito, K. Okada and K. Masu, *Tokyo Tech. (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-3: Special Session: Photonic Crystals and Si Photonics II
(9:00-10:30)
Chairs: O. Wada (Kobe Univ.)
R. Akimoto (AIST)

9:00 E-3-1(Invited)
LSI on-chip optical interconnection with Si nano-photonics
J. Fujikata[1], K. Nishi[1], A. Gomyo[1], J. Ushida[1], T. Ishi[1], H. Yukawa[1], D. Okamoto[1], M. Nakada[1], T. Shimizu[1], M. Kinoshita[1], K. Nose[1], M. Mizuno[1], T. Tsuchizawa[2], T. Watanabe[2], K. Yamada[2], S. Itabashi[2] and K. Ohashi[1], *[1]MIRAI-Selete and [2]NTT Microsystem Integration Labs. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-3: Group-IV Semiconductors I
(9:00-10:15)
Chairs: K. Hiruma (Hokkaido Univ.)
K. Nishi (NEC Corp.)

9:00 F-3-1
Fabrication of 3-D Silicon Micro Probes for Neural Recording Using Multi-Step VLS Growth
A. Ikedo[1], N. Funagayama[1], T. Kawashima[1], H. Takao[1,2], K. Sawada[1,2] and M. Ishida[1,2], *[1]Toyohashi Univ. of Tech. and [2]CREST-JST (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-3: High-Speed Devices and ICs I
(9:00-10:15)
Chairs: S. Yamahata (NTT)
Y. J. Chan (National Central Univ. Taiwan)

9:00 G-3-1(Invited)
Class-F Microwave Amplifier Design Using GaAs-HBT and GaN-HEMT
K. Honjo, R. Ishikawa, T. Yoshida and C. Zheng, *Univ. of Electro-Communications (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-3: Nanowire & Nanotube Sensors
(9:00-10:30)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Cui (Stanford Univ.)

9:00 H-3-1(Invited)
Nanowires for Nanoscale Electronics, Biosensors and Energy Applications
S. Meister, C. K. Chan, H. Peng and Y. Cui, *Stanford Univ. (USA)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-3: Flash Memory II
(9:00-10:20)
Chairs: Y. Shimamoto (Hitachi, Ltd.)
C. Hsu (eMemory Tech. Inc.)

9:00 J-3-1
2-bit/cell Characteristics of High-Density and High-Performance SONOS Flash Memory Cell with Recessed Channel Structure
K. R. Han, Y. M. Kim, K. H. Park, S. G. Jung, B. K. Choi and J. H. Lee, *Kyungpook National Univ. (Korea)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

9:30 A-3-2
Comprehensive Understanding of PBTI and NBTI reliability of High-k / Metal Gate Stacks with EOT Scaling to sub-1nm
M. Sato[1], K. Yamabe[2], K. Shiraishi[2], S. Miyazaki[3], K. Yamada[4], C. Tamura[2], R. Hasunuma[2], S. Inumiya[1], T. Aoyama[1], Y. Nara[1] and Y. Ohji[1], *[1]Selete, [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Waseda Univ. (Japan)*

9:50 A-3-3
Performance and Reliability Improvement by Optimized Nitrogen Content of TaSiNx Metal Gate in Metal/ HfSiON nFETs
T. Onizawa, M. Sato, T. Aoyama, T. Eimori, Y. Nara and Y. Ohji, *Selete (Japan)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

9:30 B-3-2
High Performance and Low Leakage CMOS for 45nm Low Power Technology and Beyond
J. P. Han[1], Y. M. Lee[2], H. Utomo[3], R. Lindsay[1], M. Eller[1], J. C. Kim[4], V. Sardesai[3], V. Chan[3], S. Fang[3], J. Holt[3], T. N. Adam[3], H. Zhuang[1], W. Wille[3], Z. Lun[2], H. Wang[3], T. Dyer[3], J. Yan[1], O. J. Kwon[3], O. S. Kwon[1], C. W. Lai[2], T. J. Tang[2], S. S. Tan[2], J. Yuan[3], J. Li[3], H. Ng[3], H. Shang[3], J. Sudijono[2], D. Schepis[3], M. Ieong[3], Y. Li[3], J. H. Ku[4], A. Gutmann[1] and M. Hierlemann[1], *[1]Infineon Technologies AG, [2]Chartered Semiconductor Manufacturing Ltd., [3]IBM and [4]Samsung Electronics Co., Ltd. (USA)*

9:50 B-3-3
In-Depth Study of Two-Dimensional Layout Dependences in Multiple-Stressor CMOS for 45 nm Technology Node High-Performance Applications
T. Miyashita[1], J. Ogura[2], T. Owada[2], T. Sakuma[1], H. Nomura[2], H. Miyaoka[2], A. Hasegawa[2], S. Yamaguchi[2] and S. Satoh[1], *[1]Fujitsu Labs. Ltd. and [2]Fujitsu Ltd. (Japan)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

9:30 C-3-2
Impact of Barrier Metal Sputtering on Low-k SiOCH Films with Various Chemical Structures
N. Inoue, N. Furutake, F. Ito, H. Yamamoto, T. Takeuchi and Y. Hayashi, *NEC Corp. (Japan)*

9:50 C-3-3
Process Induced Damage Analysis of Low-k SiOCH Films Focusing on Siloxane Network and Methyl End Group
S. Nakao, K. Kinoshita and S. Ogawa, *Selete (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

9:20 D-3-2
Evaluation of Digital Crosstalk Noise on a Differential Input VCO
A. Toya[1], Y. Murasaka[2], T. Ohmoto[2] and A. Iwata[1,2], *[1]Hiroshima Univ. and [2]A-R-Tec Corp. (Japan)*

9:50 D-3-3
A New Symmetric Inductor Model for RF Circuits under Single-end and Differential Operations
J. C. Guo and T. Y. Tan, *National Chiao Tung Univ. (Taiwan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

9:30 E-3-2
A Study on the Design and Properties of an SiON/SiO_2 Waveguide: The Effect of the Substrate on Propagation Loss
J. Ushida[1], A. Gomyo[1], J. Fujikata[1], D. Okamoto[1], K. Nishi[1], K. Ohashi[1], T. Watanabe[2], T. Tsuchizawa[2], K. Yamada[2] and S. Itabashi[2], *[1]MIRAI-Selete and [2]NTT Microsystem Integration Labs. (Japan)*

9:45 E-3-3
Proposal of a Silicon Optical Modulator Based on Inversion-Carrier Absorption
T. Hirata, K. Kajikawa, T. Tabei and H. Sunami, *Hiroshima Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:15 F-3-2
Demonstration of holes in strained Ge quantum wells with much higher drift mobility and density than that of electrons in strained Si channels
M. Myronov[1], K. Sawano[1], K. M. Itoh[2] and Y. Shiraki[1], *[1]Musashi Inst. of Tech. and [2]Keio Univ. (Japan)*

9:30 F-3-3
Pulsed Laser Irradiation of Silicon-Germanium-on-Insulator ($Si_{0.17}Ge_{0.83}OI$) Substrates for Strain Relaxation and Defect Reduction
G. H. Wang[1], E. H. Toh[1], X. Wang[2], K. M. Hoe[3], S. Tripathy[1], G. Q. Lo[3], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Singapore Inst. of Manufacturing Tech. and [3]Inst. of Microelectronics (Singapore)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

9:30 G-3-2
High-Performance InGaAs/InP Composite-Channel High Electron Mobility Transistors Grown by Metal Organic Vapor-Phase Epitaxy
H. Sugiyama[1], T. Kosugi[1], H. Yokoyama[1], K. Murata[1], Y. Yamane[2], M. Tokumitsu[1] and T. Enoki[1], *[1]NTT Corp. and [2]NTT Electronics Corp. (Japan)*

9:45 G-3-3
Low Power Consumption and Low Noise InGaP/GaAs HBT MMIC Amplifier for Full-Band UWB Receiver
R. Ishikawa[1], T. Abe[1], M. Shimada[2] and K. Honjo[1], *[1]Univ. of Electro-Communications and [2]NANOTECO Corp. (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

9:30 H-3-2
Electrical Sensing of Calcium Ions using Silicon Nanowire Array
A. Agarwal[1], W. L. Wong[1,2], K. L. Yang[2], S. Balakumar[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore (Singapore)*

9:45 H-3-3
Fabrication of vertically-aligned CNT electrodes using plasma-enhanced CVD for chemical sensors
Y. Kojima, S. Kishimoto, M. Okochi, H. Honda and T. Mizutani, *Nagoya Univ. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

9:20 J-3-2
ESR and PL Study of Charge Trapping Centers in Silicon Nitride Films and Its Verification with Novel ONO-Sidewall 2-bit/cell Nonvolatile Memory
A. Toki[1], N. Shinohara[1], M. Nakano[2], H. Kotaki[2] and Y. Kamigaki[1], *[1]Kagawa Univ. and [2]Sharp Corp. (Japan)*

9:40 J-3-3
ONO Thickness Dependency of Complementary Bit Disturb in SONOS-type Nonvolatile Memory
K. Kikuchi, *Spansion Japan Ltd. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

10:10 A-3-4
nMOSFET Reliability Improvement attributed to the Interfacial Dipole formed by La Incorporation in HfO_2
C. Y. Kang[1], P. kirsch[2], D. Heh[1], C. Young[1], P. Sivasubramani[1], G. Bersuker[1,] S. C. Song[1], R. Choi[1], B. H. Lee[2], J. Lichtenwalner[3], J. S. Jur[3], A. I. Kingon[3] and R. Jammy[2], *[1]SEMATECH, [2]IBM Assignee and [3]North Carolina State Univ. (USA)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

10:10 B-3-4
Is a "Power Optimized" Roadmap Realistic for High Performance Applications?
F. Boeuf and T. Skotnicki, *STMicroelectronics (France)*

Room 201A (C)

Area 2: Characterization and Materials Engineering for Interconnect Integration

10:10 C-3-4
Plasma Cure Process for Porous SiOCH Films using CF_4 Gas
K. Tomioka, J. Nakahira, S. Kondo, S. Ogawa and S. Saito, *Selete (Japan)*

Room 201B (D)

Area 5: Advanced Circuits and Systems

10:10 D-3-4
Thick Au High-Q Inductor and Its Chip-on-Chip Bonding on an RF IC for Various Frequencies
J. Kodate[1], K. Kuwabara[1], N. Sato[1], H. Morimura[1], K. Kudou[2], K. Machida[2] and H. Ishii[1], *[1]NTT Corp. and [2]NTT AT (Japan)*

Room 202A (E)

Area 7: Photonic Devices and Device Physics

10:00 E-3-4
Photoelastic Effect in Silicon Ring Resonator
Y. Amemiya, Y. Tanushi, T. Tokunaga and S. Yokoyama, *Hiroshima Univ. (Japan)*

10:15 E-3-5
Magneto-optic Effect in Amorphous $Bi_3Fe_5O_{12}$ Waveguide Sputtered at Room Temperature
H. Taura, Y. Shishido, Y. Tanushi, T. Tokunaga and S. Yokoyama, *Hiroshima Univ. (Japan)*

Break

Short Presentation P-1 (10:45-12:15)
Chair: H. Fukutome (Fujitsu Labs. Ltd.)

Short Presentation P-3 (10:45-12:15)
Chair: S. Hayashi (Matsushita Electric Industrial Co., Ltd.)

Short Presentation P-2 and P-12 (10:45-12:15)
Chair: S. Ogawa (Selete)

Short Presentation P-5 and P-11 (10:45-12:15)
Chairs: R. Fujimoto (Toshiba Corp.) H. Tabata (Univ. of Tokyo)

Short Presentation P-7 (10:45-12:15)
Chair: M. Sugawara (Fujitsu Labs. Ltd.)

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

9:45 F-3-4
Strain-Relaxed $Si_{1-x}Ge_x$ and Strained Si Grown by Sputter Epitaxy
H. Hanafusa[1], Y. Suda[1], A. Kasamatsu[2], N. Hirose[2], T. Mimura[2] and T. Matsui[2], *[1]Tokyo Univ. of Agri. and Tech. and [2]NICT. (Japan)*

10:00 F-3-5
A Novel Approach to Fabricate ～ 120 nm Thick Fully Relaxed Ge-on-Insulator
S. Balakumar[1], K. M. Hoe[1], W. Tang[1], Y. L. Foo[2], S. Tripathy[2], C. H. Tung[1], G. Q. Lo[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]Inst. of Materials Research and Engineering (Singapore)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

10:00 G-3-4
Ku-band Compact Multi-layer Monolithic Microwave Digital Attenuator using InP/InGaAs PIN Diodes
H. Eom, J. G. Yang, S. Choi and K. Yang, *KAIST (Korea)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

10:00 H-3-4
Comparison of Top gate Structures for Carbon Nanotube Field Effect Transistor Biosensor
M. Abe[1,2], K. Murata[1,2,3], T. Ataka[1,2] and K. Matsumoto[2,3,4,5], *[1]Olympus Corp., [2]NEDO, [3]CREST-JST, [4]AIST and [5]Osaka Univ. (Japan)*

10:15 H-3-5
Development of gas sensors based on tungsten oxide nanowires in a metal/SiO_2/metal structure and their sensing responses to NO_2
R. M. Ko[1], Z. F. Wen[1], S. J. Wang[1], J. K. Lin[1], G. H. Fan[1], W. I. Shu[1] and B. W. Liou[2], *[1]National Cheng Kung Univ. and [2]WuFeng Inst. of Tech. (Taiwan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

10:00 J-3-4
Ramping Amplitude Multi-Frequency Charge Pumping Technique for Silicon-Oxide-Nirtride-Oxide-Silicon Flash EEPROM Cell Transistors
W. H. Choi[1], H. S. Joo[1], I. S. Han[1], S. S. Park[1], H. M. Kwon[1], T. G. Goo[1], O. S. Yoo[1], M. K. Na[1], J. C. Om[2], S. S. Lee[2], G. H. Bae[2], H. D. Lee[1] and G. W. Lee[1], *[1]Chungnam National Univ. and [2]Hynix Semiconductor Inc. (Korea)*

Break

Short Presentation P-8 (10:45-12:15)
Chair: H. Yamaguchi (NTT Corp.)

Short Presentation P-6 (10:45-12:15)
Chair: M. Kuzuhara (Univ. of Fukui)

Short Presentation P-10 and P-13 (10:45-12:15)
Chairs: T. Kamata (AIST) K. Matsumoto (Osaka Univ.)

Short Presentation P-9 (10:45-12:15)
Chair: Y. Takahashi (Hokkaido Univ.)

Short Presentation P-4 (10:45-12:15)
Chair: I. Asano (Elpida Memory, Inc.)

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-5: Junction
(15:15-16:25)
Chairs: B. Mizuno (Ultimate Junction Technologies Inc.)
H. Fukutome (Fujitsu Labs. Ltd.)

15:15 A-5-1(Invited)
Study of Dopant Diffusion and Defect Evolution for Advanced Ultra Shallow Junctions based on Atomistic Modeling
T. Noda[1], W. Vandervorst[2], S. Felch[3], V. Parihar[3], C. Vrancken[2], S. Severi[2], T. Y. Hoffmann[2], A. Falpin[2], B. van Daele[2], T. Jannssens[2], H. Bender[2], P. Eyben[2], M. Niwa[1], R. Schreutelkamp[3], F. Nouri[3], P. P. Absil[2], M. Jurczak[2], K. De Meyer[2] and S. Biesemans[2],
[1]Matsushita Electric Industrial Co., Ltd., [2]IMEC and [3]AMAT (Japan)

15:45 A-5-2
Electron Holography Characterization of Ultra-Shallow Junctions in 30-nm Gate-length MOSFETs
N. Ikarashi[1], M. Oshida[1], M. Miyamura[1], M. Saitoh[1], A. Mineji[2] and S. Shishiguchi[2],
[1]NEC Corp. and [2]NEC Electronics Corp. (Japan)

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-5: Mobility Characterization
(15:15-16:35)
Chairs: Y. Kamakura (Osaka Univ.)
K. Takeuchi (NEC Corp.)

15:15 B-5-1
Experimental Study of Uniaxial Stress Effects on Coulomb-limited Electron and Hole Mobility in Si-MOSFETs
S. Kobayashi, M. Saitoh, Y. Nakabayashi and K. Uchida,
Toshiba Corp. (Japan)

15:35 B-5-2
Physical Mechanism for Hole Mobility Enhancement in (110)-Surface Strained-Si/Strained-SiGe Structures with Anisotropic/Biaxial Strain
T. Mizuno[1,3], T. Irisawa[2], N. Hirashita[2], Y. Moriyama[2], T. Tezuka[2], N. Sugiyama[2] and S. Takagi[1,4],
[1]MIRAI-AIST, [2]MIRAI-ASET, [3]Kanagawa Univ. and [4]Univ. of Tokyo (Japan)

Room 201A (C)

Area 12: Spintronic Materials and Devices

C-5: Symposium on Magnetic Tunnel Junctions and Beyond
(15:15-16:45)
Chairs: M. Tanaka (The Univ. of Tokyo)
K. Ando (AIST)

15:15 C-5-1(Invited)
Spin Transfer Torque RAM（STT-RAM) Technology
Y. Huai, Z. Diao, Y. Ding, A. Panchula, S. Wang, Z. Li, D. Apalkov, X. Luo, H. Nagai, A. Driskill-Smith and E. Chen, *Grandis, Inc. (USA)*

15:45 C-5-2(Invited)
Structural Study on CoFeB/MgO/CoFeB Magnetic Tunnel Junctions
K. Tsunekawa[1,2], Y. Choi[1], Y. Nagamine[1], H. Maehara[1], D. D. Djayaprawira[1], T. Takeuchi[2] and Y. Kitamoto[2],
[1]Canon ANELVA Corp. and [2]Tokyo Tech. (Japan)

Room 201B (D)

Area 5: Advanced Circuits and Systems

D-5: RF CMOS Circuits and Systems
(15:15-16:15)
Chairs: K. Masu (Tokyo Tech.)
T. Matsuoka (Osaka Univ.)

15:15 D-5-1(Invited)
RF CMOS Circuits-Overview and Perspective
T. Tsukahara,
Univ. of Aizu (Japan)

15:45 D-5-2(Invited)
Compensation techniques for integrated analog device issues
A. Matsuzawa,
Tokyo Tech. (Japan)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-5: Special Session: Photonic Crystals and Si Photonics III
(15:15-16:30)
Chairs: M. Tokushima (NEC Corp.)
O. Wada (Kobe Univ.)

15:15 E-5-1
Thermal Modulation of Group Delay of Pillar-Photonic-Crystal Waveguide
M. Tokushima,
NEC Corp. (Japan)

15:30 E-5-2(Invited)
Plasmonic Crystals and Nanophotonic Sensing Devices
T. A. Kelf[1], Y. Sugawara[2], R. M. Cole[3], N. M. B. Perney[3], J. J. Baumberg[3], M. E. Abdelsalam[3] and P. N. Bartlett[3],
[1]Hokkaido Univ., [2]FUJIFILM Corp. and [3]Univ. of Southampton (Japan)

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-5: Group-IV Semiconductors II
(15:15-16:30)
Chairs: K. Nishi (NEC Corp.)
H. Yamaguchi (NTT Basic Research Labs.)

15:15 F-5-1(Invited)
Bottom-up approach for the nanopatterning of Si(001)
R. Koch, *Johannes Kepler Univ. (Austria)*

15:45 F-5-2
Plasma Deposition of HfO_2 and TiO_2 onto Plasma-Nitrided Ge Surfaces
S. Lee[1], G. Lucovsky[1], J. P. Long[1] and J. Lüning[2],
[1]North Carolina State Univ. and [2]Stanford Synchrotron Research Lab. (USA)

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-5: High-Speed Devices and ICs II
(15:15-16:15)
Chairs: S. Kuroda (Eudyna Devices Inc.)
K. Maezawa (Univ. of Toyama)

15:15 G-5-1
A 7.6-ps Pulse Generator Using 0.13-μm InP-based HEMTs for Ultra Wide-Band Impulse Radio Systems
Y. Nakasha[1], Y. Kawano[1], T. Suzuki[1], T. Ohki[2], T. Takahashi[1], K. Makiyama[1], T. Hirose[2] and N. Hara[1],
[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd. (Japan)

15:30 G-5-2
Novel MOBILE Circuits Using 3 RTDs Operating up to 12.5 Gb/s
H. Kim, N. Jeon and K. Seo, *Seoul National Univ. (Korea)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-5: Nanowire Growth and Devices I
(15:15-16:30)
Chairs: J. Motohisa (Hokkaido Univ.)
T. Fukui (Hokkaido Univ.)

15:15 H-5-1(Invited)
III-V semiconductor hetero-structure nanowires by selective area MOVPE
T. Fukui, S. Hara and J. Motohisa, *Hokkaido Univ. (Japan)*

15:45 H-5-2
InP Nodes in GaP-based Free-standing Nanowires on Si(111)
K. Tateno, G. Zhang, T. Sogawa and H. Nakano, *NTT Corp. (Japan)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-5: PRAM
(15:15-16:25)
Chairs: M. Moniwa (Renesas Technology Corp.)
I. Asano (Elpida Memory, Inc.)

15:15 J-5-1(Invited)
Current Status and Future View of Phase Change Memory
Y. Matsui, *Hitachi, Ltd. (Japan)*

15:45 J-5-2
Three-Dimensional Electro-Thermal Compact Model for Reset Operation of Phase Change Memories
A. Sakai, K. Sonoda, M. Moniwa, K. Ishikawa, O. Tsuchiya and Y. Inoue, *Renesas Tech. Corp. (Japan)*

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

16:05 A-5-3
$Si_{1-x}Ge_x$/Si Selective Etch with HCl for Thin Si-Channel Transistors Integration
N. Loubet[1], S. Denorme[1], A. Pouydebasque[2], F. Leverd[1], P. Gouraud[1], C. Tallaron[1], T. Skotnicki[1] and D. Dutartre[1], *[1]STMicroelectronics and [2]NXP Semiconductors (France)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

15:55 B-5-3
Behavior of Low-Temperature Phonon-Limited Electron Mobility of Double-Gate Field-Effect Transistor with (111) Si Surface Channel
T. Yamamura, S. Sato and Y. Omura, *Kansai Univ. (Japan)*

16:15 B-5-4
Mobility Degradation in (110)-Oriented Ultra-thin Body Double-Gate pMOSFETs with SOI Thickness of less than 5nm
K. Shimizu and T. Hiramoto, *Univ. of Tokyo (Japan)*

Room 201A (C)

Area 12: Spintronic Materials and Devices

16:15 C-5-3(Invited)
Giant TMR in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions
S. Ikeda[1], J. Hayakawa[2,1], Y. M. Lee[1,3], K. Miura[2,1], R. Sasaki[1], F. Matsukura[1], T. Meguro[1] and H. Ohno[1], *[1]Tohoku Univ., [2]Hitachi, Ltd. and [3]Fujitsu Labs. Ltd. (Japan)*

Room 201B (D)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

16:00 E-5-3
Application of Surface-Plasmon Antenna to Near-Infrared Photodetectors for Optical Communication
D. Okamoto, J. Fujikata, K. Nishi and K. Ohashi, *NEC Corp. (Japan)*

16:15 E-5-4
Cavity mode in trilayer Ag/SiO_2/Au plasmonic thermal emitter
M. W. Tsai, Y. W. Jiang, C. Y. Chen, Y. H. Ye and S. C. Lee, *National Taiwan Univ. (Taiwan)*

Break

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

16:00 F-5-3
A Novel Process-Compatible Floating Channel Crystallization Technique to Fabricate High-Performance Poly-Si TFTs
C. W. Chang[1], J. W. Lee[2], C. L. Chang[1] and T. F. Lei[1], *[1]National Chiao Tung Univ. and [2]TSMC (Taiwan)*

16:15 F-5-4
Low Temperature Ultra-thin Hafnium Oxide Dielectrics by Sputtering of Hf Metal on Tilted Substrate Followed by Nitric Acid Oxidation then Anodization Compensation in D. I. Water
C. H. Chang and J. G. Hwu, *National Taiwan Univ. (Taiwan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

15:45 G-5-3
Ultra-Short Pulse Generators Using Resonant Tunneling Diodes and Their Integration with Antennas on Ceramic Substrates
N. Kamegai[1], S. Kishimoto[1], K. Maezawa[2], T. Mizutani[1], H. Andoh[3], K. Akamatsu[4] and H. Nakata[4], *[1]Nagoya Univ., [2]Univ. of Toyama, [3]Toyota National College of Tech. and [4]Nippon Mining & Metals Co., Ltd. (Japan)*

16:00 G-5-4
High Tuning-Range VCO Using a Gated Tunnel Diode
M. Ärlelid, M. Nilsson, G. Astromskas, E. Lind and L. E. Wernersson, *Lund Univ. (Sweden)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

16:00 H-5-3
CMOS Compatible Si-Nanowire Inverter Logic Gate for Low Power Applications
N. Singh, K. D. Buddharaju, S. C. Rustagi, S. H. G. Teo, A. Agarwal, L. Y. Wong, L. J. Tang, C. H. Tung, J. Yu, G. Q. Lo, N. Balasubramanian and D. L. Kwong, *Inst. of Microelectronics (Singapore)*

16:15 H-5-4
Silicon Nanowire Schottky Barrier NMOS Transistors
E. J. Tan[1,2,3], K. L. Pey[1], N. Singh[2], G. Q. Lo[2], D. Z. Chi[3], K. M. Hoe[2], P. S. Lee[1] and G. D. Cui[1], *[1]Nanyang Technological Univ., [2]Inst. of Microelectronics and [3]Inst.of Materials Research and Engineering (Singapore)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

16:05 J-5-3
Comprehensive HSPICE Model of Phase Change Memory Cell for Static and Transient Programming
D. S. Chao[1, 2], Y. K. Chen[3], Y. B. Liao[3], M. H. Chiang[3], C. Lien[2], M. J. Kao[1] and M. J. Tsai[1], *[1]EOL/ITRI, [2]National Tsing Hua Univ. and [3]National Ilan Univ. (Taiwan)*

Break

Room 101 (A)

Area 1: Advanced Gate Stack/Si Processing Science

A-6: Reliability-II
(16:45-18:05)
Chairs: K. Shiraishi (Univ. of Tsukuba)
Y. Nara (Selete)

16:45 A-6-1
Effects of O_2 Plasma Treatment on the Reliabilities of Metal Gate/High-k Dielectric MOSFETs
K. T. Lee[1,5], C. Y. Kang[2], R. Choi[2], S. C. Song[2], B. H. Lee[2,3], H. D. Lee[4,5] and Y. H. Jeong[1], *[1]Pohang Univ. of Sci. and Tech., [2]SEMATECH, [3]IBM, [4]Chungnam National Univ. and [5]Univ. of Taxas at Austin (Korea)*

17:05 A-6-2
The origin of slow and fast trapping under Bias Temperature Instability in HfSiO MOSFET
M. Jo[1], H. Park[1], M. Chang[1], H. S. Jung[2], J. H. Lee[2] and H. Hwang[1], *[1]GIST and [2]Samsung Electronics Co., Ltd. (Korea)*

Room 102 (B)

Area 3: CMOS Devices/Device Physics

B-6: Device Technology
(16:45-18:05)
Chairs: K. Shibahara (Hiroshima Univ.)
H. C. Lin (National Chiao Tung Univ.)

16:45 B-6-1
Modeling of Floating-Body Effect in SOI-MOSFET with Complete Surface-Potential Description
T. Murakami, M. Ando, N. Sadachika and M. Miura-Mattausch, *Hiroshima Univ. (Japan)*

17:05 B-6-2
Device Performance and Reliability Considerations of Biaxially Strained Si by Wafer-Bonding-Technology
W. Y. Loh[1], D. S. H. Chan[2], D. Y. J. Choo[1,2], S. M. Koh[1,2], R. Yang[1], X. W. Zhang[1], C. Cai[3], G. Q. Lo[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics, [2]National Univ. of Singapore and [3]IHPC (Singapore)*

Room 201A (C)

Area 12: Spintronic Materials and Devices

C-6: Symposium on Magnetic Tunnel Junctions and Beyond
(17:00-18:00)
Chairs: K. Ando (AIST)
M. Tanaka (Univ. of Tokyo)

17:00 C-6-1(Invited)
Giant TMR and future nonvolatile memory
S. S. P. Parkin, *IBM (USA)*

17:30 C-6-2(Invited)
Spin Injection and Transport in Ferromagnet/semiconductor Structures
C. J. Palmstrom, *Univ. of Minnesota (USA)*

Room 201B (D)

Room 202A (E)

Area 7: Photonic Devices and Device Physics

E-6: Detectors and Sensors
(16:45-18:00)
Chairs: M. Gotoda (Mitsubishi Electric Corp.)
M. Sugawara (Fujitsu Labs. Ltd.)

16:45 E-6-1
In(Ga)As Quantum Rings for Terahertz Detectors
J. H. Dai, J. H. Lee, Y. L. Lin and S. C. Lee, *National Taiwan Univ. (Taiwan)*

17:00 E-6-2
Design of a spin-coherent photo detector for high-fidelity and high-yield photon-spin quantum state transfer
Y. Rikitake[1,2], H. Imamura[1,2] and H. Kosaka[1,3], *[1]CREST-JST, [2]AIST and [3]Tohoku Univ. (Japan)*

Room 202B (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-6: Group-IV Semiconductors III
(16:45-17:45)
Chairs: R. Koch (Johannes Kepler Univ.)
S. Shimomura (Ehime Univ.)

16:45 F-6-1
MBE-grown $Ge_{1-x}C_x$ nanocrystals by using a novel bio-nanoprocess due to protein "ferritin"
Y. Nakama, J. Ohta and M. Nunoshita, *NAIST (Japan)*

17:00 F-6-2
Enhancement of crystal growth rate of Bio-Nano Crystallization by Pulsed Rapid Thermal Annealing
M. Ochi[1], Y. Nanjo[1], Y. Sugawara[1], Y. Uraoka[1], T. Fuyuki[1], M. Okuda[2] and I. Yamashita[1,2], *[1]NAIST and [2]Matsushita Electric Industrial Co., Ltd. (Japan)*

Room 303 (G)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

G-6: Process and Characterization
(16:45-18:00)
Chairs: A. Nakagawa (New Japan Radio Co., Ltd.)
K. J. Chen (Hong Kong Univ. of Sci. and Tech.)

16:45 G-6-1
Dynamic response of interface state charges in GaN MIS structures
K. Ooyama[1,2], H. Kato[1], M. Miczek[1] and T. Hashizume[1], *[1]Hokkaido Univ. and [2]Sumitomo Metal Mining (Japan)*

17:00 G-6-2
Temperature dependence of current-voltage characteristics for AlGaN-based vertical conducting diodes
A. Nishikawa, K. Kumakura and T. Makimoto, *NTT Corp. (Japan)*

Room 304 (H)

Area 13: Applications of Nanotubes and Nanowires

H-6: Nanowire Growth and Devices II
(16:45-17:45)
Chairs: K. Tateno (NTT)
K. Ishibashi (RIKEN)

16:45 H-6-1
Poly-Si Nanowire Thin-Film Transistors with Inverse-T Gate
H. H. Hsu[1], H. C. Lin[1,2], J. F. Huang[1] and C. J. Su[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)*

17:00 H-6-2
Strained Ge-rich SiGe Nanowire pFETs with High-k/Metal Gate Fabricated using Germanium Condensation Technique
Y. Jiang[1,2], N. Singh[1], D. S. H. Chan[2], T. Y. Liow[1,2], W. Y. Loh[1], S. Balakumar[1], Y. Sun[1], G. Q. Lo[1] and D. L. Kwong[1,2], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore (Singapore)*

Room 405 (I)

Room 406 (J)

Area 4: Advanced Memory Technology

J-6: ReRAM
(16:45-17:55)
Chairs: K. Ito (NEC Corp.)
Y. Shimamoto (Hitachi Ltd.)

16:45 J-6-1(Invited)
Current Development Status and Future Challenge of Metal Oxide RRAM Technologies
N. Awaya, *Sharp Corp. (Japan)*

17:15 J-6-2
Elucidation of ReRAM Mechanism and Improvement of Memory Characteristics by HPHA
D. Seong, D. Lee, S. Oh, M. Pyun and H. Hwang, *GIST (Korea)*

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	**Area 3: CMOS Devices/Device Physics**			**Area 7: Photonic Devices and Device Physics**
17:25 A-6-3 A Comparative Study of Plasma Source-Dependent Charging Polarity in MOSFETs with High-k and SiO_2 Gate Dielectrics K. Eriguchi[1], M. Kamei[1], D. Hamada[1], K. Okada[2] and K. Ono[1], *[1]Kyoto Univ. and [2]MIRAI-AIST (Japan)*	**17:25 B-6-3** LDMOS Model for Device and Circuit Optimization M. Yokomichi, M. Miyake, T. Kajiwara, N. Sadachika, A. Yumisaki, H. J. Mattausch and M. Miura-Mattausch, *Hiroshima Univ. (Japan)*			**17:15 E-6-3** Functional Enhancement of Metal-Semiconductor-Metal (MSM) Infrared Photodetectors on Heteroepitaxial SiGe-on-Si Using the Anodic Oxidation/Passivation Method R. W. Chuang[1], Z. L. Liao[1], H. T. Chiang[1] and N. Usami[2], *[1]National Cheng Kung Univ. and [2]Tohoku Univ. (Taiwan)*
17:45 A-6-4 Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs N. Mise, T. Matsuki, T. Watanabe, T. Robata, T. Morooka, T. Eimori and Y. Nara, *Selete (Japan)*	**17:45 B-6-4** A New Insulated Gate Bipolar Transistor Structure employing an Embedded Over-current Protection Device I. H. Ji [1], K. H. Cho[1], Y. H. Choi[1], S. S. Kim[2], K. H. Oh[2], C. M. Yun[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Fairchild Semiconductor (Korea)*			**17:30 E-6-4** A MSM Photodetector on p-type GaN for UV Image system H. B. Lee, H. I. Cho, J. H. Lee and S. H. Hahm, *Kyungpook National Univ. (Korea)*
				17:45 E-6-5 MOVPE Prepared ZnO/Si Heterojunction Diodes with Dual Functions: Light-Emission and UV Photo-Detection J. D. Ye[1], S. L. Gu[2], X. W. Sun[1,3], G. Q. Lo[1], D. L. Kwong[1] and Y. D. Zheng[2], *[1]Inst. of Microelectronics, [2]Nanjing Univ. and [3]Nanyang Technological Univ. (Singapore)*

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**	**Area 13: Applications of Nanotubes and Nanowires**		**Area 4: Advanced Memory Technology**
17:15 F-6-3 Compositionally Bi-layered Formation of Interfacial Voids in a Porous Anodic Alumina Template Directly Formed on Si H. S. Seo[1], Y. G. Jung[1], S. W. Jee[1], J. M. Yang[2] and J. H. Lee[1], *[1]Hanyang Univ. and [2]National Nanofab Center (Korea)*	**17:15 G-6-3** Investigations of Metal/Insulator/AlGaN/GaN Structures by Capacitance-Voltage Measurements and Auger Chemical Profiling B. Adamowicz[1], M. Miczek[1,2], T. Hashizume[2], A. Klimasek[1], P. Bobek[1] and J. Żywicki[3], *[1]Silesian Univ. of Tech., [2]Hokkaido Univ. and [3]High-Tech International Services Inc. (Poland)*	**17:15 H-6-3** High quality $Si_{1-x}Ge_x$ nanowire and its application to MOSFET integrated with HfO_2/TaN/Ta gate stack W. F. Yang[1], S. J. Lee[1], S. J. Whang[1], S. Y. Lim[1], B. J. Cho[1] and D. L. Kwong[2], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics (Singapore)*		**17:35 J-6-3** Gd doping improved resistive switching characteristics of TiO_2-based resistive memory devices L. F. Liu, J. F. Kang, H. Tang, N. Xu, Y. Wang, X.. Y. Liu, X. Zhang and R. Q. Han, *Peking Univ. (China)*
17:30 F-6-4 Computational Chemistry Study of Diamond-like Carbon: Functions and Structure Control by Frictional Force Y. Morita, T. Shibata, T. Onodera, R. Sahnoun, M. Koyama, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*	**17:30 G-6-4** Shuttle Activation Annealing of Implanted Al in 4H-SiC T. Watanabe, R. Hattori, M. Imaizumi and T. Oomori, *Mitsubishi Electric Corp. (Japan)*	**17:30 H-6-4** Epitaxial insertion of Au_5Si nanodiscs during the growth of silicon nanowires H. D. Um, Y. G. Jung, H. S. Seo, K. T. Park and J. H. Lee, *Hanyang Univ. (Korea)*		
	17:45 G-6-5 Silicon oxide Gate Dielectric on N-Type 4H-SiC Prepared by Low Thermal Budget Anodization Method K. C. Chuang and J. G. Hwu, *National Taiwan Univ. (Taiwan)*			

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"