POSTER SESSION (13:00-15:00, Room 501, 502, 511/512)

P1
Advanced Gate Stack / Si Processing Science
(28 Papers)

P-1-1
Suppression of Leakage Current and Moisture Absorption of La_2O_3 films with Ultraviolet Ozone Post Treatment
Y. Zhao, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

P-1-2
Dielectric Constant Behavior of Oriented Tetragonal Zr-Si-O System
T. Ino, Y. Kamimuta, M. Koyama and A. Nishiyama, *Toshiba Corp. Japan*

P-1-3
Interface Layer Control at Y_2O_3/Ge by N_2 and O_2 Annealing on Ge(100) and Ge(111) Surfaces
H. Nomura, K. Kita, T. Nishimura and A. Toriumi, *Univ. of Tokyo, Japan*

P-1-4
Non-crystalline Stable Gate Dielectrics for Advanced Nano-Cmos Devices
G. Lucovsky[1], S. Lee[1] and J. Lüning[2], *[1]North Carolina State Univ. and [2]Stanford Synchrotron Radiation Lab., USA*

P-1-5
Hf and N Release from HfSiON in High-Temperature Annealing Induced by Oxygen Incorporation
T. Matsuki, S. Inumiya, N. Mise, T. Eimori and Y. Nara, *Semiconductor Leading Edge Techonologies, Inc., Japan*

P-1-6
Epitaxial High-K Oxide Metal Gate MOSFETs: Damascene CMP Process Integration and Electrical Results
R. Endres, Y. Stefanov and U. Schwalke, *Darmstadt Univ. of Technology, Germany*

P-1-7
Impact of PVD-based In-situ Fabrication Method for Metal/High-k Gate Stacks
S. Horie[1], T. Minami[2], N. Kitano[2], M. Kosuda[2], H. Watanabe[1] and K. Yasutake[1], *[1]Osaka Univ. and [2]Canon ANELVA Corp., Japan*

P-1-8
Investigation of Inversion C-V Reconstruction for Long-Channel MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach
W. Lee[1], P. Su[1], K. W. Su[2], C. S. Chiang[2] and S. Liu[2], *[1]National Chiao Tung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P-1-9
Behavior of Local Charge Trapping Sites in La_2O_3-Al_2O_3 Composite Films under Constant Voltage Stress
T. Sago, A. Seko, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*

P-1-10
Improvement of mobility and NBTI reliability in MOSFETs with ALD-Si-nitride/SiO_2 stack dielectrics and P^+-poly Si gate
S. Zhu[1], A. Nakajima[1], T. Ohashi[2] and H. Miyake[2], *[1]Hiroshima Univ. and [2]Elpida Memory Inc., Japan*

P-1-11
Near Surface Oxide Trap Density Profiling in NO and Remote Plasma Nitrided Oxides in Nano-Scale MOSFETs, Using Multi-Temperature Charge Pumping Technique: No+ vs. Oxide Processing
Y. Son[1], C. K. Baek[2], B. Kim[2], I. S. Han[1], T. G. Goo[1], H. D. Lee[1] and D. M. Kim[2], *[1]Chungnam National Univ. and [2]Korea Inst. for Advanced Study, Korea*

P-1-12
Ultra-thin Oxide Lifetime Projection and Comparison of nFET and pFET for 90nm/65nm Application
C. L. Lin, T. Kao, J. P. Chen, J. Shieh and K. C. Su, *United Microelectronics Corp. (UMC), Taiwan*

P-1-13
Theoretical Simulation of Dielectric Breakdown by Molecular Dynamics and Tight-Binding Quantum Chemistry Method
Z. Zhu[1], A. Chutia[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. Del Carpio[1], P. Selvam[3] and A. Miyamoto[1,3], *[1]Tohoku Univ., [2]PRESTO-JST and [3]NICHe, Tohoku Univ., Japan*

P-1-14
Electrical characteristic improvement of high-k gated MOS device by nitridation treatment using plasma immersion ion implantation (PIII)
K. S. Chang-Liao[1], P. H. Tsai[1], H. Y. Kao[1], T. K. Wang[1], S. F. Huang[2], W. F. Tsai[2] and C. F. Ai[2], *[1]National Tsing Hue Univ. and [2]Inst. of Nuclear Energy Research, Taiwan*

P-1-15
Effect of Gate Oxide Thickness Uniformity on the Characteristics of Three-dimensional Transistors
H. J. Cho, T. Y. Kim, Y. S. Kim, S. A. Jang, S. R. Lee, K. Y. Lim, M. G. Sung, J. H. Kim, S. W. Oh, T. W. Jung, T. K. Oh, Y. T. Hwang, Y. H. Kim, H. S. Yang and J. W. Kim, *Hynix Semiconductor Inc., Korea*

P-1-16
Precise Extraction of Metal Gate Work Function from Bevel Structures
A. Kuriyama[1,3,4], O. Faynot[1], L. Brévard[1], A. Tozzo[1], L. Clerc[1], J. Mitard[1,2], V. Vidal[1,2], S. Deleonibus[1], S. Cristoloveanu[3] and H. Iwai[4], *[1]CEA-LETI, [2]STMicroelectronics, [3]IMEP and [4]Tokyo Tech, France*

P-1-17
Work Function Modulation Using Thin Interdiffused Metal Layers for Dual Metal-Gate Technology
A. E. Lim[1], W. S. Hwang [1], X. P. Wang[1], D. L. Kwong[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*

P-1-18
Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes
T. Matsukawa, Y. X. Liu, K. Endo, M. Masahara, K. Ishii, H. Yamauchi, J. Tsukada and E. Suzuki, *National Inst. Adv. Ind. Sci. and Technol., Japan*

P-1-19
Nitrogen Induced Extrinsic States (NIES) in Effective Work Function Instability of TiNx/SiO_2 and TiNx/HfO_2 Gate Stacks
C. S. Lai[1], J. C. Wang[2], S. C. Yang[1], J. Y. Wong[1] and S. K. Peng[1], *[1]Univ. of Chang Gung and [2]Nanya Technology Corp. Taiwan*

P-1-20
Physical and Electrical Characteristics of HfN Metal Gate Electrode Synthesized by Post-Rapid Thermal Annealing-assisted MOCVD
W. Wang[1], T. Nabatame[2] and Y. Shimogaki[1], *[1]Univ. of Tokyo and [2]MIRAI-ASET, Japan*

P-1-21
Composition Dependence of Work Function in Metal (Ni, Pt)-Germanide Gate Electrodes
D. Ikeno, K. Furumai, H. Kondo, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*

P-1-22
Stress-Relaxation Process during Post-Annealing in SGOI Formed by H^+ Irradiation and Oxidation-Induced Ge Condensation
M. Tanaka[1], T. Sadoh[1], K. Matsumoto[2], T. Enokida[3] and M. Miyao[1], *[1]Kyushu Univ., [2]SUMCO Corp. and [3]Fukuryo Semicon Engineering Corp., Japan*

P-1-23
Microscopic Mechanism of Oxygen Transport during Thermal Silicon Oxidation
H. Kageshima[1], M. Uematsu[1], T. Akiyama[2] and T. Ito[2], *[1]NTT Basic Research Labs. and [2]Mie Univ., Japan*

P-1-24
Low-Leakage-Current Ultra-thin SiO_2 Film by Low-Temperature Neutral Beam Oxidation
T. Ikoma[1], C. Taguchi[1], S. Fukuda[1], K. Endo[2], H. Watanabe[3] and S. Samukawa[1], *[1]Tohoku Univ., [2]AIST and [3]Osaka Univ., Japan*

P-1-25
Rate-Limiting Reaction of Layer-by-Layer Oxidation on Si(001) Surfaces: Dependence on the First Oxide Layer Growth Kinetics
S. Ogawa and Y. Takakuwa, *Tohoku Univ., Japan*

P-1-26
Xe Preamorphization Implantation for Transient Enhanced Diffusion Suppression of As in Ge Substrate
T. Fukunaga, K. Hosawa, T. Hosoi and K. Shibahara, *Hiroshima Univ. , Japan*

P-1-27
Low Leakage Current and Low Resistivity p^+n Diodes on Si(110) Fabricated by Ga^+/B^+ Combination I/I and Low Temperature Annealing
H. Imai, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P-1-28
Effects of CF_3I Plasma for Reducing UV Irradiation Damage in Dielectric Film Etching Processes
Y. Ichihashi[1,2], Y. Ishikawa[1], R. Shimizu[2], H. Mizuhara[2], M. Okigawa[2] and S. Samukawa[1], *[1]Tohoku Univ. and [2]Sanyo Electric Co., Ltd., Japan*

P2
Characterization and Materials Engineering for Interconnect Integration
(17 Papers)

P-2-1
Formation of Mesoporous Pure Silica Zeolite Film
T. Seo[1], T. Yoshino[2], N. Hata[2] and T. Kikkawa[1,2], *[1]Hiroshima Univ. and [2]National Inst. of Advanced Industrial Science and Technology, Japan*

P-2-2
Pure-Silica Zeolite Films Prepared by a Vapor Phase Transport Method
Y. Cho[1], K. Kohmura[2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Mitsui Chem., Japan*

P-2-3
Thermally Stable Carbon-Doped Silicon Oxide Films Deposited at Room Temperature
K. Yamaoka, H. Kato, D. Tsukiyama, Y. Yoshizako, Y. Terai and Y. Fujiwara, *Osaka Univ., Japan*

P-2-4
Comparison of the Planarization Technologies for the Next Generation
I. Kobata[1], Y. Wada[1], Y. Toma[2], T. Suzuki[2], A. Kodera[2], K. Tokushige[1], A. Fukunaga[1] and M. Tsujimura[1], *[1]Ebara Corporation and [2]Ebara Research Co., Ltd., Japan*

P-2-5
Application of Double Polishing Pad for Shallow Trench Isolation Chemical Mechanical Polishing Process
Y. J. Seo and S. W. Park, *Daebul Univ., South korea*

P-2-6
Analyses of Interface Adhesion between Cu and SiCN Etch Stop Layers by Nanoindentation and Nanoscratch Tests
S. Y. Chang and Y. S. Lee, *National Chung Hsing Univ., Taiwan*

P-2-7
Characterization of pore sealing effect on trench sidewalls in porous low-k films by vapor adsorption in-situ spectroscopic ellipsometry
N. Hata[1], K. Koga[2], K. Sumiya[2], S. Takada[1], M. Tada[2], Y. Kawamoto[2] and T. Kanayama[1], *[1]MIRAI-ASRC-AIST and [2]CASMAT, Japan*

P-2-8
Anisotropic mechanical characterization of Cu single crystals and thin films
S. Shimizu, N. Kojima and J. Ye, *NISSAN ARC, Ltd., Japan*

P-2-10
Relationship between structure and conductance of nanometer-sized iridium contacts
M. Ryu[1] and T. Kizuka[1,2], *Univ. of Tsukuba and [2]JST, Japan*

P-2-11
Effectiveness of Titanium and Carbon capping layer in NiSi formation with Ni film deposited by Atomic Layer Deposition
C. M. Yang, S. W. Yun, J. B. Ha, K. I. Na, H. I. Cho, H. B. Lee, J. H. Jeong, S. H. Hahm, S. H. Kong and J. H. Lee, *Kyungpook National Univ. Korea*

P-2-12
A Study of Relationship of Wafer Breakage vs. Wafer Edge Analysis
S. H. Chen[1], S. L. Chen[2] and W. K. Yeh[3], *[1]Tung Fang Institute of Technology, [2]National United Univ. and [3]National Univ. of Kaohsiung, Taiwan*

P-2-13
Characterization of Void in Bonded SOI Wafers by Controlling Coherence Length of Near-Infrared Microscope
N. Ajari, J. Uchikosi, T. Hirokane, K. Arima and M. Morita, *Osaka Univ., Japan*

P-2-14
Evaluation of Alignment Accuracy for Wafer Bonding Using Moiré Technique
C. Wang and T. Suga, *Univ. of Tokyo, Japan*

P-2-15
Sub-Atmospheric Chemical Vapor Deposition Process for Chip-to-Wafer 3-Dimensional Integration
H. Kikuchi, Y. Yamada, A. M. Ali, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. Japan*

P-2-16
A Low Temperature Process of Bonding Fine Pitch Au/Sn Bumps in Air
Y. H. Wang[1], K. Nishida[2], M. Hutter[3], T. Kimura[2] and T. Suga[1], *[1]Univ. of Tokyo, [2]National Inst. for Materials Science and [3]Fraunhofer IZM, Japan*

P-2-17
Finite element analysis of nanometer-scale contact for low temperature bonding
T. Higashino and T. Suga, *Univ. of Tokyo, Japan*

P-2-18
Low Temperature Interconnection of Cu Micro-bump on Polyimide and Ni/Au Film by Surface Activated Flip Chip Method
Z. Xu and T. Suga, *Univ. of Tokyo, Japan*

P3
CMOS Devices / Device Physics
(24 Papers)

P-3-1
An Efficient Mobility Enhancement Engineering on 65nm FUSI CMOSFETs using a Second CESL Process
C. M. Lai[1], Y. K. Fang[1], C. T. Lin[1], W. K. Yeh[2], C. W. Hsu[2], C. H. Hsu[3], L. W. Chen[3] and M. Ma[3], *[1]National Cheng Kung Univ. [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P-3-2
Monte Carlo Simulation of Band-to-band Tunneling in Silicon Devices
Z. L. Xia, G. Du, Y. C. Song, J. Wang, X. Y. Liu, J. F. Kang and R. Q. Han, *Peking Univ., China*

P-3-3
Local Strained Channel nMOSFETs by Different Poly-Si Gate and SiN Capping Layer Thicknesses: Mobility, Simulation, Size Dependence, and Hot Carrier Stress
Y. J. Lee[1], C. H. Fan[2], W. Y. Lin[3], C. C. Wan[2], B. R. Huang[3], W. L. Yang[2], T. S. Chao[4] and D. S. Chuu[2], *[1]National Nano Device Lab., [2]Feng Chia Univ. and [3]Department of Electronic Engineering, National Yunlin Univ. of Science and Technology, Taiwan*

P-3-4
Characterization of Subthreshold Behavior of Narrow-Channel SOI nMOSFET with Additional Side-Gate Electrodes
K. Okuyama, K. Yoshikawa and H. Sunami, *Hiroshima Univ. Japan*

P-3-5
Gate Capacitance Analysis of Multi-finger MOSFETs for RF Applications
H. Aoki and M. Shimasue, *MODECH Inc., Japan*

P-3-6
Characteristics of Poly-Si Nanowire Thin Film Transistors with Double-Gated Structures
C. J. Su[1], H. C. Lin[1,2], C. C. Hung[1], H. H. Tsai[1], Y. J. Lee[2] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P-3-7
A New 1200V PT-IGBT with Protection Circuit employing the Lateral IGBT and Floating p-well Voltage Sensing Scheme
I. H. Ji[1], Y. H. Choi[1], B. C. Jeon[1], S. C. Lee[2], S. S. Kim[2], K. H. Oh[2], C. M. Yun[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Fairchild Semiconductor Korea, Korea*

P-3-8
Efficient Improvement on Device Performance for sub-90nm SOI CMOSFETs
C. T. Lin[1], Y. K. Fang[1], C. M. Lai[1], W. K. Yeh[2], C. W. Hsu[2], C. H. Hsu[3], L. W. Chen[3] and M. Ma[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P-3-9
Multiband Simulation of Quantum Electron Transport in Nano-Scale Devices Based on Non-Equilibrium Green's Function
H. Fitriawan, S. Souma, M. Ogawa and T. Miyoshi, *Kobe University, Japan*

P-3-10
Effect of Mobility Degradation and Supply Voltage on NBTI Induced Drain Current Degradation
J. F. Chen[1], D. H. Yang[1], C. Y. Lin[2] and S. Y. Wu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P-3-11
Impact of Source/Drain $Si_{1-y}C_y$ Stressors on the Silicon-on-Insulator NMOSFETs
J. Huang, W. C. Wang, J. W. Fan and S. T. Chang, *National Chung Hsing Univ. Taiwan*

P-3-13
Modeling of Drain Bias Dependence on Threshold Voltage Shift Under Negative Gate Bias Stress of a-Si: H TFTs
H. Y. Tseng, K. Y. Chiang and C. P. Kung, *Industrial Technology Research Institute (ITRI), Taiwan*

P-3-14
A New SOI Lateral Insulated Gate Bipolar Transistor and Lateral Diode employing the Separated Schottky Anode for a Power Integrated Circuit
I. H. Ji, Y. H. Choi, M. W. Ha and M. K. Han, *Seoul National Univ., Korea*

P-3-15
Impacts of LP-SiN Capping Layer and Lateral Diffusion of interface Trap on Hot Carrier Stress of NMOSFETs
C. Y. Lu[1], C. S. Lu[1], Y. L. Hsieh[1], Y. J. Lee[2], H. C. Lin[1,2] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P-3-16
Effects of Strained Layers on Zener Tunneling in Silicon Nanostructures
H. Minari and N. Mori, *Osaka Univ., Japan*

P-3-17
A New Statistical Evaluation Method for the Variation of MOSFETs
S. Watabe, S. Sugawa, A. Teramoto and T. Ohmi, *Tohoku Univ., Japan*

P-3-18
A Novel Self Aligned Design Adapted Gate All Around (SADAGAA) MOSFET including two stacked Channels : A High Co-Integration Potential
R. Wacquez[1,2,3], R. Cerutti[1], P. Coronel[1], A. Cros[1], D. Fleury[1], A. Pouydebasque[4], J. Bustos[1], S. Harrison[4], N. Loubet[1], S. Borel[3], D. Lenoble[1], D. Delille[4], F. Leverd[1], F. Judong[1], MP. Samson[1,3], N. Vuillet[1,3], B. Guillaumot[1,3], T. Ernst[3], P. Masson[2] and T. Skotnicki[1], *[1]ST Microelectronics, [2]IMT Technipôle Château Gombert and [3]LETI, France*

P-3-19
Characterization of RF LDMOS Transistors with Different Layout Structures
H. H. Hu[1], K. M. Chen[2], G. W. Huang[2], C. Y. Chang[1], Y. C. Lu[3], Y. C. Yang[3] and E. Cheng[3], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]United Microelectronics Corp., Taiwan*

P-3-20
Combined Negative Bias Temperature Instability and Hot Carrier Stress Effects in Low Temperature Poly-Si Thin Film Transistors
C. Y. Chen[1], J. W. Lee[2], W. C. Chen[3], H. Y. Lin[3], K. L. Yeh[3], P. H. Lee[1], M. S. Shieh[1], S. D. Wang[1] and T. F. Lei[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]Toppoly Optoelectronics Corp., Taiwan*

P-3-21
N-Type Extended Drain Silicon Controlled Rectifier ESD Protection Device with High Latchup Immunity for High Voltage Operating I/O Application
Y. J. Seo[1] and K. H. Kim[2], *[1]Daebul Univ. and [2]MagnaChip Semiconductor Ltd., Korea*

P-3-23
Empirical Model of Phonon-Limited Electron Mobility for Ultra-Thin Body SOI MOS-FET
T. Yamamura, S. Sato and Y. Omura, *Kansai Univ., Japan*

P-3-24
Re-examination of 1/f Noise in FD-SOI for Practical Usage of Analog Circuits
A. Kumar, Y. Domae, N. Miura, T. Okamura, H. Komatsubara, Y. Kita and J. Ida, *Oki Electric Industry Co. Ltd., Japan*

P-3-25
Ultra-Narrow Silicon Nanowire (~ 3 nm) Gate-All-Around MOSFETs
N. Singh, Y. F. Lim, S. C. Rustagi, L. K. Bera, A. Agarwal, G. Q. Lo, N. Balasub and D. L. Kwong, *Inst. of Microelectronics, Singapore*

P-3-26
Hot-Carrier Reliability Improvement in Submicron High-Voltage DMOS Transistors
J. F. Chen[1], J. R. Lee[1], K. M. Wu[1], Y. K. Su[1], H. C. Wang[1], Y. C. Lin[2] and S. L. Hsu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P4
Advanced Memory Technology
(11 Papers)

P-4-1
Technology of Ferroelectric Thin Film Formation with Large Coercive Field for Future Scaling Down of Ferroelectric Gate FET Memory Device
I. Takahashi, T. Isogai, K. Azumi, M. Hirayama, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P-4-2
FinFET NAND Flash with Nitride/Si Nanocrystal/Nitride Hybrid Trap Layer
J. D. Choe[1], S. H. Lee[1], J. J. Lee[1], E. S. Cho[1], Y. Ahn[1], B. Y. Choi[1], S. K. Sung[1], J. No[1], I. Chung[2], K. Park[1] and D. Park[1], *[1]Samsung Electronics Co. and [2]Sungkyunkwan Univ., Korea*

P-4-3
2-Bit Lanthanum Oxide Trapping Layer Nonvolatile Flash Memory
Y. H. Lin, T. Y. Yang, C. H. Chien and T. F. Lei, *National Chiao Tung Univ., Taiwan*

P-4-4
A Novel NAND Flash Technology with Selective Epitaixial Growth Plug Structure for the Improvement in HV Transistor Breakdown Voltage
S. Jeon, C. Kang, U. Roh, C. Lee, Y. Shin, J. Sim, J. Kim, J. Sel, Y. Jeong, W. Jung, J. Choi and K. Kim, *Samsung Electronic Co., Ltd., Korea*

P-4-6
Lateral and vertical magnetic interaction in a submicron-sized Fe monolayer and a Fe/Au/Fe trilayer ring structure
M. Kohda[1], K. Takagi[1], T. Miyawaki[1], K. Toyoda[1], A. Fujita[1] and J. Nitta[1,2], *[1]Tohoku Univ. and [2]CREST-JST, Japan*

P-4-7
Low Current Reversible Resistive Switching in Bismuth Titanate Deposited by Electron Cyclotron Resonance Sputtering
Y. Jin, H. Shinojima and M. Shimada, *NTT Microsystem Integration Labs., Japan*

P-4-8
Resistive Switching Properties of $SrZrO_3$-based Memory Films
C. C. Lin[1], B. C. Tu[1], C. C. Lin[1], C. H. Lin[2] and T. Y. Tseng[1], *[1]National Chiao Tung Univ. and [2]Winbond Electronics Corp., Taiwan*

P-4-9
Thermal properties of NiO_y resistor practically free from the 'forming' process
K. Kinoshita, C. Yoshida, H. Aso, M. Aoki and Y. Sugiyama, *Fujitsu Labs. Ltd., Japan*

P-4-10
Resistance Switching Characteristics of Binary Metal Oxides
I. S. Park, K. R. Kim and J. Ahn, *Hanyang Univ., Korea*

P-4-11
Capacitorless DRAM Cell with Highly Scalable Surrounding Gate Structure
H. Jeong, Y. S. Lee, S. Kang, I. H. Park, W. Y. Choi, H. Shin, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*

P-4-12
Cost-Effective and Highly Reliable 6F2 Multi-Gigabit DRAM in 60nm Technology Node for Low Power and High Performance Applications
D. Ha, J. H. Kim, T. H. An, S. S. Lee, S. H. Jang, S. H. Kim, M. S. Kang, H. T. Kim, S. H. Lee, M. Y. Sim, W. T. Park, D. H. Han, S. M. Jeon, J. W. Park, S. H. Kim, S. H. Kwon, Y. G. Kim, Y. J. Choi, M. S. Sim, C. H. Cho, M. M. Jeong, T. W. Lee, G. Jin, W. S. Lee and B. I. Ryu, *Samsung Electronics Co., Ltd., Korea*

P5
Advanced Circuits and Systems
(10 Papers)

P-5-1
Hardware Architecture for Pseudo-2D Hidden-Markov-Model-Based Face Recognition System Employing Laplace Distribution Functions
Y. Suzuki and T. Shibata, *Univ. of Tokyo, Japan*

P-5-2
Binocular Range Image Sensor LSI with Fully Parallel Stereo Correlation Processing
T. Yoshida, K. Ono and Y. Arima, *Kyushu Inst. of Technology, Japan*

P-5-3
A Novel Vision Chip for High-Speed Target Tracking
W. Miao, Q. Lin and N. Wu, *Chinese Academy of Sciences, China*

P-5-4
Image-Scan Video Segmentation Architecture and FPGA Implementation
T. Morimoto, H. Adachi, K. Yamaoka, K. Awane, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan*

P-5-5
An Edge Cache Memory Arhcitecture for Early Visual Processing VLSIs
Ö. Özturk and T. Shibata, *Univ. of Tokyo, Japan*

P-5-6
A Hardware-Implementation-Friendly PCNN for Analog Image-Feature-Generation Circuits
J. Chen and T. Shibata, *Univ. of Tokyo, Japan*

P-5-7
A Double-Feedback Voltage-Control-Oscillator
H. M. Chen[1], S. H. Lee[2] and S. L. Jang[2], *[1]Lunghwa Univ. of Science and Technology and [2]National Taiwan Univ. of Science and Technology, Taiwan*

P-5-8
Design of Cartesian Feedback Loop Linearization Chip for UHF band Using 0.6μm Bi-CMOS Technology
M. S. Kang, Y. J. Chong, S. J. You and T. J. Chung, *ETRI, Korea*

P-5-9
Optimization on Layout Structures of LTPS TFTs for On-Panel ESD Protection Design
C. K. Deng[1], M. D. Ker[1], J. Y. Chung[1] and W. T. Sun[2], *[1]National Chiao-Tung Univ. and [2]AU Optronics Corp., Taiwan*

P-5-10
Low Power Spin-Transfer MRAM Writing Scheme with Selective Word Line Bootstrap
T. Sugimura, T. Sakaguchi, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. Japan*

P6
Compound Semiconductor Circuits, Electron Devices and Device Physics
(7 Papers)

P-6-3
Influence of T-gate shape on the device characteristics in SiN-assisted 0.12um AlGaAs/InGaAs PHEMT
H. Ahn, J. W. Lim, H. G. Ji, W. J. Chang, J. K. Mun and H. Kim, *ETRI, Korea*

P-6-4
Auger Effect of Hole Accumulation on Characteristics of InAlAs/InGaAs HEMTs
H. Taguchi, H. Murakami, M. Oura, T. Iida and Y. Takanashi, *Tokyo Univ. of Science, Japan*

P-6-5
Pt Buried Gate E-pHEMT with High $V_{G.ON}$ and Reduced Surface Trap Effects
K. Jang[1], G. Seol[1], S. Kim[1], J. Her[1], J. Lee[2] and K. Seo[1], *[1]Seoul National Univ. and [2]Theleds Co., Ltd., Korea*

P-6-6
Direct Calculation of Source Parasitic Resistance in AlGaAs/GaAs HEMTs
H. Saito, S. Ito and M. Kuzuhara, *Univ. of Fukui, Japan*

P-6-7
Highly-Stable Thermal Characteristics of a High Electron-Mobility Transistor with a Novel $In_{0.3}Ga_{0.7}As_{0.99}N_{0.01}$(Sb) Dilute Channel
K. H. Su[1], W. C. Hsu[1], C. S. Lee[2], Y. S. Lin[3], P. J. Hu[1], R. S. Hsiao[4,5], T. W. Chi[4] and J. Y. Chi[4], *[1]National Cheng-Kung Univ. [2]Feng Chia Univ. [3]National Dong Hwa Univ. [4]National Chiao-Tung Univ. and [5]Industrial Technology Research Inst., Taiwan*

P-6-8
The GaN based HEMT and Schottky diode with filed plate technology for DC/DC converter
W. K. Wang, Y. J. Chang, C. K. Lin, C. H. Lin and Y. J. Chan, *National Central Univ. Taiwan*

P-6-9
A Size-Dependent Equivalent-Circuit Model of High Performance Near-Ballistic-Transport Photodiode
Y. S. Wu, D. M. Lin, F. H. Huang, W. Y. Chiu, J. W. Shi and Y. J. Chan, *Natonal Central Univ., Taiwan*

P7
Photonic Devices and Device Physics
(15 Papers)

P-7-1
Lock-in pixel using a Current-assisted photonic demodulator Implemented in 0.6μm Standard CMOS
W. Van der Tempel, D. Van Nieuwenhove, R. Grootjans and M. Kuijk, *Vrije Univ. Brussel, Belgium*

P-7-3
Development of Flexible Electrochromic Device with Thin Film Configuration
H. Yoshimura, T. Sakaguchi and N. Koshida, *Tokyo Univ. of Agriculture and Technology, Japan*

P-7-4
Effect of Temperature on the Bandwidth and Responsivity of Uni-Traveling-Carrier and Modified Uni-Traveling-Carrier Photodiodes
D. H. Jun, J. H. Jang and J. I. Song, *GIST, Korea*

P-7-5
The Fabrication of the Double Ring Resonators Semiconductor Laser
M. C. Shih[1], S. C. Wang[1], C. W. Liang[1] and M. H. Weng[2], *[1]National Univ. of Kaohsiung and [2]National Nano Device Labs., Taiwan*

P-7-6
AlGaN Ultraviolet Metal-Semiconductor-Metal Photodetectors with Low-Temperature-Grown Cap Layers
S. J. Chang[1], M. H. Wu[1], H. Hung[1], Y. C. Lin[1], H. Kuan[2], R. M. Lin[3] and C. H. Chen[4], *[1]National Cheng Kung Univ., [2]Far East College, [3]Chang Gung Univ. and [4]Cheng Shiu Univ., Taiwan*

P-7-8
Optical constants of beta-$FeSi_2$ film on Si substrate obtained from transmittance and reflectance data and origin of Urbach-tail
H. Kakemoto[1], T. Higuchi[2], H. Shibata[3], S. Wada[1] and T. Tsurumi[1], *[1]Tokyo Tech, [2]Tokyo Univ. of Science and [3]National Inst. of Advanced Industrial Science and Technology, Japan*

P-7-9
Improved Device Characteristocs of InGaAsN Photodetectors Using MIMS Structure
Y. K. Su, W. C. Chen, R. W. Chuang, S. H. Hsu and B. Y. Chen, *National Cheng Kung Univ., Taiwan*

P-7-11
High Reliable Nitride Based LEDs with Internal ESD Protection
C. F. Shen[1], S. J. Chang[1], S. C. Shei[2], C. S. Chang[3], W. S. Chen[1], T. K. Ko[1] and Y. Z. Chiou[4], *[1]National Cheng Kung Univ., [2]National Univ. of Tainan, [3]Epitech Technology Corp. and [4]Southern Taiwan Univ. of Technology, Taiwan*

P-7-12
Design and Characterization of 1 by 128 Linear Arrays of Sensitivity Improved InGaAs/InP NIR Photodetector
Y. C. Jo[1], H. J. Song[1], H. Kim[1] and P. Choi[2], *[1]KETI and [2]Kyungpook National Univ., Korea*

P-7-13
Junction Temperature and Thermal Resistance Measurement in High-Power Light Emitting Diodes Using A Real-Time Diode Forward Voltage Sampling Technique
S. J. Wang[1], T. M. Chen[1,2], K. M. Uang[2], S. L. Chen[1], D. M. Kuo[1], H. Y. Kuo[1], B. W. Liou[2] and S. H. Yang[3], *[1]National Cheng Kung Univ., [2]Wu-Feng Inst. of Technology, and [3]National Kaohsiung Univ., Taiwan*

P-7-14
Enhancement of Carrier Confinement by the Multiquantum Barriers in Blue InGaN/GaN Multiple Quantum Well Light-emitting Diodes
J. C. Wang, H. T. Shen and T. E. Nee, *Chang Gung Univ., Taiwan*

P-7-15
Effect of Residual Stress in Thin Films on the Radiation Spectrum of a Semiconductor Laser
H. Miura, T. Kawauchi, K. Suzuki and M. Sasaki, *Tohoku Univ., Japan*

P-7-16
Photodiode Model for CMOS Image Sensor SPICE Simulation
W. J. Chiang, H. C. Chen and Y. C. King, *National Tsing Hua Univ., Taiwan*

P-7-19
Ultraviolet Random Laser Action of Nano-structured Zinc Oxide
F. I. Lai[1], W. C. Chen[2], S. Y. Kuo[2] and C. P. Cheng[3], *[1]Ching Yun Univ., [2]National Applied Research Labs. and [3]National Taiwan Normal Univ., Taiwan*

P-7-20
Mechanism investigation of chlorine-treated InGaN/GaN light-emitting diodes
P. S. Chen and C. T. Lee, *National Cheng Kung Univ., Taiwan*

P8
Advanced Material Synthesis and Crystal Growth Technology
(18 Papers)

P-8-3
Characteristic comparison of GaN grown on patterned sapphire substrates following growth time
D. H. Kang, J. C. Song, B. Y. Shim, E. A. Ko, D. W. Kim and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-4
Efficient stress relief in GaN heteroepitaxy on Si(111) using various metal buffer
E. A. Ko, D. W. Kim, B. Y. Shim, I. W. Lee and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-5
Electroabsorptive Properties of InGaAs/InAlAs Five-Layer Asymmetric Coupled Quantum Well (FACQW)
T. Arakawa[1], K. Takimoto[1], S. Miyazaki[1], K. Yamaguchi[1], N. Haneji[1], J. H. Noh[2] and K. Tada[3], *[1]Yokohama National Univ., [2]Yokogawa Electric Corp. and [3]Kanazawa Inst. of Technology, Japan*

P-8-6
Photoluminescence characterization of type II $Zn_{0.97}Mn_{0.03}Se/ZnSe_{0.92}Te_{0.08}$ multiple-quantum-well structures
J. J. Shiu[1], W. L. Chen[1], D. Y. Lin[1], C. S. Yang[2] and W. C. Chou[2], *[1]National Changhua Univ. of Education and [2]National Chiao Tung Univ., Taiwan*

P-8-7
Growth of III-V epitaxial material on Si Substrates for high-speed electronic applications
G. L. Luo[1], Y. C. Hsieh[2], T. H. Yang [2] and E. Y. Chang[2], *[1] National Nano Devices Labs. and [2]National Chiao Tung Univ., Taiwan*

P-8-8
Self-assembled GaN nano-column grown on Si (111) substrate using Au+Ga alloy seeding method by MOCVD
B. Y. Shim, E. A. Ko, J. C. Song, D. H. Kang, D. W. Kim, I. H. Lee and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-9
The Influence of Carbon Content on Material and Field Emission Properties of Nanowires Self-synthesized from Sputter-deposited WCx Films
R. M. Ko, S. J. Wang, C. H. Chen, W. C. Tsai, Y. C. Kuo, C. L. Chang and Z. F. Wen, *National Cheng Kung Univ., Taiwan*

P-8-10
A Novel Method for the Preparation of Si Nanowires
R. Lin[1], H. C. Lin[1,2], J. Y. Yang[1], S. W. Shen[1] and C. J. Su[2], *[1]National Nano Device Labs. and [2]National Chiao Tung Univ., Taiwan*

P-8-11
In situ High-Resolution Transmission Electron Microscopy of Deformation of Multi-walled Carbon Nanometer-sized capsules
R. Kato[1], K. Asaka[1], K. Miyazawa[2] and T. Kizuka[1,3], *[1]Univ, of Tsukuba , [2]National Inst for Materials Science and [3]JST, Japan*

P-8-12
Enlargement of Crystal-Grains in Thin Silicon Films Using Continuous-Wave Laser Irradiation
S. Fujii, S. Kuroki, K. Kotani and T. Ito, *Tohoku Univ., Japan*

P-8-13
Kinetic Monte Carlo (KMC) Modeling for Boron Diffusion in Strained Silicon
Y. K. Kim, K. S. Yoon and T. Won, *Inha Univ., Korea*

P-8-14
Ab-initio Study on Energy Barrier for Neutral Indium Migration in a Silicon Substrate
K. S. Yoon, C. O. Hwang and T. Won, *Inha univ., Korea*

P-8-15
Moisture-Barrier Properties of Carbon-coated Silicon Oxide Films
W. R. Chen[1], H. M. Guo[2], T. H. Meen[1], K. H. Wu[2], F. S. Juang[1] and C. J. Huang[3], *[1]National Formosa Univ., [2]Southern Taiwan Univ. of Technology and [3]National Univ. of Kaohsiung, Taiwan*

P-8-16
TiO_2 nanocrystal prepared by ALD system at elevated temperature
C. H. Lin, C. C. Wang, P. J. Tzeng, S. Maikap, H. Y. Lee, L. S. Lee and M. J. Tsai, *Industrial Technology Research Inst., Taiwan*

P-8-17
Synthesis of Au/TiO_2 Core-Shell Nanoparticles from TTIP and Thermal Resistance Effect of TiO_2 Shell
H. Kwon, Y. Lim and Y. Yu, *Chonbuk National Univ., Korea*

P-8-18
Electrical Characteristics and Preparation of $(Ba_{0.5}Sr_{0.5})TiO_3$ Ferroelectric Films by Spray Pyrolysis and Rapid Thermal Annealing
H. S. Koo[1], M. Chen[2], H. K. Ku[3] and T. Kawai[1], *[1]Osaka Univ., [2]Ming Hsin Univ. of Science and Technology and [3]Fortune Inst. of Technology, Japan*

P-8-19
Photoluminescence Characteristics of YAG:Ce Phosphor by Sol-Gel Method
H. W. Choi, S. K. Lee, J. H. Cha[1] and K. H. Kim, *Univ. of Kyungwon, Korea*

P-8-20
Development of Accelerated Large-Scale Electronic Structure Calculation Program for Designing of Rare Earth Phosphors
A. Endou[1], H. Onuma[1], C. Lv[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], H. Takaba[1], M. Kubo[2], C. A. del Carpio[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P9
Physics and Applications of Novel Functional Materials and Devices
(13 Papers)

P-9-1
Effects of Thermal Effusivity in Nanocrystalline Porous Silicon on Long-Term Operation of Thermally Induced Ultrasonic Emission
Y. Watabe[1], Y. Honda[1] and N. Koshida[2], *[1]Matsushita Electric and [2]Tokyo Univ. of Agriculture and Technology, Japan*

P-9-2
Mechanical Properties of Nanometer-sized Fullerene C_{60} Whiskers Studied by In situ High-Resolution Transmission Electron Microscopy
R. Kato[1], K. Asaka[1], K. Miyazawa[2] and T. Kizuka[1,3], *[1]Univ. of Tsukuba, [2]National Inst. for Materials Science and [3]JST, Japan*

P-9-3
Theoretical Study on the Electronic and Structural Properties of p-Type Transparent Conducting Metal Oxides
C. Lv[1], X. Wang[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. del Carpio[1], P. Selvam[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P-9-4
Field Emission Improvement from Pillar Array of Aligned Carbon Nanotubes
C. P. Juan[1,2], K. C. Lin[2], R. L. Lai[2], J. Y. Yang[3] and H. C. Cheng[2], *[1]St. John's Univ., [2]National Chiao Tung Univ. and [3]National Nano Device Lab., Taiwan*

P-9-5
Macroscopic Model of Current-induced Magnetic Switching Effect in Pseudo-spin-valve Structure
M. Ren, L. Zhang, J. Hu, N. Deng and P. Chen, *Tsinghua Univ., China*

P-9-6
Electrical Characterization of Carbon Nanowalls
M. Ura[1], W. Takeuchi[2], Y. Tokuda[2], M. Hiramatsu[3], H. Kano[4] and M. Hori[1], *[1]Nagoya Univ., [2]Aichi Inst. of Technology, [3]Meijo Univ. and [4]NU Eco-Engineering Corp., Japan*

P-9-7
Optical Properties of Size-Controlled Porous Nanostructures Formed on n-InP (001) Substrates by Electrochemical Process
T. Fujino, T. Sato and T. Hashizume, *Hokkaido Univ., Japan*

P-9-8
Development of a Thermal Conductivity Prediction Simulator of Lattice Vibration for Semiconductor, Insulator and Conduction Electron for Metal
H. Tsuboi[1], C. Arunabhirun[1], Z. Zhu[1], C. Lv[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. del Carpio[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P-9-9
Local Characterization of Photovoltage on Polycrystalline Silicon Solar Cells by KFM with Piezo-resistive Cantilever
M. Takihara[1], T. Igarashi[1], T. Ujihara[2] and T. Takahashi[1], *[1]Univ. of Tokyo and [2]Nagoya Univ., Japan*

P-9-10
A Spin Drag Effect in Temperature Dependence of Spin-Polarized Electron Mobilities
Y. Takahashi[1], Y. Sato[2], F. Hirose[1] and H. Kawaguchi[2,3], *[1]Yamagata Univ., [2]CREST and [3]Nara Inst. of Science and Technology, Japan*

P-9-11
Hybrid simulation of the RF-SET and its charge sensitivity analysis
M. Manoharan[1], H. Mizuta[1,2] and S. Oda[1,2], *[1]Tokyo Tech and [2]SORST-JST, Japan*

P-9-12
Electrical Characteristics and Preparation of Nanostructured $Pb(Zr_{0.5}Ti_{0.5})O_3$ Ferroelectric Films by Spray Pyrolysis
M. Chen[1], H. S. Koo[2], Y. Hotta[2] and T. Kawai[2], *[1]Ming-Hsin Univ. of Science and Technology and [2]Osaka Univ., Taiwan*

P-9-13
A transmission-type radio-frequency single-electron transistor (RF-SET) with an in-plane-gate SET (IPG-SET)
Y. S. Yu[1], E. S. Kim[1], C. H. Lee[1], S. H. Kim[1], S. H. Son[2,3], S. W. Hwang[2,3] and D. Ahn[3], *[1]Hankyong National Univ., [2]Korea Univ. and [3]Univ. of Seoul, Korea*

P10
Organic Materials Science, Device Physics, and Applications
(17 Papers)

P-10-2
Fabrication of color-stable organic light-emitting devices by utilizing incomplete energy transform
C. S. Huang, Y. K. Su and B. T. Wu, *National Cheng Kung Univ., Taiwan*

P-10-3
Effect of $SnDP(HPB)_2$ as Hole Blocking Layer in OLED
D. E. Kim[1], B. S. Kim[1], W. S. Kim[2], O. K. Kwon[1], B. J. Lee[2] and Y. S. Kwon[1], *[1]Dong-A Univ. and [2]Inje Univ., Korea*

P-10-4
Theoretical Study on the Photophyscial Properties of an Efficient Sensitizer for Nanocrystalline TiO_2-Based Solar Cells
A. Govindasamy[1], C. Lv[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], C. A. Del Carpio [1], M. Kubo[1,2] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]JST-PRESTO, Japan*

P-10-5
Dye Sensitization Effect on Photocurrent Generation of Porphyrin-Polythiophene Composite Films
K. Sugawa[1], K. Kakutani[1], T. Akiyama[1], S. Yamada[1], K. Takechi[2], T. Shiga[2], M. Motohiro[2], H. Nakayama[3] and K. Kohama[3], *[1]Kyushu Univ., [2]Toyota Central R&D Labs., Inc. and [3]Toyota Motor Corp., Japan*

P-10-7
A Low Voltage Memory (~2V) Based on Polystyrene for Printable Electronics
C. C. Chang, H. T. Lin, Z. Pei, W. M. Lou, C. A. Jong and Y. J. Chan, *ITRI, Taiwan*

P-10-8
The Measurement of Electrical Conduction of Self-Assembled Viologen Derivatives Using Scanning Tunneling Microscopy
N. S. Lee[1], H. K. Shin[2], D. J. Qian[3] and Y. S. Kwon[1], *[1]Dong-A Univ., [2]Pohang Univ. of Science and Technology and [3]Fudan Univ., Korea*

P-10-9
Effect of Oxygen Contents on the Property of Hydrophobic Thin Films Deposited on Flexible Substrates Using Plasma-enhanced CVD
D. S. Liu[1], C. Y. Wu[1], B. W. Huang[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*

P-10-10
Synchrotron Radiation Studies of the Orientation of Thin Silicon Phthalocyanine Dichloride Film on HOPG Substrate
D. Juzhi[1,2], T. Sekiguchi[1], Y. Baba[1] and N. Hirao[1], *[1]Japan Atomic Energy Agency and [2]China Univ. of Tech., Japan*

P-10-11
Reduction of Electrical Damage due to Au/Pentacene Contact Formation by Introducing Ar Gas during Au Evaporation
T. Sawabe[1], K. Okamura[1], T. Miyamoto[2], M. Nakamura[1] and K. Kudo[1], *[1]Chiba Univ. and [2]Toray Research Center, Inc, Japan*

P-10-13
Fabrication of Nano-gate Structure Organic Static Induction Transistor using Electron Beam Lithography
M. Fukuda, H. Yamaguchi, M. Iizuka and K. Kudo, *Chiba Univ., Japan*

P-10-14
A Simple Method for Extraction of Contact Resistance in Organic Thin Film Transistor
B. C. Jung and C. K. Song, *Dong-A Univ., Korea*

P-10-15
Analysis of pentacene FET characteristics using a Maxwell-Wagner model
R. Tamura, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech, Japan*

P-10-16
Fabrication and Ethanol Vapor Treatment of Magnesium Phthalocyanine Field Effect Transistor
K. Shinbo, T. Akazawa, H. Ikarashi, Y. Ohdaira, K. Kato and F. Kaneko, *Niigata Univ., Japan*

P-10-17
Full-swing Pentacene Organic Inverter with Long-channel Driver and Short-channel Load
C. A. Lee, D. W. Park, K. D. Jung, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*

P-10-18
Physical Properties and Fabricating Technology of Novel Type Resist for Color Filter in TFT LCD
P. C. Pan, H. C. Wu, H. S. Koo and T. Kawai, *Osaka Univ., Japan*

P-10-19
Fabrication of vertical organic light emitting transistor using thin-film ZnO
H. Yamauchi, M. Iizuka and K. Kudo, *Chiba Univ., Japan*

P-10-20
Significantly Enhancing Luminance of Organic Light-Emitting Diodes (OLEDs) with Doping Iodine and Nitrogen Treatment
S. F. Chen, Y. K. Fang, S. C. Hou, F. S. Lin, C. Y. Lin, S. H. Chang and T. H. Chou, *National Cheng Kung Univ., Taiwan*

P11 Micro/Nano Electromechanical and Bio-Systems (Devices)
(8 Papers)

P-11-1
High Performance RF Passive Devices on Plastic Substrates for RFIC Application
B. F. Hung, C. C. Chen, H. L. Kao and A. Chin, *National Chiao Tung Univ., Taiwan*

P-11-2
Development of a Functional Chromosome Nano-Dissection System Using Porous Anodic Alumina Pattern Chip and AFM Cantilever
D. K. Kim[1], M. Saito[1], Y. S. Kwon[2] and E. Tamiya[1], *[1]JAIST and [2]Dong-A Univ., Japan*

P-11-3
Effect of Chemical Modification of the Substrate Surface on Lipid Bilayer Formation
T. Isono, H. Tanaka and T. Ogino, *Yokohama National Univ., Japan*

P-11-4
Biosensing with CNx multi-wall carbon nanotubes
H. J. Burch, S. A. Contera, C. N. Toldeo, M. R. Planque, N. Grobert, K. Voitchovsky and J. F. Ryan, *Univ. of Oxford, UK*

P-11-5
Novel process techniques for ISFET/REFET micro chip based on common Si_3N_4 sensing membrane
C. S. Lai, C. E. Lue, C. M. Yang and J. H. Jao, *Chang Gung Univ., Taiwan*

P-11-6
Modulation of the Density of Assembled Gold Nanoparticles and Local Plasmon Coupling Effect on SPR Spectrum Response
X. Li, K. Tamada and M. Hara, *Tokyo Tech, Japan*

P-11-7
Electric Properties in Biofilms Studied by Resonant Auger Electron Spectroscopy
Y. Baba[1], T. Sekiguchi[1], I. Shimoyama[1], K. G. Nath[2] and N. Hirao[1], *[1]Japan Atomic Energy Agency and [2]Univ. of Quebec, Japan*

P-11-8
Micro molding of three-dimensional metal structure by non-electro plating of photopolymerized resin
T. Yoshimura, S. Maruo and K. Mukai, *Yokohama National Univ., Japan*