## Room 411/412 (A)

**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**

A-3: MEMS and NEMS : Fabrication
(9:00-10:30)
Chairs: T. Nishimoto (Shimadzu)
T. Ono (Tohoku Univ.)

**9:00 A-3-1 (Invited)**
New Approach to Experimental Nanomechanics Using MEMS Technology
Y. Isono, *Ritsumeikan Univ., Japan*

## Room 413 (B)

**Area 7: Photonic Devices and Device Physics**

B-3: LEDs and Lasers
(9:00-10:30)
Chairs: M. Ezaki (Toshiba)
M. Sugawara (Fujitsu Labs.)

**9:00 B-3-1**
High Brightness and Crack-free InGaN/GaN Light Emitting Diode With AlGaN Buffer Layer On Si (111)
Y. P. Hsu[1], S. J. Chang[1], Y. K. Su[1], W. S. Chen[1], J. K. Sheu[1], J. Y. Chu[1] and C. T. Kuo[2], *[1]National Cheng Kung Univ. and [2]Epitech Technology Corp., Taiwan*

## Room 414/415 (C)

**Area 5: Advanced Circuits and Systems**

C-3: Toward Next Generation Systems
(9:00-9:40)
Chairs: H. Yamauchi (Sanyo Electric)
H. Kobayashi (Gunma Univ.)

C-3: Toward Next Generation Systems
(9:40-10:20)
Chairs: K. Masu (Tokyo Tech)
H. Yamauchi (Sanyo Electric)

**9:00 C-3-1**
Large-Scale Quantum Computing Emulation Based on Unitary Macro-Operations
Y. Goto and M. Fujishima, *Univ. of Tokyo, Japan*

**9:20 C-3-2**
Random Number Generator with 0.3MHz Generation Rate using Non-Stoichiometric $Si_xN$ MOSFET
M. Matsumoto, R. Ohba, S. Yasuda, K. Uchida, T. Tanamoto and S. Fujita, *Toshiba Corp., Japan*

## Room 416/417 (D)

**Area 10: Organic Materials Science, Device Physics, and Applications**

D-3: Organic Materials and Device Physics I
(9:00-10:30)
Chairs: K. Kato (Niigata Univ.)
K. Kudo (Chiba Univ.)

**9:00 D-3-1 (Invited)**
Organic Single Crystal Transistors and Interface Control
Y. Iwasa, *Tohoku Univ., Japan*

## Room 418 (E)

**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**

E-3: Sensors and Interface Physics
(9:00-10:00)
Chairs: T. Hashizume (Hokkaido Univ.)
K. Kumakura (NTT)

**9:00 E-3-1**
Performance of open-gate AlGaN/GaN HFET in various kinds of liquids
T. Kokawa, T. Sato and T. Hashizume, *Hokkaido Univ., Japan*



## Room 419 (F)

**Area 3: CMOS Devices/Device Physics**

F-3: Quasi-Ballistic Transport
(9:00-10:40)
Chairs: Y. Kamakura (Osaka Univ.)
K. Kurimoto (Matsushita Electric)

**9:00 F-3-1**
Ohm's Law from a Transmission Viewpoint
K. Natori[1,2] and T. Shimizu[1], *[1]Univ. of Tsukuba and [2]CREST-JST, Japan*

**9:20 F-3-2**
A Picture of Quasi-Ballistic Transport in Nanoscale MOSFETs
H. Tsuchiya, K. Fujii, T. Mori and T. Miyoshi, *Kobe Univ., Japan*

## Room 501 (G)

## Room 502 (H)

## Room 511/512 (I)

## Small Auditorium (J)

**Area 1: Advanced Gate Stack / Si Processing Science**

J-3: Characterization of Gate Stack
(9:10-10:40)
Chairs: S. Miyazaki (Hiroshima Univ.)
A. Sakai (Nagoya Univ.)

**9:10 J-3-1 (Invited)**
High-resolution RBS Analysis of Si-dielectrics Interfaces
K. Kimura[1], Z. Ming[1], K. Nakajima[1], M. Suzuki[1], M. Uematsu[2], K. Torii[3], S. Kamiyama[3], Y. Nara[3], H. Watanabe[4], K. Shiraishi[5], T. Chikyow[6] and K. Yamada[7], *[1]Kyoto Univ., [2]NTT Corp., [3]Selete, [4]Osaka Univ., [5]Univ. of Tsukuba, [6]NIMS and [7]Waseda Univ., Japan*

| Room 411/412 (A) | Room 413 (B) | Room 414/415 (C) | Room 416/417 (D) | Room 418 (E) |
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| | **9:30 B-3-3**<br>Fabrication of High Light-Extraction Efficiency LED Using Nanostructures by UV Nanoimprint Lithography and Electrodeposition<br>H. Ono[1], Y. Ono[2], K. Kasahara[2], J. Mizuno[1] and S. Shoji[1], *[1]Waseda Univ. and [2]Sumitomo Chemical Co., Ltd, Japan* | **9:40 C-3-3**<br>Nearest-Euclidean-Distance Search Associative Memory Architecture with Fully Parallel Mixed Digital-Analog Match Circuitry<br>M. A. Abedin, Y. Tanaka, A. Ahmadi, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan* | **9:30 D-3-2**<br>Decay process of a large surface potential of as-deposited Alq3 films<br>N. Kajimoto, T. Manaka and M. Iwamoto, *Tokyo Tech, Japan* | **9:30 E-3-3**<br>Modulation of Resistivity of Two-Dimensional Electron Gas in AlGaN/GaN Structure<br>Y. C. Chang[1], J. K. Sheu[1] and Y. L. Li[2], *[1]National Cheng Kung Univ. and [2]National Taiwan Univ., Taiwan* |
| **9:45 A-3-3**<br>Ultra high aspect ratio sub-micron silicon micromachining by double-passivation deep reactive ion etching<br>R. Nagarajan and B. R. Murthy, *Inst. of Microelectronics, Singapore* | **9:45 B-3-4**<br>Light Emitting Diode Array Prepared by Epitaxial Film Bonding<br>T. Suzuki, H. Fujiwara, M. Mutoh, T. Sagimori, H. Kurokawa, T. Igari, T. Kaneto, H. Furuta, I. Abiko, M. Sakuta and M. Ogihara, *Oki Digital Imaging Corp., Japan* | | **9:45 D-3-3**<br>Electronic structure of bathocuproine on metal studied by ultraviolet photoemission spectroscopy<br>S. Toyoshima[1,2], K. Kuwabara[1], T. Sakurai[1], T. Taima[2], K. Saito[2], H. Kato[3] and K. Akimoto[1], *[1]Tsukuba Univ., [2]AIST and [3]Hirosaki Univ., Japan* | **9:45 E-3-4**<br>Electrical and Optical Properties of an n-Channel GaN Schottky Barrier MISFET<br>H. B. Lee, H. I. Cho, H. S. An, J. H. Lee and S. H. Hahm, *Kyungpook National Univ., Korea* |
| **10:00 A-3-4**<br>Room Temperature Vacuum Sealing with Au Thin Films Using Ar Beam Surface Activation<br>H. Okada, T. Itoh and T. Suga, *Univ. of Tokyo, Japan* | **10:00 B-3-5**<br>High Performances of 650 nm Resonant Cavity Light Emitting Diodes for Plastic Optical Fiber Applications<br>Y. C. Lee[1], C. E. Lee[1], S. W. Chiou[2], H. C. Kuo[1], T. C. Lu[1] and S. C. Wang[1], *[1]National Chiao Tung Univ. and [2]United Epitaxy Co., Taiwan* | **10:00 C-3-4**<br>Scaling Trends and Mitigation Techniques for Soft Errors in Flip-Flops<br>T. Uemura[1], Y. Tosaka[1], S. Satoh[1], K. Takahisa[2] and K. Hatanaka[2], *[1]Fujitsu Labs. Ltd. and [2]Osaka Univ., Japan* | **10:00 D-3-4**<br>Spin injection from magnetic electrodes to organic semiconductors studied by transport and spectroscopic measurements<br>T. Shimada, *Univ. of Tokyo, Japan* |



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| **9:40 F-3-3**<br>Intrinsic Delay of Nanoscale MOSFETs under Ballistic Transport<br>A. Tsuda, T. Kunikiyo, T. Okagaki, T. Watanabe, M. Tanizawa, K. Ishikawa, H. Nunogami and A. Uchida, *Renesas Technology Corp., Japan* | | | | **9:40 J-3-2**<br>Real-Time Observation of Initial Thermal Oxidation on Si(110)-16x2 Surfaces by O1s Photoemission Spectroscopy Using Synchrotron Radiation<br>M. Suemitsu[1], A. Kato[1], H. Togashi[1], A. Konno[1], Y. Yamamoto[1], Y. Teraoka[2], A. Yoshigoe[2] and Y. Narita[3], *[1]Tohoku Univ., [2]Japan Atomic Energy Agency and [3]Kyushu Inst. of Technology, Japan* |
| **10:00 F-3-4**<br>The effect of side-traps on ballistic transistor in Kondo regime<br>T. Tanamoto, K. Uchida and S. Fujita, *Toshiba Corp., Japan* | | | | **10:00 J-3-3**<br>Nonlinear Al Concentration Dependence of the HfAlOx/Si Conduction Band Offset Studied by Internal Photoemission Spectroscopy<br>T. Horikawa[1], A. Ogawa[2], K. Iwamoto[2], K. Okada[2], H. Ota[1], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan* |

| Room 411/412 (A) | Room 413 (B) | Room 414/415 (C) | Room 416/417 (D) | Room 418 (E) |
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| **10:15 A-3-5**<br>MEMS Wafer Level Packaging by Using Surface Activated Bonding<br>Y. Takegawa, T. Baba, T. Okudo and Y. Suzuki, *Matsushita Electric Works, Ltd., Japan* | **10:15 B-3-6**<br>InP-Based Quantum Cascade Lateral Grating Distributed Feedback Lasers<br>K. Kennedy, D. G. Revin, A. B. Krysa, K. M. Groom, L. R. Wilson, J. W. Cockburn and R. Hogg, *Univ. of Sheffield, UK* | | | |

**Break**

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|---|---|---|---|---|
| **Short Presentation P11 and P8 (10:45-12:15) Chair: H. Tabata (Osaka Univ.)** | **Short Presentation P7 and P4 (10:45-12:15) Chair: M. Sugawara (Fujitsu Labs.)** | **Short Presentation P5 and P2 (10:45-12:15) Chair: H. Kobayashi (Gunma Univ.)** | **Area 10: Organic Materials Science, Device Physics, and Applications**<br>D-4: Organic Materials and Device Physics II (10:45-11:30)<br>Chairs: M. Iwamoto (Tokyo Tech)<br>K. Kato (Niigata Univ.) | **Short Presentation P6 and P9 (10:45-12:15) Chair: M. Kuzuhara (Univ. of Fukui)** |

**10:45 D-4-1**
Self Assembled Viologen Modified Electrode as Mediator of Glucose Sensor
D. Y. Lee[1], A. K. M. Kafi[1], S. H. Park[1], D. J. Qian[2] and S. Kwon[1], *[1]Dong-A Univ. and [2]Fudan Univ., Korea*

**11:00 D-4-2**
Orientation and Electrical Conduction of Poly(3-hexylethiophene) Thin Film Prepared by Using a Different Solution-process Method
S. Mototani, S. Ochiai, S. Tanabe, A. Ohashi, Y. Uchida, K. Kojima and T. Mizutani, *Aichi Inst. of Tech., Japan*



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| | | | | **10:20 J-3-4**<br>Electric characteristics of $Si_3N_4$ films formed by directly radical nitridation on Si (110) and Si (100) surfaces<br>M. Higuchi[1], T. Aratani[1], T. Hamada[1], A. Teramoto[1], T. Hattori[1,2], S. Sugawa[1], T. Ohmi[1], S. Shinagawa[2], H. Nohira[2], E. Ikenaga[3] and K. Kobayashi[3], *[1]Tohoku Univ., [2]Musashi Inst. of Technology and [3]JASRI/SPring8, Japan* |

**Break**

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| **Short Presentation P3 (10:45-12:15) Chair: H. Oda (Renesas)** | | | | **Short Presentation P1 (10:45-12:15) Chair: Y. Nara (Selete)** |

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| | | | **11:15 D-4-3**<br>Theoretical Investigation of Electrical and Electronic Properties of Carbon Materials<br>A. Chutia[1], Z. Zhu[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], M. Kubo[1,2], C. A. Del Carpio[1], P. Selvam[1] and A. Miyamoto[1],<br>*[1]Tohoku Univ. and [2]PRESTO, Japan* | |
| | | | **Short Presentation P10 (11:30-12:30)**<br>**Chair: K. Kubo (Chiba Univ.)** | |
| **Lunch** | | | | |
| **13:00-15:00 Poster Session (Room 501, 502, 511/512, 5F)** | | | | |
| **Area 8: Advanced Material Synthesis and Crystal Growth Technology**<br>**Area 9: Physics and Applications of Novel Functional Materials and Devices** | **Area 7: Photonic Devices and Device Physics** | **Area 4: Advanced Memory Technology** | **Area 2: Characterization and Materials Engineering for Interconnect Integration** | **Area 1: Advanced Gate Stack/Si Processing Science** |
| A-5: Nanowires and Nanotubes I<br>(15:15-16:15)<br>Chairs: T. Fukui (Hokkaido Univ.)<br>Y. L. Foo (Inst. of Materials Research & Engineering) | B-5: Quantum-dot Lasers<br>(15:15-16:30)<br>Chairs: M. Sugawara (Fujitsu Labs.)<br>K. Komori (AIST) | C-5: ReRAM<br>(15:15-16:25)<br>Chairs: Y. Ohji (Renesas)<br>I. Asano (Elpida) | D-5: Emerging Interconnect<br>(15:15-16:15)<br>Chairs: T. Yoda (Toshiba)<br>T. Tatsumi (SONY) | E-5: Junction I<br>(15:15-16:35)<br>Chairs: B. Mizuno (UJT Inc.)<br>H. Hwang (Gwangju Inst. of Sci. & Tech.) |
| **15:15 A-5-1 (Invited)**<br>ZnO Nanorods for Electronic Nanodevice Applications<br>G. C. Yi, W. I. Park, J. Yoo, H. J. Kim and C. H. Lee, *POSTECH, Korea* | **15:15 B-5-1 (Invited)**<br>Self-Assembled Quantum Dots: Engineered Gain Medium<br>S. Oktyabrsky, M. Yakimov, J. Van Eisden and V. Tokranov, *State Univ. of New York at Albany, USA* | **15:15 C-5-1 (Invited)**<br>Mechanisms of Resistance Switching Memory Effect in Oxides<br>M. Kawasaki, *Tohoku Univ., Japan* | **15:15 D-5-1 (Invited)**<br>Si Nano-photonics for LSI on-chip Optical Interconnection<br>K. Nishi, J. Fujikata, H. Yamada, T. Ishi, M. Nakada, K. Nose, M. Mizuno, M. Fukaishi, Y. Urino and K. Ohashi, *NEC Corp., Japan* | **15:15 E-5-1**<br>Atmospheric In-situ Arsenic-Doped SiGe Selective Epitaxial Growth for Raised Extension NMOSFET<br>T. Ikuta, Y. Miyanami, S. Fujita, H. Iwamoto and S. Kadomura, *Sony Corp., Japan* |



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| **Lunch** | | | | |
| **13:00-15:00 Poster Session (Room 501, 502, 511/512, 5F)** | | | | |
| **Area 3: CMOS Devices/Device Physics** | | | | **Area 1: Advanced Gate Stack/Si Processing Science** |
| F-5: Device Fluctuation Analysis<br>(15:15-16:35)<br>Chairs: Y. Kamakura (Osaka Univ.)<br>J. C. S. Woo (UCLA) | | | | J-5: High-k Dielectrics I<br>(15:15-16:35)<br>Chairs: Y. Tsunashima (Toshiba)<br>T. Nabatame (ASET) |
| **15:15 F-5-1 (Invited)**<br>Simulation of Atomic Scale Effects and Fluctuations in Nano-Scale CMOS<br>A. Asenov, A. R. Brown, G. Roy, C. Alexander and A. Martinez, *Univ. of Glasgow, UK* | | | | **15:15 J-5-1**<br>Plasma Nitridation of $HfO_2$ Enabling a 0.9 nm EOT with High Mobility for a Gate First MOSFET<br>P. D. Kirsch[1], M. Quevedo-lopez[2], S. A. Krishnan[3], C. Krug[3], F. S. Aguirre[4], R. M. Wallace[4], B. H. Lee[1] and R. Jammy[1], *[1]IBM, [2]Texas Instruments, [3]SEMATECH and [4]UT-Dallas, Usa* |

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| **15:45 A-5-2**<br>Arrangement of Catalyst Islands at Surface Atomic Steps toward Position Control of Nanowires<br>H. Hibino, K. Tateno and Y. Watanabe, *NTT Corp., Japan* | **15:45 B-5-2 (Invited)**<br>Fabrication of Sb-based QDs for Long-wavelength VCSELs<br>N.Yamamoto[1], K. Akahane[1], S. Gozu[1], A. Ueta[1], N. Ohtani[2] and M. Tsuchiya[1], *[1]NICT and [2]Doshisha Univ., Japan* | **15:45 C-5-2**<br>Low Power Operation of Non-volatile Hafnium Oxide Resistive Memory<br>H. Y. Lee[1], P. S. Chen[2], C. C. Wang[1], S. Maikap[1], P. J. Tzeng[1], C. H. Lin[1], L. S. Lee[1] and M. J. Tsai[1], *[1]Industrial Technology Research Inst. and [2]Ming Shin Univ. of Science & Technology, Taiwan* | **15:45 D-5-2 (Invited)**<br>3D System Integration: Enabling Technologies and Applications<br>P. Ramm, *Fraunhofer IZM, Germany* | **15:35 E-5-2**<br>Self-Heating Induced Germanium Outdiffusion and Non-Local Channel Degradation in the Strained-Si/SiGe N-MOSFET subjected to Channel Hot-Electron Stress<br>T. W. H. Phua[1], D. S. Ang[2], C. H. Tung[3] and C. H. Ling[1], *[1]National Univ. of Singapore, [2]Nanyang Technological Univ. and [3]Inst. of Microelectronics, Singapore* |
| **16:00 A-5-3**<br>Exciton and biexciton emissions from single GaAs quantum dots in (Al,Ga)As nanowires<br>H. Sanada, H. Gotoh, K. Tateno and H. Nakano, *NTT Corp., Japan* | | **16:05 C-5-3**<br>SiOx/ß-SiC/Si MIS Resistive Memory Devices Formed by One- and Two-Stage Oxidation of ß-SiC<br>M. Shouji, T. Nagashima and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan* | | **15:55 E-5-3**<br>Ni(alloy)-germanosilicide contact technology for Si1-xGex (x=0.20-0.5) junctions<br>K. L. Pey[1,2], L. Jin[1], W. K. Choi[1,3], H. P. Yu[1], D. A. Antoniadis[1,4], E. A. Fitzgerald[1,4], D. Z. Chi[5] and D. M. Isaacson[1,4], *[1]SMA, [2]Nanyang Technological Univ., [3]National Univ. of Singapore, [4]MIT and [5]IMRE, Singapore*<br><br>**16:15 E-5-4**<br>Impacts of Si Crystal Orientation on NiSi Silicided Junction Leakage Induced by Anisotropic Ni Migration<br>M. Tsuchiaki[1] and A. Nishiyama[1], *Toshiba Corp., Japan* |
| **Break** | | | | |



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| **15:45 F-5-2**<br>Improvement of Device Characteristics Variation by using a Body-Bias Controlling Technology Based on a Hybrid Trench Isolated SOI<br>Y. Maki, Y. Hirano, M. Tsujiuchi, T. Iwamatsu, O. Ozawa, T. Ipposhi and Y. Inoue, *Renesas Technology Corp., Japan* | | | | **15:35 J-5-2**<br>Excellent Leakage Current of Crystallized Silicon-Doped $HfO_2$ Films Down to Sub-nm EOT<br>K. Tomida, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan* |
| **16:05 F-5-3**<br>3D Statistical Simulation of Gate Leakage Fluctuations Due to Combined Interface Roughness and Random Dopants<br>S. Markov[1], A. R. Brown[1], B. Cheng[1], G. Roy[1], S. Roy[1] and A. Asenov[1], *Univ. of Glasgow, UK* | | | | **15:55 J-5-3**<br>Spatial Fluctuation of Electrical properties in Hf-Silicate Film Observed with Scanning Capacitance Microscopy<br>Y. Naitou[1,4], A. Ando[1], H. Ogiso[2], S. Kamiyama[3], Y. Nara[3], H. Watanabe[4] and K. Yasutake[4], *[1]AIST NeRI, [2]AIST-Advanced Manufacturing Research Inst., [3]Selete and [4]Osaka Univ., Japan*<br><br>**16:15 J-5-4**<br>Mechanism of Threshold Voltage Reduction and Hole Mobility Enhancement in pMOSFETs Employing Sub-1nm EOT HfSiON by Use of Substrate Fluorine Ion Implantation<br>S. Inumiya[1], A. Uedono[2], S. Miyazaki[3], S. Ohtsuka[1], T. Matsuki[1], T. Wada[1], T. Aoyama[1], K. Yamada[4] and Y. Nara[1], *[1]Selete, [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Waseda Univ., Japan* |
| **Break** | | | | |

## Room 411/412 (A)

**Area 8: Advanced Material Synthesis and Crystal Growth Technology**

**Area 9: Physics and Applications of Novel Functional Materials and Devices**

A-6: Nanowires and Nanotubes II
(16:30-18:00)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Awano (Fujitsu Labs.)

**16:30 A-6-1 (Invited)**
Probing Carbon Nanostructures Growth Mechanism Using an in-situ UHVTEM
Y. L. Foo, *Inst. of Materials Research and Engineering, Singapore*

**17:00 A-6-2**
High-Sensitive and Label-Free Detection of Biomolecules Using Single-Walled Carbon Nanotube Modified Microelectrodes
J. Okuno[1], K. Maehashi[1], K. Matsumoto[1], K. Kerman[2], Y. Takamura[2] and E. Tamiya[2], *[1]Osaka Univ. and [2]JAIST, Japan*

## Room 413 (B)

**Area 7: Photonic Devices and Device Physics**

B-6: Quantum Optical Devices
(16:45-18:00)
Chairs: L. Lester (Univ. of New Mexico)
T. Usuki (Univ. of Tokyo)

**16:45 B-6-1 (Invited)**
Single-photon Generator for Telecom Applications
T. Usuki[1], K. Takemoto[2], S. Hirose[2], M. Takatsu[2], T. Miyazawa[1], Y. Sakuma[3], N. Yokoyama[2] and Y. Arakawa[1], *[1]Univ. of Tokyo, [2]Fujitsu Labs. and [3]NIMS, Japan*

## Room 414/415 (C)

**Area 4: Advanced Memory Technology**

C-6: Flash Memory I
(16:45-17:55)
Chairs: Y. Yamauchi (Sharp)
Y. Shimamoto (Hitachi Ltd.)

**16:45 C-6-1 (Invited)**
Future Outlook of Floating Gate Flash Memory
F. Arai, *Toshiba Corp., Japan*

## Room 416/417 (D)

**Area 2: Characterization and Materials Engineering for Interconnect Integration**

D-6: Assembly and Packaging
(16:25-17:45)
Chairs: S. H. Brongersma (IMEC)
D. Y. Yoon (Seoul National Univ.)

**16:25 D-6-1**
Real-time observation of Hydrogen Plasma Reflow Process with Lead-free Solder Pastes
S. Nishi[1], E. Higurashi[1], T. Suga[1], T. Hagihara[2], T. Takeuchi[2], Y. Shingai[2], S. Yamagata[3], R. Katoh[3] and K. Arase[3], *[1]Univ. of Tokyo, [2]Shinko Seiki Co., Ltd. and [3]Senju Metal Industry Co., Ltd., Japan*

**16:45 D-6-2**
The Reliability Characteristics of Wafer-Level Chip-Scale Package under Various Current Stressing
H. Y. Kung[1,3], S. H. Chen[2], Y. S. Lai[3], E. Jahja[1] and W. K. Yeh[1], *[1]National Univ. of KaoHsiung, [2]Tung Fang Inst. of Technology and [3]Advanced Semiconductor Engineering, Inc., Taiwan*

## Room 418 (E)

**Area 1: Advanced Gate Stack/Si Processing Science**

E-6: Junction II
(16:45-17:45)
Chairs: B. Mizuno (UJT Inc.)
H. Fukutome (Fujitsu Labs.)

**16:45 E-6-1**
Reduction in PN Junction Leakage for Ni-silicided Small Si Islands by Using Thermal Conduction Heating with Stacked Hot Plates
H. Itokawa[1], H. Akutsu[1], A. Nomachi[1], H. Oono[2], T. Iinuma[1] and K. Suguro[1], *[1]Semiconductor Company, Toshiba Corp. and [2]Toshiba Corp., Japan*

**17:05 E-6-2**
A Novel Laser Annealing Process for Advanced CMOS with Suppressed Gate Depletion and Ultra-shallow Junctions
A. Shima[1], T. Mine[1], L. Feng[2], X. Wang[2], Y. Wang[2] and K. Torii[1], *[1]Hitachi, Ltd. and [2]Ultratech Inc., Japan*



## Room 419 (F)

**Area 3: CMOS Devices/Device Physics**

F-6: Device Reliability and Characterization
(16:45-18:05)
Chairs: D. Hisamoto (Hitachi Ltd.)
Y. Momiyama (Fujitsu)

**16:45 F-6-1**
NBTI Improvement under Highly Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS and Beyond
C. T. Huang, L. S. Jeng, W. H. Hung, S. F. Ting, K. H. Lee, M. L. Tseng, O. Cheng and C. W. Liang, *United Microelectronics Corp., Taiwan*

**17:05 F-6-2**
NBT Stress Induced Anomalous Drain Current Instability in HfSiON pMOSFETs Arising from Bipolar Charge Trapping
C. J. Tang[1], H. C. Ma[1], C. T. Chan[1], T. Wang[1] and H. C. Wang[2], *[1]National Chiao Tung Univ. and [2]TSMC, Taiwan*

## Room 501 (G)

## Room 502 (H)

## Room 511/512 (I)

**Area 5: Advanced Circuits and Systems**

I-6: Analog Circuit Techniques
(16:45-18:05)
Chairs: H. Kobayashi (Gunma Univ.)
T. Komuro (Agilent Technologies International Japan)

**16:45 I-6-1 (Invited)**
A Practical, Systematic, Simple Method to Evaluate Speed/Bandwidth Potential of CMOS Processes for Analog Design and Related Practical Considerations
K. Hadidi, *Urmia Univ., Iran*

## Small Auditorium (J)

**Area 1: Advanced Gate Stack / Si Processing Science**

J-6: Interface Properties of Ge
(16:45-17:45)
Chairs: K. Shiraishi (Univ. of Tsukuba)
A. Sakai (Nagoya Univ.)

**16:45 J-6-1**
Quantitative Evaluation of Interface Trap Density in Ge-MIS Interfaces
N. Taoka[1], K. Ikeda[2], Y. Yamashita[2], N. Sugiyama[2] and S. Takagi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*

**17:05 J-6-2**
Fabrication of $SiO_2$/Ge MIS structures by plasma oxidation of ultrathin Si films grown on Ge
H. Kumagai[1], M. Shichijo[1], H. Ishikawa[1], T. Hoshii[1], S. Sugahara[1], Y. Uchida[2] and S. Takagi[1], *[1]Univ. of Tokyo and [2]Teikyo Univ. of Science and Technology, Japan*

| Room 411/412 (A) | Room 413 (B) | Room 414/415 (C) | Room 416/417 (D) | Room 418 (E) |
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| **17:15 A-6-3**<br>Electric properties of single-walled carbon nanotube film field effect transistors with various work function electrodes: a comparison between pristine and potassium-encapsulated nanotubes<br>H. Maki[1], S. Suzuki[2], T. Sato[1] and K. Ishibashi[3], *[1]Keio Univ., [2]NTT Corp. and [3]RIKEN, Japan* | **17:15 B-6-2**<br>Wavelength Tunable (1.55 µm Region) InAs/InGaAsP/InP (100) Quantum Dots in Telecom Laser Applications<br>R. Nötzel, S. Anantathanasarn, P. J. van Veldhoven, F. W. M. van Otten, T. J. Eijkemans, Y. Barbarin, E. A. J. M. Bente, T. du. Vries, E. Smalbrugge, E. J. Geluk, Y. S. Oei, M. K. Smit and J. H. Wolter, *Eindhoven Univ. of Technology, The Netherlands* | **17:15 C-6-2**<br>An Advanced Air Gap Process for MLC flash memories reducing Vth interference and realizing high reliability.<br>K. Tsukamoto, T. Murata, T. Fukumura, F. Ohta, T. Yoshitake, S. Shimizu, Y. Ikeda, K. Asai, M. Shimizu and O. Tsuchiya, *Renesas Technology Corp., Japan* | **17:05 D-6-3**<br>65nm Node Transistor Characteristic Evaluation Technology for Assembly Stress and Assembly Stress Relaxation Design<br>K. Takemura, M. Takahashi, H. Sano, K. Koike, Y. Itoh and H. Hirano, *Matsushita Electric, Japan* | |
| **17:30 A-6-4**<br>DNA Aptamer-Based Biosensing of Immunoglobulin E Using Carbon Nanotube Field-Effect Transistors<br>T. Katsura[1], K. Maehashi[1], K. Matsumoto[1], K. Kerman[2], Y. Takamura[2] and E. Tamiya[2], *[1]Osaka Univ. and [2]JAIST, Japan* | **17:30 B-6-3**<br>Novel Quantum Dot 3-section Super-luminescent Diode<br>Y.C. Xin[1], A. Martinez[1], T. A. Saiz[1], T. Nilsen[1,2], A. L. Moscho[1], Y. Li[1], A. Gray[4], A. Vahktin[3] and L. F. Lester[1], *[1]Univ.of New Mexico, [2]Univ. of Science and Technology, [3]Southwest Sciences, Inc. and [4]Zia Laser, Inc., USA* | **17:35 C-6-3**<br>Very Low Bit Error Rate in Flash Memory using Tunnel Dielectrics formed by Kr/$O_2$/NO Plasma Oxynitridation<br>T. Suwa[1], H. Takahashi[1], Y. Kumagai[1], G. Fujita[1], A. Teramoto[1], S. Sugawa[1] and T. Ohmi[1], *Tohoku Univ., Japan* | **17:25 E-6-3**<br>Dopant-atom distribution measurement at p-n junctions on wet-prepared Si(111): H surfaces by scanning tunneling microscopy<br>M. Nishizawa, L. Bolotov and T. Kanayama, *MIRAI-ASRC-AIST, Japan* |
| **17:45 A-6-5**<br>Surface Potential Measurement of Carbon Nanotube FETs using Kelvin Probe Force Microscopy<br>T. Umesaka[1], H. Ohnaka[1], Y. Ohno[1,2], S. Kishimoto[1], K. Maezawa[1] and T. Mizutani[1], *[1]Nagoya Univ. and [2]PRESTO, Japan* | **17:45 B-6-4**<br>MBE Growth of High Power Quantum Dot Superluminescent LEDs<br>S. K. Ray, T. L. Choi, K. M. Groom, H. Y. Liu, M. Hopkinson and R. A. Hogg, *Univ. of Sheffield, UK* | | | |

**18:30-20:30 Rump Session (Room 501, Room 502)**



| Room 419 (F) | Room 501 (G) | Room 502 (H) | Room 511/512 (I) | Small Auditorium (J) |
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| | | | **17:15 I-6-2**<br>A 0.6V Supply CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization<br>Y. Masui, T. Yoshida, M. Sasaki and A. Iwata, *Hiroshima Univ., Japan* | |
| **17:25 F-6-3**<br>Impact of Silicon Film Thickness on LF Noise in SOI Devices<br>L. Zafari, J. Jomaah and G. Ghibaudo, *IMEP, France* | | | **17:35 I-6-3**<br>Low-Voltage, Low-Phase-Noise Ring-VCO using 1/f-Noise Reduction Techniques<br>T. Yoshida, N. Ishida, M. Sasaki and A. Iwata, *Hiroshima Univ., Japan* | **17:25 J-6-3**<br>Strong Fermi-level Pinning of Wide Range of Work-function Metals at Valence Band Edge of Germanium<br>T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan* |

**18:30-20:30 Rump Session (Room 501, Room 502)**