Wednesday, September 13

MAIN HALL, 1F

PL: Opening Session (10:00–12:20)
Chairpersons: T. Hiramoto, Univ. of Tokyo and Y. Hirayama, Tohoku Univ.

10:00 Pl-0
Welcome Address and Award Presentation
H. Sakaki, Univ. of Tokyo

10:40 PL-1 (Plenary)
Nano-CMOS & Emerging Technologies–Myths and Hopes
T. Skotnicki, STMicroelectronics, France

11:30 PL-2 (Plenary)
MEMS as Key Components for Systems
M. Esashi, Tohoku Univ., Japan

12:20-14:00 Lunch

Room 411/412 (A)

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-1: Novel Devices and Characterization
(14:00-15:45)
Chairs: J. Motohisa (Hokkaido Univ.)
Y. Nakamura (NEC)

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-1: Special Session ; Photonic Crystals and Si Photonics I
(14:00-16:00)
Chairs: S. Noda (Kyoto Univ.)
M. Tokushima (NEC)

Room 414/415 (C)

Area 5: Advanced Circuits and Systems

C-1: MEMS and Modeling
(14:00-15:20)
Chairs: T. Komuro (Agilent Technologies International Japan)
K. Masu (Tokyo Tech)

C-1: MEMS and Modeling
(15:20-16:20)
Chairs: T. Hamasaki (Texas Instruments Japan)
M. Horiguchi (Renesas)

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-1: Organic Light Emitting Diodes
(14:00-15:45)
Chairs: Y. Ohmori (Osaka Univ.)
T. Sano (Sanyo Electric)

Room 418 (E)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

E-1: High-Speed Devices and Ics
(14:00-15:45)
Chairs: K. Maezawa (Nagoya Univ.)
S. Yamahata (NTT)

Room 419 (F)

Area 4: Advanced Memory Technology

F-1: FeRAM
(14:00-15:50)
Chairs: T. Eshita (Fujitsu)
H. S. Jeong (Samsung Electronics)

Room 501 (G)

Area 2: Characterization and Materials Engineering for Interconnect Integration

G-1: Advanced Metallization
(14:00-15:50)
Chairs: S. Ogawa (Selete/ Matsushita)
K. Ueno (Shibaura Institute of Technology)

Room 502 (H)

Area 3: CMOS Devices/Device Physics

H-1: CMOS Performance Enhancement Technology I
(14:00-16:00)
Chairs: K. Shibahara (Hiroshima Univ.)
D. Hisasmoto (Hitachi)

Room 511/512 (I)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

I-1: Nanostructure Fabrication
(14:00-15:45)
Chairs: T. Sogawa (NTT)
K. Yamaguchi (Univ. of Electro-Communications)

Small Auditorium (J)

Area 1: Advanced Gate Stack / Si Processing Science

J-1: Metal/High-k Gate Stack
(14:00-16:00)
Chairs: Y. Nara (Selete)
J. Yugami (Renesas)

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
14:00 A-1-1 (Invited) Nanowire Field Effect Transistor L. E. Wernersson, *Lund Univ., Sweden*	**14:00 B-1-1 (Invited)** Control of Light Emission and Propagation in Semiconductor Photonic Nanostructures T. Baba, *Yokohama National Univ., Japan*	**14:00 C-1-1 (Invited)** Low-Voltage Operated Piezoelectric Tunable Capacitor for Reconfigurable RF Systems T. Kawakubo, T. Nagano, M. Nishigaki and K. Itaya, *Toshiba Corp., Japan*	**14:00 D-1-1 (Invited)** Highly Efficient Carrier Injection and Transport in Organic Light Emitting Diodes C. Adachi, *Kyushu Univ., Japan*	**14:00 E-1-1 (Invited)** InP-based High-speed Transistors and their IC Applications K. Murata, K. Sano, H. Fukuyama, T. Kosugi, M. Nakamura, K. Kurishima, M. Tokumitsu and T. Enoki, *NTT Corp., Japan*
14:30 A-1-2 Infrared detection with silicon nano transistors K. Nishiguchi[1], Y. Ono[1], A. Fujiwara[1], H. Yamaguchi[1], H. Inokawa[2] and Y. Takahashi[3], *[1]NTT Corp., [2]Shizuoka Univ. and [3]Hokkaido Univ., Japan*	**14:30 B-1-2 (Invited)** All-Optical Switching and Control of Si Photonic Crystal Nanocavities M. Notomi, *NTT Corp., Japan*	**14:30 C-1-2 (Invited)** MEMS Packaging for RF Switch T. Seki, *OMRON, Japan*	**14:30 D-1-2** Top emission organic light emitting diodes with double metal layer anode C. R. Tsai, F. S. Juang, L. W. Ji, Y. S. Tsai and C. C. Liu, *National Formosa Univ., Taiwan*	**14:30 E-1-2** High Power and Stable Oscillations in the RTD Pair Oscillator ICs Fabricated with Metamorphic RTDs K. Maezawa[1], Y. Ookawa[1], S. Kishimoto[1], T. Mizutani[1], M. Takakusaki[2] and H. Nakata[2], *[1]Nagoya Univ. and [2]Nippon Mining & Metals Co., Ltd., Japan*
14:45 A-1-3 High-Resolution Measurement of Ultra-Shallow Structures by Scanning Spreading Resistance Microscopy L. Zhang, K. Ohuchi, K. Adachi, M. Tomita, K. Ishimaru, M. Takayanagi and A. Nishiyama, *Toshiba Corp., Japan*			**14:45 D-1-3** The Experiment and Simulation Study Top Emission PLEDs Using LiF/Ag/ITO Cathode C. W. Teng[1], Y. H. Lu[1], Y. C. Tsai[1], K. Y. Chang[1], S. H. Chou[1], K. C. Liu[1], L. C. Chen[2], Y. C. Fang[3] and H. E. Huang[3], *[1]Chang Gung Univ., [2]DELTA OPTOELECTRONICS and [3]CSIST, Taiwan*	**14:45 E-1-3** High-speed and Low-Power NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology H. Kim, S. Yeon and K. Seo, *Seoul National Univ., Korea*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
14:00 F-1-1 (Invited) Overview and Future Challenge of FeRAM Technologies Y. Kato, H, Tanaka, K. Isogai, K. Kaibara, Y. Kaneko and Y. Shimada, *Matsushita Electric, Japan*	**14:00 G-1-1 (Invited)** Carbon Nanotube via Technologies for Advanced Interconnect Integration M. Nihei[1,2], A. Kawabata[1,2], T. Hyakushima[1], S. Sato[1,2], T. Nozue[1], D. Kondo[1,2], H. Shioya[1,2], T. Iwai[2,3], M. Ohfuti[1,2] and Y. Awano[1,2], *[1]Selete, [2]Fujitsu Ltd. and [3]Fujitsu Labs., Japan*	**14:00 H-1-1 (Invited)** Direct Silicon Bonded (DSB) Mixed Orientation Substrate for High Performance Bulk CMOS Technology C. Y. Sung, H. Yin, H. Ng, K. L. Saenger, G. Pfeiffer, V. Chan, R. Zhang, J. Li, J. A. Ott, R. Bendernagel, S. B. Ko, Z. Ren, X. Chen, V. Ku, Z. J. Luo, N. Rovedo, K. Fogel, M. Khare, G. Shahidi and S. Crowder, *IBM, USA*	**14:00 I-1-1 (Invited)** GaN-based Quantum Wires, Discs, and Dots with Novel Electronic Properties K. H. Ploog, *Paul Drude Inst. for Solid State Electronics, Germany*	**14:00 J-1-1 (Invited)** Towards Metal-gate/ high-k Integration for High Performance CMOS Technology E. Cartier, *IBM, USA*
14:30 F-1-2 Full-Bit Functional, High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process K. R. Udayakumar[1], T. S. Moise[1], S. R. Summerfelt[1], F. G. Celii[1], G. Shinn[1], K. Boku[1], K. Remack[1], A. Haider[1], D. Anderson[1], J. Gertas[1], Y. Obeng[1], G. Albrecht[1], J. S. Martin [1], J. Rodriguez[1], B. Khan[1], S. Aggarwal[1], N. Schauer[1], H. McAdams[1], and A. Mckerrow[1] J. Eliason[2], J. Groat[2], R. Bailey[2], G. R. Fox[2], E. Jabillo[2] and J. Walbert[2], *[1]Texas Instruments Inc. and [2]Ramtron International Corp., USA*	**14:30 G-1-2** Ti-barrier Metal for Robust and Reliable 45nm Node Porous Low-k/Copper Interconnects K. Higashi[1], H. Yamaguchi[1], T. Yosho[1], A. Sakata[1], S. Omoto[1], S. Yamashita[1], T. Fujimaki[1], Y. Enomoto[2], N. Matsunaga[1] and H. Shibata[1], *[1]Toshiba Corp. and [2]Sony Corp., Japan*	**14:30 H-1-2 (Invited)** Strained-Silicon Transistors with Silicon-Carbon Source/Drain Y. C. Yeo, *National Univ. of Singapore, Singapore*	**14:30 I-1-2 (Invited)** Functions and Device Applications of Quantum-sized Silicon N. Koshida, *Tokyo Univ. o f Agriculture and Technology, Japan*	
14:50 F-1-3 Formation of Ferroelectric $Sr_2(Ta_{1-x}, Nb_x)_2O_7$ Thin Film on Amorphous SiO_2 by Microwave-Excited Plasma Enhanced Metalorganic Chemical Vapor Deposition I. Takahashi, K. Funaiwa, K. Azumi, S. Yamashita, Y. Shirai, M. Hirayama, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*	**14:50 G-1-3** Key mechanisms for improved EM lifetime of CoWP capped Cu interconnects Y. Kakuhara[1], N. Kawahara[1], K. Ueno[2] and N. Oda[1], *[1]NEC Corp. and [2]Shibaura Inst. of Tech., Japan*			**14:40 J-1-2** Demonstration of Low Vt NMOSFETs Using Thin HfLaO in ALD TiN/HfSiO Gate Stack C. S. Park[1], S. C. Song[1], G. Bersuker[1], H. N. Alshareef[2], B. S. Ju[1], P. Majhi[3], B. H. Lee[4], R. Jammy[4], H. K. Park[5], M. S. Joo[6], J. Pu[6] and B. J. Cho[6], *[1]SEMATECH, [2]Texas Instruments, [3]Intel, [4]IBM Assignee, [5]GIST and [6]NUS, USA*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
15:00 A-1-4 Imaging of interference between incident and reflected electron waves at an InAs/GaSb heterointerface by low-temperature scanning tunneling spectroscopy K. Suzuki[1], K. Kanisawa[1], S. Perraud[1,2], M. Ueki[3], K. Takashina[1] and Y. Hirayama[1,4,5], *[1]NTT Corp., [2]CNRS, [3]NTT Electronics Techno Corp., [4]SORST-JST and [5]Tohoku Univ., Japan*	**15:00 B-1-3** Photonic Crystal Nanocavity Continuous-wave Laser Operation at Room Temperature M. Nomura, S. Iwamoto, K. Watanabe, N. Kumagai, Y. Nakata, S. Ishida and Y. Arakawa, *Univ. of Tokyo, Japan*	**15:00 C-1-3** A Capacitive-Sensing Scheme for Control of Adaptive MEMS Device Stacked on CMOS LSI T. Shimamura[1], H. Morimura[1], K. Kuwabara[1], N. Sato[1], J. Terada[1], M. Ugajin[1], S. Shigematsu[1], K. Machida[2], M. Nakanishi[1] and H. Ishii[1], *[1]NTT Microsystem Integration Labs. and [2]NTT Advanced Technology Corp., Japan*	**15:00 D-1-4** Simulation for double ultra-thin separately doped red organic light-emitting diode S. H. Wang[1], T. S. Li[1], F. S. Juang[2] and Y. S. Tsai[2], *[1]Kun-Shan Univ. and [2]National Formosa Univ., Taiwan*	**15:00 E-1-4** Effect of flatness of heterointerfaces on device performance of InP-based HEMTs I. Watanabe[1], K. Shinohara[1], T. Kitada[2], S. Shimomura[2], A. Endoh[3], Y. Yamashita[3], T. Mimura[3], S. Hiyamizu[2] and T. Matsui[1], *[1]National Inst. of Information and Communications Technology, [2]Osaka Univ. and [3]Fujitsu Labs. Ltd., Japan*
		15:20 C-1-4 Equivalent Circuit Model for On-Chip Variable Inductor T. Yammouch, K. Ishida, K. Okada and K. Masu, *Tokyo Tech, Japan*		
15:15 A-1-5 Magnetopiezoresistance effects in an InAs/AlGaSb nanomechanical resonator with extremely small power consumption I. Mahboob[1], H. Okamoto[1], M. Ueki[1] and H. Yamaguchi[1,2], *[1]NTT Corp. and [2]Tohoku Univ., Japan*	**15:15 B-1-4** Modified Luminescence from Germanium Self-assembled Quantum Dots in Photonic Crystal Cavity at Room Temperature J. Xia[1], N. Usami[2], Y. Ikegami[1], Y. Nakata[3] and Y. Shiraki[1], *[1]Musashi Inst. of Technology, [2]Tohoku Univ. and [3]Horiba Ltd., Japan*	**15:40 C-1-5** On-Chip Asymmetric Coaxial Waveguide Structure for Chip Area Reduction I. C. H. Lai, H. Tanimoto and M. Fujishima, *Univ. of Tokyo, Japan*	**15:15 D-1-5** Black film improving the contrast ratio of organic light emitting diodes Y. L. Wu [1], Y. C. Lin[1], F. S. Juang[2] and Y. K. Su[3], *[1]National Changhua Univ. of Education, [2]National Formosa Univ. and [3]National Cheng Kung Univ., Taiwan*	**15:15 E-1-5** Thermally-stable gate technologies for InAlAs/InGaAs/InP HEMTs L. Wang, W. Zhao and I. Adesida, *Univ. of Illinois at Urbama Champaign, USA*
15:30 A-1-6 Structure, strength and conductance of palladium wires of single atom width T. Matsuda[1] and T. Kizuka[1,2], *[1]Univ. of Tsukuba and [2]JST, Japan*	**15:30 B-1-5** Highly Efficient and Stable Photoluminescence of Nanocrystalline Porous Silicon with Fully Annealed and Passivated Surfaces B. Gelloz[1] and N. Koshida[1,2], *[1]Tokyo Univ. of Agriculture and Technology and [2]Quantum14 Co., Japan*	**16:00 C-1-6** On-Die Monitoring of Substrate Coupling for Mixed-Signal Circuit Isolation D. Kosaka, M. Fujiwara, T. Danjo and M. Nagata, *Kobe Univ., Japan*		**15:30 E-1-6** The Gate Length Reducing Process for Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs S. J. Yeon, J. Lee, G. Seol and K. Seo, *Seoul National Univ., Korea*
Break				

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
15:10 F-1-4 Robust 2-D Stack Capacitor Technologies for 64Mb 1T1C FRAM J. Y. Jung, H. J. Joo, J. H. Park, S. K. Kang, H. S. Kim, D. Y. Choi, J. H. Kim, Y. S. Lee, Y. M. Kang, S. Y. Lee, H. S. Jeong and K. Kim, *Samsung Electronics Co., Ltd., Korea*	**15:10 G-1-4** A MOCVD TiSiN/Ta Barrier Metal for Improved EM Performance and Low Via/line Resistance using Direct Contact Via (DCV) Process for Sub-65 nm Technology H. C. Lee[1], S. J. Joo[1], I. C. Baek[1], C. Shim[1], J. H. Hong[1], J. W. Han[1], K. H. Kim[1] and Y. M. Kim[2], *[1]Dongbu Electronics and [2]Hongik Univ., Korea*	**15:00 H-1-3** Effect of Tensile Strain on Gate and Substrate Currents of strained-Si n-MOSFETs T. Hoshii, S. Sugahara and S. Takagi, *Univ. of Tokyo, Japan*	**15:00 I-1-3** Uniform Self-Formation of High-Density InAs Quantum Dots by InGaAs Embedding Growth S. Tonomura[1], M. Tomita[1] and K. Yamaguchi[1], *Univ. of Electro-Communications, Japan*	**15:00 J-1-3** Wide Controllability of Flatband Voltage in La_2O_3 Gate Stack Structures - Remarkable Advantages of La_2O_3 over HfO_2 - K. Ohmori[1], P. Ahmet[2], K. Shiraishi[3], K. Yamabe[3], H. Watanabe[4], Y. Akasaka[5], N. Umezawa[1], K. Nakajima[1], M. Yoshitake[1], T. Nakayama[6], K. S. Chang[7], K. Kakushima[2], Y. Nara[5], M. L. Green[7], H. Iwai[2], K. Yamada[8] and T. Chikyow[1], *[1]National Inst. for Materials Science, [2]Tokyo Tech, [3]Univ. of Tsukuba, [4]Osaka Univ., [5]Selete, [6]Chiba Univ., [7]National Inst. of Standards and Technology and [8]Waseda Univ., Japan*
		15:20 H-1-4 Sub-30 nm Strained P-Channel FinFETs with Condensed SiGe Source/Drain Stressors K. M. Tan[1], T. Y. Liow[1,2], R. T. Lee[1], K. J. Chui[1], C. H. Tung[2], N. Balasubramanian[2], G. S. Samudra[1], W. J. Yoo[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*	**15:15 I-1-4** Individual cathode luminescence spectroscopy of zinc oxide particles based on in situ transmission electron microscopy M. Ohyama[1] and T. Kizuka[1,2], *[1]Univ. of Tsukuba and [2]JST, Japan*	**15:20 J-1-4** Study of La Concentration Dependent V_{FB} Shift in Metal/HfLaOx/Si Capacitors Y. Yamamoto, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*
15:30 F-1-5 Impact of (111)-Oriented $SrRuO_3$/Pt Tailored Electrode for Highly Reproducible Preparation of MOCVD-PZT Film for High Density FeRAM N. Menou, H. Kuwabara and H. Funakubo, *Tokyo Tech, Japan*	**15:30 G-1-5** Modeling and Characterization of the On-chip Interconnects R. Kumar[1], S. C. Rustagi[1], S. Sun[1], K. Mouthaan[2] and T. K. S. Wong[3], *[1]Inst. of Microelectronics, [2]National Univ. of Singapore and [3]Nanyang Technological Univ., Singapore*	**15:40 H-1-5** Evaluating Strained/Relaxed-Ge, Strained-Si, Strained-SiGe For Future Nanoscale p-MOSFETs. T. Krishnamohan[1], D. Kim[1], C. Jungemann[2], Y. Nishi[1] and K. C. Saraswat[1], *[1]Stanford Univ. and [2]Univ. of the Armed Forces, USA*	**15:30 I-1-5** Facile Fabrication of Gold Nanoparticle-Titanium Oxide Alternate Assemblies by Surface Sol-Gel Process and Their Photoresponsive Properties T. Arakawa, T. Kawahara, T. Akiyama and S. Yamada, *Kyushu Univ., Japan*	**15:40 J-1-5** High quality La aluminates/Si (100) interface realized by passivation of Si dangling bonds with 1monolayer epitaxial $SrSi_2$ A. Takashima, Y. Nishikawa, T. Schimizu, D. Matsushita, M. Suzuki, T. Yamaguchi and N. Fukushima, *Toshiba Corp., Japan*
Break				

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Area 9: Physics and Applications of Novel Functional Materials and Devices	**Area 7: Photonic Devices and Device Physics**	**Area 5: Advanced Circuits and Systems**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**
A-2: Novel Optical Devices (16:15-18:00) Chairs: T. Usuki (Fujitsu Labs.) Y. Ohno (Tohoku Univ.)	B-2: Special Session ; Photonic Crystals and Si Photonics II (16:15-18:00) Chairs: O. Wada (Kobe Univ.) H. Yamada (NEC)	C-2: Wireless Interconnect (16:30-17:30) Chairs: M. Horiguchi (Renesas) R. Fujimoto (Toshiba) C-2: Wireless Interconnect (17:30-18:10) Chairs: R. Fujimoto (Toshiba) T. Hamasaki (Texas Instruments Japan)	D-2: Organic Light Emitting Diodes and Solar Cells (16:00-17:15) Chairs: Y. Ohmori (Osaka Univ.) T. Sano (Sanyo Electric) T. Someya (Univ. of Tokyo)	E-2: Wide-Bandgap Devices (16:15-17:45) Chairs: Y. Ohno (Univ. of Tokushima) S. Kuroda (Eudina Devices Inc.)
16:15 A-2-1 (Invited) Single Photon Detectors based on Quantum Dot Devices-from Principle of Operation to Single Photon Counting B. E. Kardynal[1], S. S. Hees[1,2], P. See[1], A. J. Shields[1], I. Farrer[2] and D. A. Ritchie[2], *[1]Toshiba Research Europe and [2]Univ. of Cambridge, UK*	**16:15 B-2-1 (Invited)** Integrated Photonic Network Node-Chip with Photonic Crystals H. Yamada[1,2], T. Chu[2], A. Gomyo[1,2], J. Uchida[1,2], S. Ishida[3] and Y. Arakawa[3], *[1]NEC Corp., [2]OITDA and [3]Univ. of Tokyo, Japan*	**16:30 C-2-1** 60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique K. Niitsu[1], N. Miura[1], M. Inoue[1], Y. Nakagawa[2], M. Tago[2], M. Fukaishi[2], H. Ishikuro[1] and T. Kuroda[1], *[1]Keio Univ. and [2]NEC Corp., Japan*	**16:00 D-2-1 (Invited)** TFT Technologies for Flexible Displays J. Jang, *Kyung Hee Univ., Korea*	**16:15 E-2-1 (Invited)** Diamond Electronics-Will it be able to compete with III-Nitrides?- E. Kohn, *Univ. of Ulm, Germany*
		16:50 C-2-2 Inter-chip Transmission Characteristics of Meander Dipole Antennas Integrated in 0.18 µm CMOS UWB Transceiver Chips K. Kimoto, N. Sasaki, M. Nitta, M. Fukuda and T. Kikkawa, *Hiroshima Univ., Japan*	**16:30 D-2-2** Efficient Red Electrophosphorescent Devices Based on Iridium Complexes of Fluorinated 1-phenylisoquinoline G. Y. Park, J. H. Seo, D. I. Yoo, Y. K. Kim, Y. S. Kim and Y. Ha, *Hongik Univ., Korea*	

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
Area 4: Advanced Memory Technology	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 3: CMOS Devices/Device Physics**	**Area 8: Advanced Material Synthesis and Crystal Growth Technology**	**Area 1: Advanced Gate Stack / Si Processing Science**
F-2: DRAM (16:15-18:00) Chairs: I. Asano (Elpida) H. S. Jeong (Samsung Electronics)	G-2: Characterization I (16:15-18:00) Chairs: N. Hata (AIST) F. Mizuno (Meisei Univ.)	H-2: CMOS Performance Enhancement Technology II (16:15-18:00) Chairs: F. Boeuf (STMicroelectronics) H. Oda (Renesas)	I-2: Compound Semiconductors (16:15-18:00) Chairs: K.H. Ploog (Paul Drude Inst.) D. Iwai (Fujitsu Labs.)	J-2: FUSI Gate Electrode (16:15-18:00) Chairs: K. Shiraishi (Univ. of Tsukuba) E. Cartier (IBM)
16:15 F-2-1 (Invited) Overview and Future Challenges eDRAM Technologies H. Sugimura, T. Wake, K. Inoue, M, Hamada, H. Shirai, S. Arai, M. Takeuchi, T. Sakoh, M. Sakao and T. Tanigawa, *NEC Corp., Japan*	**16:15 G-2-1 (Invited)** Ultralow-dielectric Polysilsesquioxane Films with High Modulus and Closed-pore Morphology D. Y. Yoon, *Seoul National Univ., Korea*	**16:15 H-2-1** Potential of and Issues with Multiple-Stressor Technology (MST) in High-Performance 45nm Generation Devices T. Miyashita[1], A. Hatada[1], Y. Shimamune[1], T. Owada[2], N. Tamura[1], T. Aoyama[1] and S. Satoh[1], *[1]Fujitsu Labs., Ltd. and [2]Fujitsu Ltd., Japan*	**16:15 I-2-1** Electrical Properties of Ge-Doped InSb and InAs on GaAs(111)A Substrate J. Nishinaga, R. Harada, T. Takada, A. Kawaharazuka and Y. Horikoshi, *Waseda Univ., Japan*	**16:15 J-2-1** Evaluation of Chemical Structures and Work Function of NiSi near the Interface between Nickel Silicide and SiO_2 A. Ohta[1], H. Yoshinaga[1], H. Murakami[1], D. Azuma[1], Y. Munetaka[1], S. Higashi[1], S. Miyazaki[1], T. Aoyama[2], K. Kosaka[2] and K. Shibahara[1], *[1]Hiroshima Univ., [2]Fujitsu Labs. and, Japan*
		16:35 H-2-2 Large Reduction in Standby Power Consumption Achieved with Stress-controlled SRAM Cell Layout H. Kudo[1], K. Ishikawa[1,], R. Tanabe[1], H. Fukutome[1], Y. Mishima[1], S. Satou[1], T. Sugii[1], F. Kihara[2], M. Okamoto[2], M. Yoshimura[2], T. Sugimachi[2], H. Hashimoto[2] and M. Ohtsuki[2], *[1]Fujitsu Labs., Ltd. and [2]Fujitsu Ltd., Japan*	**16:30 I-2-2** A method for suppressing deep-level emission in ZnSe/Ge/Ge_xSi_{1-x}/Si structure J. T. Ku[1], T. H. Yang[1], G. Luo[2], W. C. Chou[1], T. Y. Yang[3] and C. Y. Chang[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]Academia Sinica, Taiwan*	**16:35 J-2-2** Pd_2Si Fully-Silicided Gate: Kinetics of Silicide Formation and Workfunction Tuning T. Hosoi, K. Sano, K. Hosawa and K. Shibahara, *Hiroshima Univ., Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
16:45 A-2-2 Optical Properties of Dynamically-Modulated Dots and Wires Formed by Surface Acoustic Waves T. Sogawa[1], H. Gotoh[1], Y. Hirayama[1], T. Saku[1], S. Miyashita[2], P. V. Santos[3] and K. H. Ploog[3], *[1]NTT Corp., [2]NTT Advanced Technology Corp. and [3]Paul Drude Inst., Japan*	**16:45 B-2-2** Compact Multi-Mode Optical Ring Resonators for Interconnection on Si Chips Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*		**16:45 D-2-3** Efficiency improvement in flexible phosphorescent organic light-emitting diode S. Y. Su[1], Y. S. Tsai[1], F. S. Juang[1], L. W. Ji[1], S. H. Wang[2] and Y. K. Su[3], *[1]National Formosa Univ., [2]Kun-Shan Univ. and [3]National Cheng Kung Univ., Taiwan*	**16:45 E-2-2** C-band GaN-FET Power Amplifiers with 160-W Output Power Y. Okamoto, A. Wakejima, K. Matsunaga, Y. Ando, T. Nakayama, K. Ota and H. Miyamoto, *NEC Corp., Japan*	**16:45 F-2-2** A Highly Reliable MIM Technology with non-Crystallized HfOx Dielectrics Using Novel MOCVD Stacked TiN Bottom Electrodes T. Ohtsuka[2], Y. Shibata[1], H. Arai[1], H. Ichimura[1], S. Matsuyama[1], K. Uchiyama[1], J. Suzuki[1], A. Tsuzumitani[1], K. Yoneda[1], Y. Hashimoto[1], T. Nakabayashi[1] and E. Fujii[1], *[1]Matsushita Electric and [2]Panasonic Semiconductor Engineering Co., Ltd., Japan*	**16:45 G-2-2** SiOCH Films with Hydrocarbon Network Bonds: First-Principles Investigation N. Tajima[1], T. Hamada[2], T. Ohno[1], K. Yoneda[3], S. Kondo[3], N. Kobayashi[3], M. Shinriki[4], K. Miyazawa[4], K. Sakota[4], S. Hasaka[4] and M. Inoue[4], *[1]NIMS, [2]Univ. of Tokyo, [3]Selete and [4]Taiyo Nippon Sanso Corp., Japan*	**16:55 H-2-3** Layout Independent Transistor with Stress-controlled and Highly Manufacturable STI Process K. Horita, M. Ishibashi, H. Umeda, T. Kawahara, T. Ikeda, T. Yamashita, T. Kuroi and Y. Inoue, *Renesas Technology Corp., Japan*	**16:45 I-2-3** Effect of Hydrogen in Zinc Oxide Thin-Film Transistor grown by MOCVD J. Jo[1], O. Seo[2], E. Jeong[1], H. Seo[1], B. Lee[3] and Y. I. Choi[1], *[1]Ajou Univ., [2]NFC and [3]CDA Co., Ltd., Korea*	**16:55 J-2-3** Workfunction Adjustment Using Thin Metal Film (Ti, Pd) under FUSI Gate Electrode and Laser Annealing Y. Huang [1,2,3], K. L. Pey[1], D. Z. Chi[3], K. K. Ong[1], P. S. Lee[1] and I. S. Goh[2], *[1]Nanyang Technological Univ., [2]Systems on Silicon Manufacturing Co. Pte. Ltd. and [3]Inst. of Material Research & Engineering, Singapore*
17:00 A-2-3 Photon Statistics in a Thick Barrier Coupled Quantum Dot S. Yamauchi[1,2], A. Shikanai[1,2], I. Morohashi[1,2], S. Furue[1,2], K. Komori[1,2], T. Sugaya[1,2] and T. Takagahara[3], *[1]AIST, [2]CREST and [3]Kyoto Inst. of Technology, Japan*	**17:00 B-2-3** Silicon Optical Modulators in Silicon-on-Insulator (SOI) Substrate Based on the p-i-n Waveguide Structure M. T. Hsu and R. W. Chuang, *National Cheng Kung Univ., Taiwan*	**17:10 C-2-3** On-Chip Yagi Antenna for Wireless Signal Transmission in Stacked MCP K. Ohashi[1], T. Yammouch[1], M. Kimura[1], H. Ito[1], K. Okada[1], K. Ishida[1], K. Itoi[2], M. Sato[2], T. Ito[2] and K. Masu[1], *[1]Tokyo Tech and [2]Fujikura Ltd., Japan*	**17:00 D-2-4** Energy Transfer Employing Europium Complex and Blue Phosphorescent Dye and Application for White Organic Light-Emitting Diodes Y. Hino, H. Kajii and Y. Ohmori, *Osaka Univ., Japan*	**17:00 E-2-3** GaN-based Direct-coupled FET Logic (DCFL) Digital Circuits Operating at 375ºC Y. Cai, Z. Cheng, Z. Yang, C.W. Tang, K.M. Lau, K.J. Chen, *Hong Kong University of Science and Technology, Hong Kong*	**17:05 F-2-3** Robust and Cost-Effective MIS-Al_2O_3/SiON Double-Layered Capacitor Technology for Sub-90 nm DRAMs O. Tonomura, H. Hamamura and H. Miki, *Hitahchi Ltd., Japan*	**17:05 G-2-3** Nondestructive characterization of temperature-dependent backbone Si-O-Si structure in porous silica films by in-situ Fourier-transform infrared spectroscopy S. Takada[1], N. Hata[1,2], X. Li[1], N. Fujii[3], T. Nakayama[3] and T. Kikkawa[2,4], *[1]ASRC-AIST, [2]MIRAI-ASRC-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*		**17:00 I-2-4** The Effect of As_2 and As_4 Molecule Beam Species on MBE Grown GaN_xAs_{1-x} /GaAs MQW by Modulated N Radical Beam Source M. Kakino[1], K. Fujii[1], K. Takao[1], H. Miyagawa[1], N. Tsurumachi[1], H. Itoh[1], S. Nakanishi[1], H. Akiyama[2] and S. Koshiba[1], *[1]Kagawa Univ. and [2]Univ. of Tokyo, Japan*	
17:15 A-2-4 Exciton Rabi Oscillation in InAs/GaAs Coupled Quantum Dot K. Goshima[1,2], K. Komori[1,2], S. Yamauchi[1,2], I. Morohashi[1,2] and T. Sugaya[1, 2,]*[1]AIST and [2]CREST, Japan*	**17:15 B-2-4** Low Temperature Fabrication of Monolithic Mach-Zehnder Optical Modulator on Silicon using Sputtered (Ba,Sr)TiO_3 and Mechanism of Transient Response M. Suzuki, K. Nagata, Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*		**17:15 D-2-5** Formation of bulk-heterojunction structure in organic bilayer solar cells by heat treatment T. Osasa, S. Yamamoto and M. Matsumura, *Osaka Univ., Japan*	**17:15 E-2-4** Effects of Growth Temperature of a GaN Cap Layer on Electrical Properties of AlGaN/GaN HFETs T. Deguchi[1], M. Yamashita[1], E. Waki[1], A. Nakagawa[1], H. Ishikawa[2] and T. Egawa[2], *[1]New Japan Radio Co., Ltd. and [2]Nagoya Inst. of Technology, Japan*	**17:25 F-2-4** Diffusion Barrier Characteristics of TiSix/TiN for Tungsten Dual Poly Gate in DRAM M. G. Sung, K. Y. Lim, H. J. Cho, S. R. Lee, S. A. Jang, Y. S. Kim, M. S. Joo, J. H. Lee, T. Y. Kim, H. S. Yang, S. H. Pyi and J. W. Kim, *Hynix Corp., Korea*	**17:25 G-2-4** Characterization of Low-k Interconnect Dielectrics by EELS Y. Otsuka[1], M. Shimada[2], N. Kawasaki[1] and S. Ogawa[2], *[1]Toray Research Center Inc. and [2]Selete, Japan*	**17:15 H-2-4** A Full Analytical Model to evaluate Strain Induced by CESL on MOSFET Performances F. Payet[1], F. Boeuf[1], C. Ortolland[2] and T. Skotnicki[1], *[1]STMicroelectronics and [2]Philips Semiconductors, France*	**17:15 I-2-5** GaN Heteroepitaxy on Si(111) substrates Using AlN/AlGaN Superlattice Buffer Layers T. Akasaka, Y. Kobayashi and T. Makimoto, *NTT Corp., Japan*	**17:15 J-2-4** The first principles calculations of fermi level pinning in FUSI-PtSi/HfO_2/Si system induced by local distortion of HfO_2 M. Ikeda[1], G. Kresse[2], M. Kadoshima[1], T. Nabatame[1], H. Satake[1] and A. Toriumi[3,4], *[1]MIRAI-ASET, [2]Univ. Wien, [3]MIRAI-AIST and [4]Univ. of Tokyo, Japan*

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17:30 A-2-5 Study of Basic Characteristics of Spin - Photodiode Consisting of III-V p-n Heterojunction J. Hayafuji, T. Kondo and H. Munekata, *Tokyo Tech, Japan*	**17:30 B-2-5** Light emission from two junction Si CMOS LED's (450nm - 750nm) with two order increase in emission intensity-Applications for next generation silicon-based optoelectronics L. W. Snyman[1], M. du Plessis[2] and H. Aharoni[3], *[1]Tshwane Univ. of Technology, [2]Univ. of Pretoria and [3]Ben Gurion Univ. of the Negev, South Africa*	**17:30 C-2-4** On-chip Ultra-Wideband Receiver using Silicon Integrated Antennas for Inter-chip Wireless Interconnection N. Sasaki, M. Fukuda, M. Nitta, K. Kimoto and T. Kikkawa, *Hiroshima Univ., Japan*	**17:30 D-2-6** Build-on Technology of Bi-Directional Optical Communication System using Bi-Functional Organic Diodes H. Okada, Y. Matsushita, S. Naka and H. Onnagawa, *Univ. of Toyama, Japan*	**17:30 E-2-5** The High Temperature Thermally Treated SiNx Passivation of AlGaN/GaN HEMT using Remote PECVD J. C. Her[1], D. H. Kim[1], S. W. Kim[1], K. C. Jang[1], J. H. Lee[2] and J. E. Oh[3], *[1]Seoul National Univ., [2]THELEDS Co., LTD. and [3]Hanyang Univ., Korea*
17:45 A-2-6 Resonant Terahertz Detection Based on High-electron-mobility Transistor with Schottky Source/Drain Contact A. Satou[1], V. Ryzhii[1], T. Otsuji[2] and M. S. Shur[3], *[1]Univ. of Aizu, [2]Tohoku Univ. and [3]Rensselaer Polytechnic Inst., Japan*		**17:50 C-2-5** A 0.18 μm CMOS Impulse Radio Based UWB Transmitter for Global Wireless Interconnections of 3D Stacked-Chip System M. Fukuda, P. K. Saha, N. Sasaki, M. Nitta and T. Kikkawa, *Hiroshima Univ., Japan*		

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		17:35 H-2-5 56% pMOSFETs Drive Current Enhancement from Optimized Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS K. H. Lee, C. T. Huang, W. H. Hung, L. S. Jeng, S. F. Ting, M. L. Tseng, J. C. Wu, T. M. Shen, O. Cheng and C. W. Liang, *United Microelectronics Corp., Taiwan*	**17:30 I-2-6** Strong Ultraviolet Emission from InGaN/AlGaN Multi Quantum Well Grown by Multi-step Process H. G. Chen, H. H. Yao, J. T. Chu, N. F. Hsu, T. C. Lu, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ., Taiwan*	**17:35 J-2-5** Si-Capped Annealing of HfO_2-based Dielectrics for Suppressing Interface Layer Growth and Oxygen Out-Diffusion M. Takahashi[1], H. Satake[1], M. Kadoshima[1], A. Ogawa[1], K. Iwamoto[1], H. Ota[2], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*
17:45 F-2-5 Gate Workfunction Engineering of Bulk FinFETs for Sub-50 nm DRAM Cell Transistors K. H. Park, K. R. Han, Y. M. Kim and J. H. Lee, *Kyungpook National Univ., Korea*	**17:45 G-2-5** Local Bonding Structure of High-Stress Silicon Nitride Film modified by UV Curing for Strained-Silicon Technology beyond 45nm Node SoC Devices Y. Miyagawa[1], T. Murata[1], Y. Nishida[1], T. Nakai[1], A. Uedono[2], N. Hattori[1], M. Matsuura[1], K. Asai[1] and M. Yoneda[1], *[1]Renesas Technology Corp. and [2]Univ. of Tsukuba, Japan*		**17:45 I-2-7** Hexagonal Boron Nitride Heteroepitaxial Layers on Graphitized 6H-SiC Substrate Grown by Metalorganic Vapor Phase Epitaxy Y. Kobayashi[1], H. Hibino[1], T. Nakamura[2], T. Akasaka[1], T. Makimoto[1] and N. Matsumoto[2], *[1]NTT Corp. and [2]Shonan Inst. of Technology, Japan*	

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