Advance Program Part II

LATE NEWS PAPERS

Tuesday, September 13

Oral Session

Room 501 (B)

17:25 B-2-6L Fully-depleted ultra narrow (~10 nm) body Gate-All-Around CMOS transistors
N. Singh[1], A. Agarwal[1], L. Bera[1], W. Fang[2], R. Kumar[1], G. Q. Lo[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore*

Room 505 (F)

17:15 F-2-7L Unpinning of the Fermi level at clean (111)A surfaces of heavily Si-doped $In_{0.53}Ga_{0.47}As$ thin films epitaxially grown on InP substrates
S. Perraud[1, 2], K. Kanisawa[1], Z. Z. Wang[2] and Y. Hirayama[1, 3], *[1]NTT Basic Research Labs., [2]Laboratoire de Photonique et de Nanostructures, CNRS and [3]SORST-JST*

17:30 F-2-8L Hetero-Epitaxial Growth of GaN onto SiC-on-SIMOX Substrates
T. Yokoyama[1], T. Egawa[2], K. Oouchi[3], M. Nakao[3], T. Shirahata[1], S. Kobayashi[1] and K. Izumi[3], *[1]Air Water Inc., [2]Nagoya Inst. of Technology and [3]Osaka Prefecture Univ.*

Room 401 (G)

17:45 G-2-9L Room temperature negative differential conductance due to resonant tunneling through a single nanocrystalline-Si quantum dot
A. Surawijaya[1], H. Mizuta[1, 2] and S. Oda[1, 2], *[1]Tokyo Tech and [2]SORST-JST*

Room 403 (I)

17:15 I-2-7L AlGaN/GaN MIS-HEMTs Fabricated Using $SiN/SiO_2/SiN$ Triple-Layer Insulators
A. Endoh[1], Y. Yamashita[1], N. Hirose[2], K. Hikosaka[1], T. Matsui[2], S. Hiyamizu[3] and T. Mimura[1], *[1]Fujitsu Labs. Ltd., [2]National Inst. of Information and Communications Technology and [3]Osaka Univ.*

Wednesday, September 14

Oral Session

Room 501 (B)

10:15 B-3-4L Mobility Increase in High-Ns Region in (110)-Oriented UTB pMOSFET Through Surface Roughness Improvement
D. Januar, G. Tsutsui, M. Saitoh and T. Hiramoto, *Univ. of Tokyo*

18:00 B-6-4L P-channel Vertical Tunnel Field-Effect Transistors Down to Sub-50 nm Channel Length
K. K. Bhuwalka, M. Born, M. Schindler, M. Schmidt, T. Sulima and I. Eisele, *Univ. der Bundeswehr*

Room 504 (E)

17:45 E-6-4L High Temperature Operation (> 100ºC) of InGaAs/GaAs All-Active Monolithic Passively-Mode-Locked Single Quantum Well Lasers
Y. Xin, A. Stintz, H. Cao, M. Osinski, L. and Lester, *Univ. of New Mexico*

18:00 E-6-5L Characteristics of Flip-Chip InGaN LEDs on Patterned Sapphire Substrates
W. K. Wang[1], S. H. Lin[2], D. S. Wuu[1, 2] and R. H. Horng[1], *[1]National Chung Hsing Univ. and [2]National Formosa Univ.*

Room 401 (G)

12:00 G-4-6L Performance Investigation of Field-Emission Device Surrounded by High-k Dielectric (FESH)
K. Murashima and Y. Omura, *Kansai Univ.*

Room 403 (I)

18:00 I-6-5L C-band AlGaN/GaN HEMTs with 170W Output Power
Y. Takada[1], H. Sakurai[2], K. Matsushita[2], K. Masuda[2], S. Takatsuka[2], M. Kuraguchi[2], T. Suzuki[1], T. Suzuki[1], M. Hirose[1], H. Kawasaki[2] and K. Takagi[2] and K. Tsuda[1], *[1]Corporate Research & Development Center and [2]Toshiba Corp.*

Poster Session (13:15-15:00)

Reception Hall

P1: Advanced Gate Stack / Si Processing Science

P1-29L Modulation of NiGe/Ge Schottky Barrier Height by Dopant and Sulfur Segregation during Ni Germanidation for Metal S/D Ge MOSFETs
K. Ikeda[1], Y. Yamashita[1], N. Taoka[2], N. Sugiyama[1] and S. Takagi[2, 3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo*

P1-30L Moisture Absorption-Induced Permittivity Deterioration and Surface Roughness Enhancement of Lanthanum Oxide Films on Silicon
Y. Zhao, M. Toyama, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo*

P2: Characterization and Materials Engineering for Device Integration

P2-15L Photoluminescence characterization of strained Si-SiGe-on-insulator wafers
D. Wang[1], K. Matsumoto[2], M. Nakamae[2] and H. Nakashima[1], *[1]Kyushu Univ., [2]SUMCO*

P3: CMOS Devices / Device Physics

P3-21L Empirical Quantitative Modeling of Threshold Voltage of Sub-50-nm Double-Gate SOI MOSFET's
Y. Tahara and Y. Omura, *Kansai Univ.*

P3-22L Effective Prevention of Single Event Burnout for N-Channel Power MOSFETs
Y. L. Lai[1] and C. Y. Huang[2], *[1]National Changhua Univ. of Education and [2]Feng Chia Univ.*

P3-23L A Novel Statistical Methodology for Sub-100 nm MOSFET Fabrication Optimization and Sensitivity Analysis
Y. Li and Y. S. Chou, *National Chiao Tung Univ.*

P4: Advanced Memory Technology

P4-12L Ultra High Density HfO_2-Nanodot Memory for Flash Memory Scaling
H. Wakai, T. Sugizaki, T. Kumise, M. Kobayashi, M. Yamaguchi, T. Nakanishi and H. Tanaka, *Fujitsu Labs. Ltd.*

P4-13L Amorphous Channel SESO Memory with Good Logic Process Compatibility for Low-power High-density Embedded RAM
N. Kameshiro[1], T. Ishii[1], T. Mine[1], T. Sano[2] and T. Watanabe[1], *[1]Hitachi, Ltd. and [2]Renesas Northern Japan Semiconductor, Inc.*

P4-14L Reversible Resistive Switching in $Bi_4Ti_3O_{12}$ Thin Films Deposited by Election Cyclotron Resonance Sputtering
Y. Jin, H. Sakai and M. Shimada, *NTT Microsystem Integration Labs.*

P5: Advanced Circuits and Systems

P5-10L Measurement of Inductive Coupling in Wireless Superconnect
D. Mizoguchi, N. Miura, Y. Yoshida, N. Yamagishi and T. Kuroda, *Keio Univ.*

P5-11L A 20% Power Reduction in Two-stage Opamp by Source-Degenerated Active-Load Phase Compensation
A. Tamtrakarn, K. Ishida and T. Sakurai, *Univ. of Tokyo*

P5-12L A High Throughput Configurable Motion Estimation Processor Core for Video Applicaions
Y. K. Lai and L. F. Chen, *Chung-Hsing Univ.*

P5-13L A Novel Reconfigurable Computing Core for Multimedia System-on-Chip Applications
Y. K. Lai and C. Chien-Jou, *Chung-Hsing Univ.*

P5-14L Realizing Ultra-low Energy Application Specific SoC Architectures through Novel Probabilistic CMOS (PCMOS) Technology
K. Palem, L. N. Chakrapani, B. E. Akgul and P. Korkmaz, *Georgia Inst. of Technol.*

P6: Compound Semiconductor Circuits, Electron Devices and Device Physics

P6-14L Pulsed Characteristics of Microwave SiGe Heterojunction Bipolar Transistors Operated at High Collector Voltages
L. H. Chang[1], K. M. Chen[1], G. W. Huang[1], H. C. Tseng[2] and V. Liang[2], *[1]National Nano Device Labs. and [2]United Microelectronics Corp.*

P7: Photonic Devices and Device Physics

P7-21L Enhanced Extraction Efficiency of Vertical Conducting InGaN LEDs with Micro-Pillar Surface
W. K. Wang[1], D. S. Wuu[1,2], W. Y. Lin[1], S. Y. Huang[1] and R. H. Horng[1], *[1]National Chung Hsing Univ. and [2]National Formosa Univ.*

P7-22L Optical Gain of Polarized Emission in InAs Quantum Dots with $In_xGa_{1-x}As$ Capping Layer
Y. Zhang[1], N. Tamura[1], T. Kita[1], O. Wada[1], Y. Nakata[2], H. Ebe[3], M. Sugawara[3] and Y. Arakawa[2], *[1]Kobe Univ., [2]Univ. of Tokyo and [3]Fujitsu Labs. Ltd.*

P8: Advanced Material Synthesis and Crystal Growth Technology

P8-10L Growth and Characterization of Germanium on Insulator (GOI) from Sputtered Ge by Novel Single and Dual Necking techniques
S. Balakumar[1], M. Mukherjee-Roy[1], Ramamurphy[1], G. Fei[1,2], C. Hang[1], R. Kumar[1], N. Balasubramanian[1], S. Tripathy[3], L. Sungjoo[2] and D. L. Kwong[1], *[1]Inst. of Microeletronics, [2]National Univ. of Singapore and [3]Inst. of Materials Research and Engineering*

P8-11L Control of Electrical Properties of Single-walled Carbon Nanotubes by Low-energy Electron Irradiation
K. Kanzaki, S. Suzuki, Y. Kobayashi, Y. Ono and H. Inokawa, *NTT Basic Research Labs.*

P8-12L Quantum Dot Formation by Post-Growth Annealing of a Wetting Layer
H. Z. Song[1,2], T. Usuki[1,2], Y. Nakata[1], N. Yokoyama[1], H. Sasakura[2,3] and S. Muto[2,3], *[1]Fujitsu Labs. Ltd., [2]CREST-JST and [3]Hokkaido Univ.*

P10: Organic Materials Science, Device Physics, and Applications

P10-12L Fabrication of Planar Nano-gap Electrodes for Single Molecule Evaluation
M. Nakata[1,3], T. Edura[1], K. Tsutsui[1], M. Tokuda[1], H. Onozato[1], T. Kaneko[1], K. Nagatsuma[1], M. Morita[1], K. Itaka[2,3], H. Koinuma[2,3] and Y. Wada[1,3], *[1]Waseda Univ., [2]Univ. of Tokyo and [3]CREST-JST*

P10-13L Electrospray Deposition of PEDOT-PSS and Electrochemical Characterization
R. Ohnishi[1], K. Kojima[2], K. Tanaka[1] and H. Usui[1], *[1]Tokyo Univ. of Agriculture and Technology and [2]Hitachi, Ltd.*

P10-14L Evaluation of Carrier Mobility Models for Organic Semiconductor Device Simulations
N. Ohashi, N. Hirashima, N. Goto, M. Nakamura and K. Kudo, *Chiba Univ.*

P11: Micro / Nano Electromechanical and Bio-Systems

P11-10L Fabrication of Photonic Crystals Using Nanoimprint Lithography
Y. L. Lai and C. C. Chiu, *National Changhua Univ. of Education*

Thursday, September 15

Oral Session

Room 502 (C)

10:15 C-7-4L Low Resistance Ni Thin Film Deposition for Nickel Silicide by Atomic Layer Deposition
K. W. Do, C. M. Yang, I. S. Kang, K. M. Kim, K. H. Back, H. I. Cho, H. B. Lee, J. H. Lee, S. H. Hahm, S. H. Kong and J. H. Lee, *Kyungpook Univ.*

Room 401 (G)

15:00 G-9-7L Chemical Modification of Multi-walled Carbon Nanotubes By Vacuum Ultraviolet (VUV) Irradiation Dry Process
K. Asano[1, 2], D. Kondo[1, 2], A. Kawabata[3], F. Takei[3], M. Nihei[3] and Y. Awano[1, 2], *[1]Fujitsu Ltd., [2]CREST-JST and [3]Fujitsu Labs. Ltd.*

15:15 G-9-8L One by One Control of Number of Carbon Nanotube Growth by Current Monitoring
M. Maeda[1, 3], T. Kamimura[2, 3], C. K. Hyon[3], K. Murata[3] and K. Matsumoto[2, 3], *[1]Univ. of Tsukuba, [2]Osaka Univ. and [3]CREST-JST*

UPDATED INFORMATION

P10-8 Improvement of on/off ratio of pentacene static induction transistor with ultra-thin CuPc layer
Y. Watanabe[1], H. Iechi[1,2] and K. Kudo[1,3], *[1]Optoelectronic Industry and Technology Development Association, [2]Ricoh Co. Ltd and [3]Chiba Univ., Japan*

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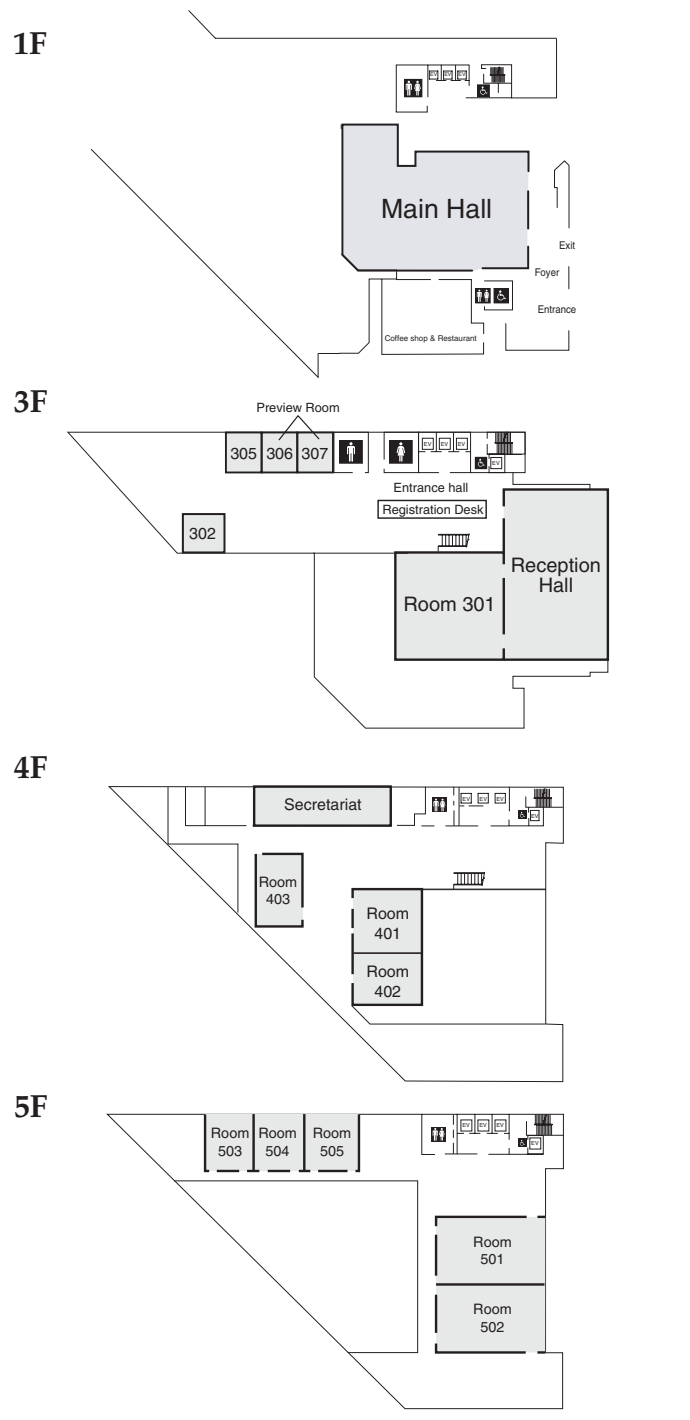
F-10-5 Room 505 (F) 16:15

Cancel

C-1-6 Room 501 (B) 15:45

D-2-5 Room 503 (D) 17:00

Floor Map



SSDM 2005 Time Table

* P# means the poster presentation of Area #

Tuesday, September 13

MAIN HALL

10:00-12:00 PL: Opening Session

Room 301	Room 501	Room 502	Room 503	Room 504	Room 505	Room 401	Room 402	Room 403
13:30-15:20 **Area1: Advanced Gate Stack/Si Processing Science** A-1: High-k Gate Dielectric Stacks I	**13:30-15:20** **Area3: CMOS Devices/Device Physics** B-1: Advanced CMOS Technology I	**13:30-15:40** **Area2: Characterization and Materials Engineering for Device Integration** C-1: Device Integration I	**13:30-15:30** **Area11: Micro/Nano Electromechanical and Bio-Systems** D-1: Micro/Nano Sensing Devices	**13:30-15:30** **Area7: Photonic Devices and Device Physics** E-1: Quantum Dot Nanostructure	**13:30-15:30** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-1: Growth and Synthesis of New Materials I	**13:30-15:30** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-1: Quantum Devices	**13:30-15:20** **Area4: Advanced Memory Technology** H-1: DRAM	**13:30-15:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-1: High-Voltage Devices
15:45-17:45 **Area1: Advanced Gate Stack/Si Processing Science** A-2: High-k Gate Dielectric Stacks II	**15:45-17:45** **Area3: CMOS Devices/Device Physics** B-2: Mobility Enhancement Technology	**16:05-17:35** **Area2: Characterization and Materials Engineering for Device Integration** C-2: New Technology	**15:45-17:15** **Area11: Micro/Nano Electromechanical and Bio-Systems** D-2: Design and Packaging	**15:45-17:45** **Area7: Photonic Devices and Device Physics** E-2: Lasers and LEDs	**15:45-17:45** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-2: Growth and Synthesis of New Materials II	**15:45-18:00** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-2: Silicon Nanodevices	**15:45-17:35** **Area4: Advanced Memory Technology** H-2: Flash Memory I	**15:45-17:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-2: Novel Devices and Applications

18:30-20:30 Banquet (PORTOPIA HOTEL Room KAIRAKU)

Wednesday, September 14

Room 301	Room 501	Room 502	Room 503	Room 504	Room 505	Room 401	Room 402	Room 403
9:15-10:15 **Area1: Advanced Gate Stack/Si Processing Science** A-3: High-k Gate Dielectric Stacks III	**9:15-10:35** **Area3: CMOS Devices/Device Physics** B-3: Carrier Transport I			**9:15-10:30** **Area7: Photonic Devices and Device Physics** E-3: Photonic Crystals and Light Control	**9:15-10:30** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-3: Nanostructure Fabrications	**9:15-10:30** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-3: Quantum Information Devices	**9:15-10:15** **Area4: Advanced Memory Technology** H-3: SRAM	
10:45-12:15 **Area1: Advanced Gate Stack/Si Processing Science** A-4: Characterization of Gate Dielectrics	**10:45-12:05** **Area3: CMOS Devices/Device Physics** B-4: Carrier Transport Modeling	**10:30-12:30** **Short Presentation** **P1, P2 and P4**	**10:30-12:30** **Short Presentation** **P6, P7, P8 and P9**	**10:45-12:15** **Area7: Photonic Devices and Device Physics** E-4: Si Photonics Interconnects and Optical	**10:45-12:15** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-4: Si and Related Materials	**10:45-12:15** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-4: Novel Devices I	**10:45-11:45** **Area4: Advanced Memory Technology** H-4: Flash Memory II	**10:30-12:30** **Short Presentation** **P3, P5, P10 and P11**

13:00-15:00 Poster Session (Reception Hall)

15:15-16:35 **Area1: Advanced Gate Stack/Si Processing Science** A-5: Characterization & Reliability of Gate Dielectrics	**15:15-16:45** **Area3: CMOS Devices/Device Physics** B-5: Advanced CMOS Technology II	**15:15-16:45** **Area2: Characterization and Materials Engineering for Device Integration** C-5: Characterization	**15:15-16:35** **Area5: Advanced Circuits and Systems** D-5: Antennas and Sensor	**15:15-16:45** **Area7: Photonic Devices and Device Physics** E-5: Detectors and Sensors I	**15:15-16:45** **Area10: Organic Materials Science, Device Physics, and Applications** F-5: Molecular Electronics and Physics I	**15:15-16:45** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-5: Novel Devices II	**15:15-16:45** **Area11: Micro/Nano Electromechanical and Bio-Systems** H-5: Bio Sensors and Chips I	**15:15-16:45** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-5: Nitride Devices
17:00-18:00 **Area1: Advanced Gate Stack/Si Processing Science** A-6: Alternative High-k Gate Dielectrics	**17:00-18:20** **Area3: CMOS Devices/Device Physics** B-6: Device Modeling	**17:00-18:00** **Area2: Characterization and Materials Engineering for Device Integration** C-6: Device Integration II	**17:00-18:10** **Area5: Advanced Circuits and Systems** D-6: Advanced System LSIs	**17:00-18:15** **Area7: Photonic Devices and Device Physics** E-6: Detectors and Sensors II	**17:00-18:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-6: Molecular Electronics and Physics II	**17:00-18:00** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-6: Spintronics	**17:00-18:15** **Area11: Micro/Nano Electromechanical and Bio-Systems** H-6: Bio Sensors and Chips II	**17:00-18:15** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-6: Nitride Devices

18:30-20:30 Rump Session
Room 501 "Beyond the Scaling Limit—Innovative Devices and Materials—"
Room 502 "Flexible Electronics—Is it Real?"

Thursday, September 15

Room 301	Room 501	Room 502	Room 503		Room 505	Room 401	Room 402	Room 403
9:15-10:25 **Area1: Advanced Gate Stack/Si Processing Science** A-7: Metal Gates I	**9:15-10:15** **Area3: CMOS Devices/Device Physics** B-7: Carrier Transport II	**9:15-10:35** **Joint Area 1, 2 and 3** C-7: Germanide and Defects	**9:15-10:25** **Area5: Advanced Circuits and Systems** D-7: Mixed-Signal Design		**9:15-10:30** **Area10: Organic Materials Science, Device Physics, and Applications** F-7: Organic Light Emitting Devices I	**9:15-10:45** **Joint Area 8 and 9** G-7: Joint Session Nanotubes and Nanowires I	**9:15-10:25** **Area4: Advanced Memory Technology** H-7: FeRAM I	**9:15-10:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-7: Modeling and Simulation
10:45-12:05 **Area1: Advanced Gate Stack/Si Processing Science** A-8: Metal Gates II	**10:45-12:15** **Area3: CMOS Devices/Device Physics** B-8: Device Reliability	**10:45-12:15** **Joint Area 1, 2 and 3** C-8: Advanced Source/Drain Technology	**10:45-12:05** **Area5: Advanced Circuits and Systems** D-8: High-Frequency Circuits		**10:45-12:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-8: Organic Light Emitting Devices II	**11:00-12:30** **Joint Area 8 and 9** G-8: Joint Session Nanotubes and Nanowires II	**10:45-12:05** **Area4: Advanced Memory Technology** H-8: FeRAM II	**10:45-11:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-8: Modeling and Simulation

12:30-13:30 SSDM 2005 Luncheon (PORTOPIA HOTEL Room KAIRAKU)

13:30-14:50 **Area1: Advanced Gate Stack/Si Processing Science** A-9: GeFETs & Simulation	**13:30-14:50** **Area3: CMOS Devices/Device Physics** B-9: Device Technology I	**13:30-14:50** **Joint Area 1, 2 and 3** C-9: Shallow Junction	**13:30-14:50** **Area5: Advanced Circuits and Systems** D-9: Device Characteristics and Circuits		**13:30-15:00** **Area10: Organic Materials Science, Device Physics, and Applications** F-9: Organic Transistors I	**13:30-15:30** **Joint Area 8 and 9** G-9: Joint Session Nanotubes and Nanowires III	**13:30-15:00** **Area4: Advanced Memory Technology** H-9: MRAM	
	15:15-16:15 **Area3: CMOS Devices/Device Physics** B-10: Device Technology II	**15:15-16:35** **Area1: Advanced Gate Stack/Si Processing Science** C-10: Metal Gates III	**15:15-16:25** **Area5: Advanced Circuits and Systems** D-10: Power Devices and Packaging Technologies		**15:15-16:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-10: Organic Transistors II		**15:15-16:15** **Area4: Advanced Memory Technology** H-10: PRAM	

SSDM 2005 Chairpersons List

	Main Hall	Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)	Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
Tuesday, September 13	**Main hall: (10:00-12:00)** M. Morita (Osaka Univ.) A. Toriumi (Univ. of Tokyo)	**A-1: (13:30-15:20)** Y. Nara (Selete) H. Satake (ASET)	**B-1: (13:30-15:20)** K. Shibahara (Hiroshima Univ.) J. C. S. Woo (UCLA)	**C-1: (13:30-15:40)** S. Ogawa (Matsushita Electric) K. Ueno (NEC)	**D-1: (13:30-15:30)** Y. Yoshino (Murata Mfg.) K. Sawada (Toyohashi Univ. of Tech.)	**E-1: (13:30-15:30)** M. Sugawara (Fujitsu Labs.) K. Komori (AIST)	**F-1: (13:30-15:30)** H. Yamaguchi (NTT) M. Tanaka (Univ. of Tokyo)	**G-1: (13:30-15:30)** J. Motohisa (Hokkaido Univ.) T. Fujisawa (NTT)	**H-1: (13:30-15:20)** I. Asano (Elpida) H. S. Jeong (Samsung Electronics)	**I-1: (13:30-15:30)** R. Hattori (Mitsubishi Electric) A. Nakagawa (New Japan Radio)
		A-2: (15:45-17:45) S. Miyazaki (Hiroshima Univ.) M. Niwa (Matsushita)	**B-2: (15:45-17:45)** K. Ohuchi (Toshiba) D. Hisamoto (Hitachi)	**C-2: (16:05-17:35)** T. Yoda (Toshiba) M. Nihei (Fujitsu Labs.)	**D-2: (15:45-17:15)** T. Ono (Tohoku Univ.) Y. Takamura (JAIST)	**E-2: (15:45-17:45)** O. Wada (Kobe Univ.) M. Ezaki (Toshiba)	**F-2: (15:45-17:45)** H. Asahi (Osaka Univ.) Y. Nanishi (Ritsumeikan Univ.)	**G-2: (15:45-18:00)** Y. Takahashi (Hokkaido Univ.) M. Tabe (Shizuoka Univ.)	**H-2: (15:45-17:35)** T. Kobayashi (Hitachi) C. Hsu (eMemory Tech.)	**I-2: (15:45-17:30)** S. Tanaka (NEC) S. Kuroda (Eudina Devices)
Wednesday, September 14	**A-3: (9:15-10:15)** J. Yugami (Renesas) T. Sugii (Fujitsu)	**B-3: (9:15-10:35)** H. C. Lin (National Chiao Tung Univ.) M. Ogawa (Kobe Univ.)			**E-3: (9:15-10:30)** S. Noda (Kyoto Univ.) M. Tokushima (NEC)	**F-3: (9:15-10:30)** S. Shimomura (Osaka Univ.) H. Yamaguchi (NTT)	**G-3: (9:15-10:30)** T. Usuki (Fujitsu) T. Fujisawa (NTT)	**H-3: (9:15-10:15)** C. Hsu (eMemory Tech.) Y. Yamauchi (Sharp)	
		A-4: (10:45-12:15) H. Satake (ASET) K. Shiraishi (Univ. of Tsukuba)	**B-4: (10:45-12:05)** M. Ogawa (Kobe Univ.) K. Kurimoto (Matsushita Electric)			**E-4: (10:45-12:15)** M. Tokushima (NEC) M. Ezaki (Toshiba)	**F-4: (10:45-12:15)** O. G. Schmidt (Max-Planck-Inst.) S. Miyazaki (Hiroshima Univ.)	**G-4: (10:45-12:15)** K. Ishibashi (RIKEN) H. Mizuta (Tokyo Tech.)	**H-4: (10:45-11:45)** Y. Yamauchi (Sharp) T. Kobayashi (Hitachi)	
		A-5: (15:15-16:35) S. Miyazaki (Hiroshima Univ.) B. Mizuno (UJT Lab.)	**B-5: (15:15-16:45)** K. Ohuchi (Toshiba) D. Hisamoto (Hitachi)	**C-5: (15:15-16:45)** N. Hata (AIST) F. Mizuno (Meisei Univ.)	**D-5: (15:15-16:35)** K. Masu (Tokyo Tech.) R. Fujimoto (Toshiba)	**E-5: (15:15-16:45)** T. Hatta (Mitsubishi Electric) K. Komori (AIST)	**F-5: (15:15-16:45)** K. Kudo (Chiba Univ.) Y. Ohmori (Osaka Univ.)	**G-5: (15:15-16:45)** K. Matsumoto (Osaka Univ.) Y. Takahashi (Hokkaido Univ.)	**H-5: (15:15-16:45)** H. Tabata (Osaka Univ.) H. Sugihara (Matsushita Electric)	**I-5: (15:15-16:45)** T. Hashizume (Hokkaido Univ.) T. Enoki (NTT)
		A-6: (17:00-18:00) H. Hwang (Gwangju Inst. of Sci. & Tech.) Y. Tsunashima (Toshiba)	**B-6: (17:00-18:20)** J. C. S. Woo (UCLA) Y. Momiyama (Fujitsu)	**C-6: (17:00-18:00)** T. Tatsumi (Sony) M. Matsuura (Renesas)	**D-6: (17:00-18:10)** M. Mizuno (NEC) H. Yamauchi (Sanyo Electric)	**E-6: (17:00-18:15)** Y. Lee (Hitachi) T. Hatta (Mitsubishi Electric)	**F-6: (17:00-18:15)** K. Kato (Niigata Univ.) M. Iwamoto (Tokyo Tech.)	**G-6: (17:00-18:00)** Y. Ohno (Tohoku Univ.) J. Motohisa (Hokkaido Univ.)	**H-6: (17:00-18:15)** H. Oana (Univ. of Tokyo) T. Nishimoto (Shimadzu)	**I-6: (17:00-18:15)** T. Hashizume (Hokkaido Univ.) T. Enoki (NTT)
hursday, September 15	**A-7: (9:15-10:25)** Y. Tsunashima (Toshiba) R. M. Wallace (Univ. of Texas at Dallas)	**B-7: (9:15-10:15)** Y. Momiyama (Fujitsu) H. Oda (Renesas)	**C-7: (9:15-10:35)** M. Kodera (Toshiba) M. Matsuura (Renesas)	**D-7: (9:15-10:25)** H. Yamauchi (Sanyo Electric) T. Komuro (Agilent Technologies International Japan)		**F-7: (9:15-10:30)** T. Kamata (AIST) T. Sano (Sanyo Electric)	**G-7: (9:15-10:45)** K. Matsumoto (Osaka Univ.) M. Nihei (Fujitsu Labs.)	**H-7: (9:15-10:25)** H. S. Jeong (Samsung Electronics) T. Eshita (Fujitsu)	**I-7: (9:15-10:30)** K. Maezawa (Nagoya Univ.) T. Tanaka (Matsushita Electric)
		A-8: (10:45-12:05) T. Aoyama (Fujitsu Labs.) G. Parsons (North Carolina State Univ.)	**B-8: (10:45-12:15)** D. Hisamoto (Hitachi) K. Kurimoto (Matsushita Electric)	**C-8: (10:45-12:15)** K. Ohuchi (Toshiba) Y. Nara (Selete)	**D-8: (10:45-12:05)** R. Fujimoto (Toshiba) M. Mizuno (NEC)		**F-8: (10:45-12:15)** H. Usui (Tokyo Univ. of Agri. & Tech.) T. Sano (Sanyo Electric)	**G-8: (11:00-12:30)** K. Ishibashi (RIKEN) G. Austing (National Research Council of Canada)	**H-8: (10:45-12:05)** T. Eshita (Fujitsu) N. Ishiwata (NEC)	**I-8: (10:45-11:30)** K. Maezawa (Nagoya Univ.) T. Tanaka (Matsushita Electric)
		A-9: (13:30-14:50) K. Shiraishi (Univ. of Tsukuba) J. Yugami (Renesas)	**B-9: (13:30-14:50)** K. Takeuchi (NEC) K. Shibahara (Hiroshima Univ.)	**C-9: (13:30-14:50)** H. Hwang (Gwangju Inst. of Sci. & Tech.) B. Mizuno (UJT Lab)	**D-9: (13:30-14:50)** T. Hamasaki (Texas Instruments Japan) K. Masu (Tokyo Tech.)		**F-9: (13:30-15:00)** K. Kudo (Chiba Univ.) H. Usui (Tokyo Univ. of Agri. & Tech.)	**G-9: (13:30-15:30)** T. Fukui (Hokkaido Univ.) K. Yamaguchi (Univ. of Electro-Communications)	**H-9: (13:30-15:00)** N. Ishiwata (NEC) Y. Ohji (Renesas)	
			B-10: (15:15-16:15) H. Oda (Renesas) K. Takeuchi (NEC)	**C-10: (15:15-16:35)** R. M. Wallace (Univ. of Texas at Dallas) T. Aoyama (Fujitsu Labs.)	**D-10: (15:15-16:25)** T. Komuro (Agilent Technologies International Japan) T. Hamasaki (Texas Instruments Japan)		**F-10: (15:15-16:15)** M. Iwamoto (Tokyo Tech.) T. Kamata (AIST)		**H-10: (15:15-16:15)** Y. Ohji (Renesas) I. Asano (Elpida)	