Call for Paper

2004

INTERNATIONAL CONFERENCE ON

SOLID STATE DEVICES AND MATERIALS

Conference — September 15-17, 2004

Short Course — September 14, 2004

Place — Tower Hall Funabori (Tokyo, Japan)

Paper Deadline — May 10, 2004

Online submission through the conference website is now available.

Late News Paper Deadline — July 25, 2004

2004 International Conference on Solid State Devices and Materials (SSDM 2004)

SECRETARIAT
c/o Inter Group Corp.
4-9-17, Akasaka, Minato-ku, Tokyo 107-8486 Japan
TEL:+81-3-3479-5131
FAX:+81-3-3423-1601
E-mail: ssdm@intergroup.co.jp

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The Institute of Image Information and Television Engineers
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ssdm 2004

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Call for Papers

2004 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: September 15-17, 2004
Short Course (in Japanese): September 14, 2004

The 2004 International Conference on Solid State Devices and Materials (SSDM 2004) will be held from September 15 to September 17, 2004 at the Tower Hall Funabori (Tokyo, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid state devices and materials. For the 2004 conference, 14 program subcommittees have been organized covering circuits and systems, as well as devices and materials. One-day short course is also scheduled for before the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM 2004 is available online at:

http://www. ssdm.jp

PLENARY SESSIONS

Plenary Speakers:

"Our Challenges to Achieve an Advanced Science and Technology-Oriented Nation"

M. Ohyama (Council for Science and Technology Policy, Cabinet Office, Japan)

"Silicon-Based Devices and Technology for the Nanoscale Era"

J.D. Plummer (Stanford Univ., USA)

"Spintronics-From Materials to Circuits-"

H. Ohno (Tohoku Univ., Japan)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging to discuss problems to be solved in these fields, new findings and new phenomena and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate the mutual understanding among people in the fields of devices and material and those in the fields of circuit, system and packaging. For the 2004 conference, fourteen program subcommittees have been organized in order to bring higher quality paper selection and strengthening into specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Silicon Circuits and Systems

(Chair, T. Kuroda, Keio Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems, are solicited in the subject areas including, but not limited to, the following: (1) Advanced digital, analog, mixed-signal, and memory, (2) Wireless, wireline, and optical communications, (3) Imagers, displays, and MEMS, (4) Low power technologies and power aware systems, (5) High speed circuits and systems, (6) Technologies for systems on a chip, (7) New concept and technologies; based on nanoelectronics, quantum mechanics, 3D-electronics, ferroelectrics, and photonics; using neural network, fuzzy logic, and multi-valued logic; and for bio-medical and microfluidic applications.

Invited speakers:
"Sub-100nm MOSFET Modeling for Integrated-Circuit Design"
A. Vladimirescu (UC Berkeley, USA)
"Impact of Device Scaling on High Speed I/O"
K. Yang (UCLA, USA)

Area 2

Advanced Silicon Devices and Device Physics

(Chair, K. Shibahara, Hiroshima Univ.)

The scope of this subcommittee covers all aspects of advanced silicon devices and device technologies for circuit applications. Papers are solicited in the following areas: (1) Sub-100nm silicon CMOS devices and their integration technologies including logic, memory and merged logic/memory LSIs, (2) Post-bulk-planar silicon device structures, including mobility enhancement technologies such as a strained-silicon, SiGe and Ge channels, (3) New concepts, theories and breakthroughs in silicon-related devices, passive devices and other functional devices, (4) Physics and reliability for advanced processes/devices including simulation and modeling and (5) Manufacturing and yield issues.

Invited speakers:
"Advanced CMOS Transistors with Strained Si/SiGe Channel and High-K/Metal Gate Stack"
S. Datta (Intel, USA)
"Nanoscale Device Simulation at the Scaling Limit and Beyond" (tentative)
G. Klimeck (Purdue Univ., USA)
"Gate Stress Induced Performance Enhancements" (tentative)
Z. Krivokapic (AMD, USA)
"Design Consideration of Body-Tied Double-Triple Gate MOSFET"
T. Park (Seoul National Univ., Korea)
"Ge and SiGe MOS Devices" (tentative)
K. Saraswat (Stanford Univ., USA)

Area 3

Silicon Process/Materials Technologies

(Chair, N. Kobayashi, Selete)

The session consists of advanced process and materials technologies for Si ULSI applications. Strongly encouraged are the topics of material innovations to

improve device performance, manufacturability, and cost-efficiency. Papers are solicited in, but not limited to, the following areas: (1) Novel materials technologies such as high-k, ultra-low-k insulators and metal gates to break through the scaling limitations of CMOS Logic, Memory, and new-concept devices (2) Key materials and process technologies to integrate 65-90 nm Si ULSIs such as shallow junction and strained-Si processes (3) Reliability of FEOL and BEOL processes for high-yield manufacturing.

Invited speakers:
"Interconnect Application of Carbon Nanotube
Y. Awano (Fujitsu Labs., Japan)
"Stress Migration Phenomena of Copper Interconnect"
J. Koike (Tohoku Univ., Japan)
"Integrating Diffusionless Anneals into 45nm CMOS"
R. Lindsay (IMEC, Belgium)
"Electrical Characterization of High-k Gated MOSFETs and Interfaces"
T. P. Ma (Yale Univ., USA)

Area 4

Silicon-on-Insulator Technologies

(Chair, A. Ogura, NEC)

SOI devices are now commercially available. Simultaneously, SOI is recognized as a basic structure to realize future advanced devices such as patterned SOI, SON (Si on nothing), FinFET, SGOI (SiGe on insulator) and SSOI (strained-Si on insulator), and so on. This subcommittee covers the whole field of SOI and SOI-related new technologies in a wide range of interests from circuit design to material issues. The topics will include, but not be limited to: (1) SOI Circuit Technology and LSI Applications (High Speed, Low Power Consumption, RF, Analog/Linear, etc), (2) New Structure Devices (Double, Triple, Quadruple Gate, FinFET, Vertical Channel, Quantum, Strained Channel, Multi-Layer Devices, etc.), (3) Process Issues for Device Manufacturing (Isolation, Silicidation, Metal Gate, Plasma Damage, etc), (4) Physics and Modeling of SOI Device/Process and Circuits (floating-body effect, self-heating, etc), (5) SOI Materials Characterization and Manufacturing, and (6) Reliability Issues (Hot Carrier Injection, GOI, Radiation Effects, ESD, etc).

Invited speakers:
"SOI Floating Body Memories for Embedded Memory Applications"
P. Fazan (Innovative Silicon S.A., Switzerland)
"Development of SGOI and sSOI for High Volume Manufacturing"
C. Mazure (SOITEC, France)
"Fully Depleted SOI Technology for Ultra-Low Power Application"
F. Ichikawa (Oki Electric, Japan)
"SOI Transistor/Power Scaling and Scaling-Strengthened Strain"
F.L. Yang (TSMC, Taiwan)

Area 5

New Materials and Characterization for Silicon LSIs

(Chair, S. Takagi, Univ. of Tokyo)

Introduction and utilization of new materials are expected as a key concept for further evolution and functionarization of Si-based logic and memory LSIs. Also, novel characterization techniques are indispensable in realizing these advance devices. Papers are solicited in the following areas (but not limited to these subjects): (1) Characterization and processing of group-IV semiconductors, high-k and low-k dielectrics and other new materials, including diamond, silicides (germanides), nano-tubes, fullerene and any other materials applicable to Si-based LSIs, (2) Physics and chemistry of surface and interface phenomena (including oxidation and nitridation), (3) Reliability physics and failure analysis of gate oxides and interconnect systems, (4) New characterization method for devices and materials including in-situ monitoring and nanometer-scale characterization. Submission of papers at a germinal stage is also encouraged.

Invited speakers:
"Reliability Issues on High k Gate Dielectrics"
R. Degraeve (IMEC, Belgium)
"To be announced"
J.C. Sturm (Princeton Univ.)
"Nanoelectronic Scaling Tradeoffs: What Does Materials Physics Have to Say?"
V. Zhirnov (SRC, USA)

Area 6

Compound Semiconductor Materials and Devices

(Chair, K. Kojima, Mitsubishi Electric)

Compound semiconductors are the key materials supporting the highly information oriented society. This area deals with III-V, II-VI compound semiconductors including wide gap GaN and ZnO, and magnetic semiconductors. The materials also includes other compound semiconductors such as SiC, FeSi2 and so on. Compound Semiconductor Materials and Devices besides covers the following areas (but not limited): (1) Growth and characterization, (2) Heterostructures and superlattices, (3) Optical devices (LEDs, LDs and detectors) and electron devices (HFETs and HBTs), their device processing and reliability.

Invited speakers:

"InGaAs Based Quantum Wells for Ultrafast All-Optical Switches Using Intersubband Transitions"

T. Mozume (FESTA, Japan)

"Diamond MISFETs for High Frequency Applications"

H. Umezawa (Waseda Univ., Japan)

Area 7

Optoelectronic Devices and Photonic Crystal Devices

(Chair, O. Wada, Kobe Univ.)

Towards ubiquitous communication and computing, optoelectronic devices are expected to explore novel functions and enhance performance by utilizing novel device physics and developing advanced fabrication techniques. The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices, which includes (1) Laser diodes, LEDs, photodetectors, SOAs, and OEICs, (2) Photonic crystal materials and novel functional devices, (3) Optical switches, modulators, and MEMS, (4) Optical wavelength converters, nonlinear optical devices, and all-optical switches, (5) Waveguide components, PLCs and integrated photonic circuts, (6) Material and device processing and characterization techniques, (7) Hybrid and monolithic integration, packaging and moduling, and (8) Optical communication, interconnection and signal processing applications of optoelectronic and photonic devices.

Invited speakers:

"All-Optical Signal Processing Based on Ultrafast Nonlinearities in Semiconductor Optical Amplifiers"

H.J.S. Dorren (Eindhoven Univ. of Technology, Netherlands)
"PBG Resonators and Waveguides in Photonic Crystal Slabs"
M. Notomi (NTT, Japan)
"Photonic Band Fiber and Fiber Based Devices; Design and Fabrication"
M. Ogai and D.J. Trevor (OFS Fitel Labs., USA)
"InGaAsN as a Material for Novel Long-wavelength Lasers"
H. Riechert (Infineon Technologies, Germany)
"Quantum Dot SOAs for Optical Signal Processing"
M. Sugawara (Univ. of Tokyo, Japan)
"All-Optical Devices for Nx160Gb/s DWDM/OTDM Transmission Systems-"
A. Suzuki (FESTA, Japan)

Area 8

Novel Devices, Physics and Fabrication

(Chair, K. Ishibashi, RIKEN)

The aim of this subcommittee is to explore novel devices and physics, mainly in nanoscale, with inorganic and molecular materials. Papers are solicited in the following areas, but not limited to: (1) Quantum phenomena in nanoscale, (2) Quantum dots and single electron devices, (3) Solid state quantum computing, (4) Spintronics, (5) New nanoscale materials such as carbon nanotubes, (6) Molecular electronics, (7) Other novel devices such as small superconducting device and resonant tunneling device. (8) Nanofabrication, nanomechanics and characterization techniques in nanoscale.

Invited speakers:
"To be announced"
M. Fuhrer (Univ. of Maryland)
"Solid-Electrolyte Nanometer Switch Implemented in Si LSI"
T. Sakamoto (NEC, Japan)

Area 9

Quantum Nanostructure Devices and Physics

(Chair, Y. Hirayama, NTT)

The field covers recent progress in physics, fabrication, characterization and device applications of nanostructures. The main topics includes (1) Growth and processing of quantum dots and nanostructures. (2) Transport/optical

properties and THz/Femto-second dynamics (3) Nanometer-scale characterization such as SPM and SNOM (4) Nano electronic/optical devices (5) Novel nanostructures and nanomaterials such as photonic crystals and magnetic nanostructures. (6) Spin and carrier control in quantum nanostructures.

Invited speakers:
"Coherent Manipulation of Electronic States in Double Quantum Dots"
T. Fujisawa (NTT, Japan)
"Nanostructure Formation Using Self-Assembled and Patterned Processes"
D.L. Huffaker (Univ. of New Mexico, USA)
"Integrated Nanoscale Mechanics and Electronics"
R. Knobel (Queen's Univ. Canada)
"Light-Emitting Diodes Based on InP Quantum Dots in GaP"
W.T. Masselink (Humboldt Univ. Berlin, Germany)

Area 10

Non-Volatile Memory Technologies

(Chair, T. Kobayashi, Hitachi)

"Non-Volatile Memory Technologies" session solicits all NV memory (Flash, MONOS, FeRAM, MRAM, Phase Change, Nanocrystal, Anti-fuse, and others) technology related papers. Topics relating to NV devices include cell device physics and characterization, processing and materials, tunnel dielectrics, ferroelectric materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, integrated circuits, new concept technologies, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited speakers:
"Recent Development and Applications of FeRAM"
T. Kijima (Seiko Epson, Japan)
"Recent Development in Phase Change Memory"
R. Bez (ST Microelectronics, Italy)
"Future Trends in NAND-Type Flash Memory"
R. Shirota (Toshiba, Japan)

Area 11

SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

(Chair N. Suematsu, Mitsubishi Electric)

Compound-semiconductor devices are playing important roles in wireless and optical communications systems. Future communications systems definitely require devices and circuits that dissipate lower energy, operate at higher bit rates or frequencies, have lower noise, generate higher signal power, and are more compact. This session covers advanced device and IC technologies that meet these challenges through the use of SiGe, GaAs-based, InP-based, and GaN-based materials (but not limited). Monolithic ICs or multi-chip modules integrating optical and electrical devices will also be discussed. Papers demonstrating breakthroughs and novel concepts, discussing on potentials and limitations, and addressing issues in these technologies are strongly solicited for this session.

Invited speakers:
"Challenges to Achieve THz SiGe HBTs"
G. Freeman (IBM, USA)
"Recent Developments in Photonic and mm-Wave"
S. Iezekiel (Univ. of Leeds, UK)
"An Over 100W GaN-HEMT High Power Transmitter Amplifier for Wireless Base Station with High Reliability"
T. Kikkawa (Fujitsu Labs., Japan)

Area 12

System-Level Integration and Packaging Technologies

(Chair, K. Takahashi, ASET)

The scope of this subcommittee involves all features of advanced packaging technologies and system-level integration technologies based on packaging technology. Papers are solicited in, but not limited to, the following areas: (1) Advanced packaging technologies including chip size package (CSP), wafer-level package, stacked package, (2) Three-dimensional (3D) integration technology including wafer stacking and chip stacking, (3) Advanced interconnection technologies such as optical, wireless, capacitive and inductive interconnections, (4) System integration technologies including SiP (system-in-package), SoP (system-on-package), opto-electronics and MEMS integration, (5) Modeling and simulation of thermal, mechanical and electrical performance of advanced packaging and system integration, (6) Design and CAD technologies for the advanced packaging and system integration including interface design, EMI and

EMC management and ultra-high speed data transfer technologies, (7)Testing technologies for the system integration including burn-in, known good die (KDG) and design for test (DFT).

Invited speakers:
"Wafer Level Package Integrated Functions"
G. Carchon (IMEC, Belgium)
"System Integration Technology of LSI"
H. Kawamoto (FAIS, Japan)
"To be announced"
L. Schaper (Univ. of Arkansas, USA)

Area 13

Organic Semiconductor Devices and Materials

(Chair, M. Iwamoto, Tokyo Tech)

Electronic and Optical processes in organic materials and device application in the following fields (but not limited): (1) Organic transistors, diodes and circuits, (2) Organic light emitting devices, (3) Organic photodetectors and photovoltaic devices, (4) Chemical sensors and gas sensors, (5) Fabrication and characterization of organic thin films, (6) Electrical and Optical properties of organic thin film and materials, (7) Organic-inorganic hybrid systems, (8) Molecular electronics, (9) Interfacial phenomena, LC devices, etc.

Invited speakers:
"Research and Development of Organic Electro-luminescent Devices and Application for Plastic Information Devices"
Y. Ohmori (Osaka Univ., Japan)
"Development of Conducting Polymers toward Molecular Elecronics"
Y. W. Park (Seoul National Univ., Korea)

Area 14

Micro/Nano Electromechanical Devices for Bio- and Chemical Applications

(Chair, Y. Miyahara, National Inst. for Materials Science)

Micro/nano electromechanical devices (M/NEMS) are now widely applied to biochemical, medical and environmental fields and a new research field called microTAS or Lab. on a Chip is expanding and being established. Fusion of microelectronic devices with

materials and methods in the chemical, biological, and medical fields is expected to open up new scientific and business fields. Papers are solicited in the following areas (but not limited): (1) Micro/nano electronic mechanical systems (M/NEMS) for RF, optical, power and others, (2) microTAS and Lab on a chip, (3) Various Bio-chips for DNA, healthcare and proteins, (4) Fabrication technologies and (5) New integrated micro/nano systems for biochemical and medical applications.

Invited speakers:
"Integrated Sensors and Systems"
D.R.S. Cumming (Univ. of Glasgow, UK)
"Micro-Nano Electromechanical Devices for Bio- and Chemical Applications"
T. Mitsui (Harvard Univ., USA)

RUMP SESSIONS

The following two Rump Sessions are planned on September 16th (Thursday).

Session A

"Why Don't You Enjoy High-k Science?"
Organizer:
A. Toriumi (Univ. of Tokyo, Japan)
Moderator:
A. Nishiyama (Toshiba, Japan)
A. Toriumi (Univ. of Tokyo, Japan)

High-k materials have been tackled for scaled CMOS applications. Although the recent progress is remarkable, most of the problems in the high-k gate stack technology seem to be based on the fundamental material science of high-k dielectrics. If it is the case, the technology tunings or improvements will be in vain or take us a long time to the final success. On the other hand, high-k materials have a number of interesting subjects for studying. The static and dynamic motions of atoms and electrons to the electric field in the highly ionic oxides, the interface properties at ionic/non-ionic films, or the nanometer characteristics of ionic films, are examples for research. In addition, glass science, electrochemical cell or Schottky barrier formation mechanism will also be included in the high-k research. Those items will directly or indirectly be related with CMOS applications, but we would propose two engagements in the rump session. 1) Forget about

technology node of ITRS, and then 2) focus on extracting an essence of high-k materials science.
You might hopefully catch something for breaking through the technology hardships on the way to your home after the rump session. Take a short cut way to the success with material science of high-k dielectrics.

Session B
"Challenges of Spintronics: from basic physics to nanoscale devices"
Organizer:
Y. Hirayama (NTT, Japan)
Moderator:
Y. Hirayama (NTT, Japan)
H. Munekata (Tokyo Tech, Japan)

Recent progress in spintronics is brilliant. Many interesting topics, such as new spintronics devices based on metal and semiconductor nanostructures, spin control in semiconductors and its application to optical and electrical devices, and coherent control of spin for future quantum information processing, have been developed in spintronics.
In this rump session we will discuss these fascinating aspects of spintronics including the control of nuclear spin in solid-state systems. Our intention is to highlight the present status, remaining problems and future dreams of spintronics from viewpoints of basic physics and device applications.

SHORT COURSE
Short Course entitled "The Latest JISSO Technology for SiP Solutions" will be held on Tuesday, September 14. All lectures are given in Japanese.

SUBMISSION OF PAPERS
Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at http://www.ssdm.jp.
Please note that submissions by post will NOT be accepted.

Deadline for Submission is May 10, 2004.

The two-page paper must be prepared in English in 8.5-×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. The second page should be used to indicate figures, tables and photographs. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean etc. fonts cannot be used for both figures and texts. The paper should report original, previously unpublished work, including specific results.

Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed without opportunity for further revision in the extended abstracts, which will be distributed to conference participants during the conference.

Authors of papers accepted for presentation at SSDM 2004 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2005.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract for review to the committee, the author(s) agrees that the work will not be published prior to the presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

Late News Paper Deadline is July 25, 2004.

Notices of acceptance will be e-mailed by mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include a plenary session, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 1998.

SSDM Paper Award

Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.

An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF) which is one of the cooperative organizations.

BANQUET

A buffet dinner will be held in the evening on September 15. Additional tickets may be purchased at the registration

desk for ¥7,000 each.

REGISTRATION

Participants may register for the conference at the web site beginning in June.

The registration and banquet fees are:

	Registration Fee		Short Course (in Japanese)	Banquet
	On or before August 14	After August 14		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Guest(s)				¥4,000/person

VISA REQUIREMENT

All foreign participants must have a valid passport. Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or consulate as soon as possible.
Concerning visa applications, generally, in applying for a visa each applicant is requested to submit the documents listed below:
(1) an invitation letter (an optional document written in English)
(2) a letter of guarantee (written in Japanese)
(3) documents certifying the purpose of the visit (written in Japanese)
(4) the applicant's schedule in Japan (written in Japanese)

Please ask the nearest Japanese Embassy to make sure what documents are required to obtain a visa first, and then, please contact the SSDM Secretariat. The Secretariat will send the Reply Form for Visa Application in order to obtain the required documents. Please complete the Reply Form for Visa Application and submit it to the secretariat. We will send you all the requested documents as soon as we receive the Reply Form.

LOCATION

Opened in March 1999, Tower Hall Funabori is a landmark facility in Edogawa ward. Edogawa ward is an historic and cultural center in Tokyo, located adjacent to the business and coastal areas of Tokyo.
The building combines an ability to: hold conventions

where people can meet, interact and share information; achieve qualitative improvements in vital policy areas of the ward such as health, culture and industry; provide amusement and relaxation to visitors through films, exhibitions, cuisine, and more.
The building's purpose is to achieve a truly enriching lifestyle for residents of the ward, a lifestyle in which working, living, playing and studying are skillfully blended.
For further information (*Japanese only), see
http://www.city.edogawa.tokyo.jp/shisetsu/bunka/bunka1.html

OFFICIAL TRAVEL AGENT

JTB Corp.
Yokohama Group Tours Office
6F, 3-29-1 Tsuruya-cho, Kanagawa-ku,
Yokohama 221-0835 Japan
Fax: +81-45-316-5703
Phone: +81-45-316-4602
E-mail: danyoko9@mnm.jtb.co.jp

Hotel accommodations

JTB has blocked rooms at following hotels in Tokyo for the conference period. Reservations can be made through the conference website beginning in April. If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

Application and payment

Participants wishing to reserve hotel accommodations should access the Accommodation page of the conference website. The page will open in early April and reservations should be made by no later than August 20, 2004. (Confirmation sheet will be sent by JTB.)
Application should be accompanied by a remittance covering the total accommodation fee plus handling fee ¥525 due JTB.

No reservation will be confirmed in the absence of this payment. All payment must be in Japanese yen. If the remitter's name is different from the participant's name, or if the amount covers more than one person, please inform us of the details for the payment.

No.	Hotel Name (Check-in & Check-out time)	Room Rates (per person, per night)		Address Phone Nearest Station Access to the Site
		Single	Twin	
1	Hotel Grand Palace (12:00/12:00)	*¥15,115	¥8,085	1-1-1, Iidabashi, Chiyoda-ku, Tokyo +81-3-3264-1111 1 min.walk to Subway Toei Shinjuku Line Kudanshita Sta. 30 min. by Subway & walk to the site.
2	Tokyo Marriott Hotel Kinshicho Tobu (14:00/11:00)	¥11,125	¥8,925	1-2-2, Kinshi, Sumida-ku, Tokyo +81-3-5611-5511 3 min. walk to Subway Hanzomon Line Kinshicho Sta. 20 min. by subway & walk to the site.
3	Hotel Park Lane Nishikasai (14:00/10:00)	¥7,875	¥7,350	6-17-9, Nishikasai, Edogawa-ku, Tokyo +81-3-3675-8900 2 min. walk to Tozai Line Nishikasai Sta. 20 min. by Local Bus & walk to the site.
4	Mizue Daiichi Hotel (15:00/10:00)	¥7,035	¥6,300	2-6-16, Mizue, Edogawa-ku, Tokyo +81-3-5243-8000 1 min. walk to Toei Shinjuku Line Mizue Sta. 10 min. by train & walk to the site.
5	Toyoko inn Tozaisen Nishikasai (16:00/10:00)	¥6,500		5-11-12, Nishikasai, Edogawa-ku, Tokyo +81-3-5676-1045 1 min. walk to Tozai Line Nishikasai Sta. 20 min. by Local Bus & walk to the site.
6	Hotel Seaside Edogawa (**Japanese Style Room**) (14:00/10:00)	¥13,586	¥8,536 (Twin) ¥6,885 (Triple) ¥6,335 (Fourth)	6-2-2 Rinkai-cho, Edogawa-ku, Tokyo +81-3-3804-1180 3 min. walk to JR Keiyo Line Kasairinkaikoen Sta. (3 min. by train to Tokyo Disney Land) 40 min. by Local Bus & walk to the site.

Notes: Room rates include tax and service charge. Only #5, #6 hotels are including breakfast.
*Indicates single occupancy of a twin or double room

Payment should be in the form of:

- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. AMEX
- A bank transfer to JTB Corp. (Message: Ref:125772-002)
  Account at the Bank of Tokyo Mitsubishi, Yokohama Branch #480, 3-27-1 Honcho, Naka-ku, Yokohama-shi, Kanagawa 231-0005, Japan (Account number: 0043079)

Cancellation

In the event of cancellation, written notification should be sent to JTB. The following cancellation fees will be deducted before refunding.

Hotels: Up to 21 days before the arrival date---------
¥525
2 to 20 days before----------
20% of daily room charge (minimum ¥525)
1 day before----------
80% of daily room charge
On the day of arrival or no notice given----------
100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Tokyo is warm and sometimes humid in September. The temperature range is 18-30˚C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

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Persons in charge of online paper submission and registration:

K. Okada (Tokyo Tech)

A. Yamada (Tokyo Tech)

SECRETARIAT

c/o Inter Group Corp.
4-9-17, Akasaka, Minato-ku,
Tokyo 107-8486 Japan
TEL:+81-3-3479-5131
FAX:+81-3-3423-1601
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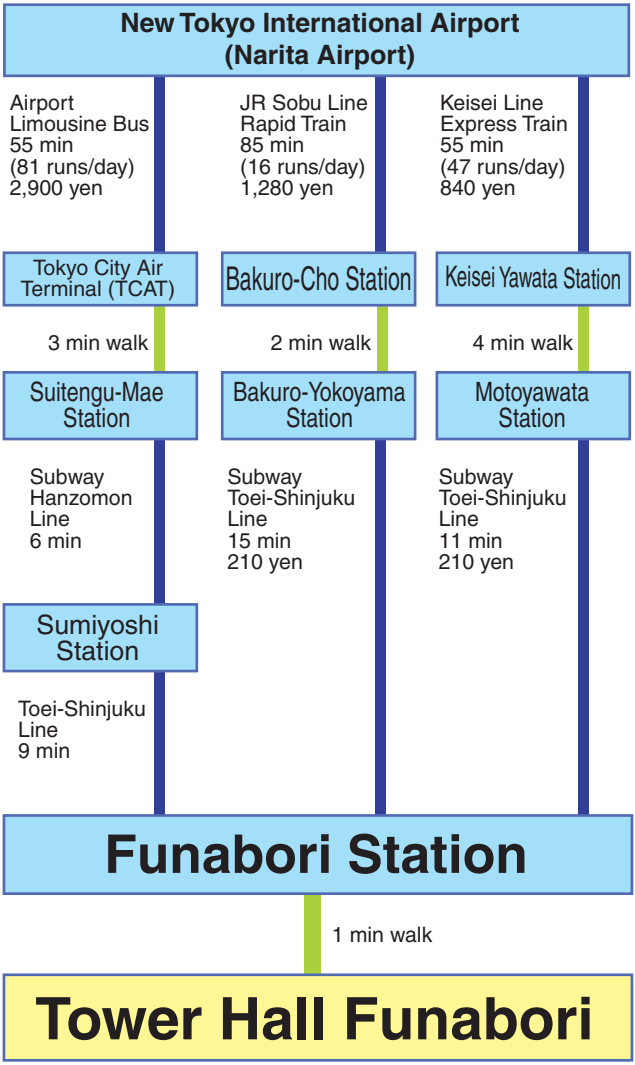

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