Advance Program Part II

LATE NEWS PAPERS

Thursday, September 16

Oral Session

Room C

18:00 C-6-4L Ultra-Shallow Junction Formation using Novel Plasma Doping Technology beyond 50 nm MOS Devices
W.-J. Cho, K. Im, C.-G. Ahn, J.-H. Yang, I.-B. Baek and S. Lee, Electronics and *Telecommunications Research Institute, Korea*

Room F

12:15 F-4-5L Layout dependence of RF CMOS performance on ultra-thin Si substrate
T. Ohguro, N. Sato, M. Matsuo, K. Kojima, H. Momose, K. Ishimaru and H. Ishiuchi, *Toshiba Corp., Japan*

Room G

12:15 G-4-4L 94-GHz f_T, 0.4-dB NF_{min} HBT with Optimized Si-cap and Extrinsic Base Using Blanket SiGeC Epitaxy for Consumer Wireless Applications
Y. Kiyota[1], H. Yamagata[2], M. Bairo[2], S. Yanagawa[2], T. Komoto[2], M. Oishi[2] and C. Arai[2],
[1]SONY Corp. and [2]SONY Semiconductor Kyusyu, Japan

Poster Session (13:15-15:00)

Exhibition Hall

P1: Advanced Silicon Circuits and Systems

P1-8L Ultra Low-energy Computing via Probabilistic Algorithms and Devices: CMOS Device Primitives and the Energy-Probability Relationship
S. Cheemavalagu, P. Korkmaz and K.V. Palem, *Georgia Institute of Technology, USA*

P2: Advanced Silicon Devices and Device Physics

P2-21L Design and Analysis of On-Chip Tapered Transformers for Silicon RFICs
M.H. Cho, G.W. Huang, C.S. Chiu, K.M. Chen and A.S. Peng, *National Nano Device Labs., Taiwan*

P3: Silicon Process/Materials Technologies

P3-21L Electrical characteristics of crystalline HfO_2 high-κ dielectric films deposited on crystalline γ-Al_2O_3 films
T. Okada[1], M. Shahjahan[2], K. Sawada[1] and M. Ishida[1], *[1]Toyohashi Univ. of Technology, Japan and [2]Rajshahi Univ., Bangladesh*

P3-22L Flat-band Voltage Tunability and No Depletion Effect of Poly-Si Gate CMOS with Nanometer-size Metal Dots at the Poly-Si/Dielectric Interface
H. Fujiwara[1], M. Kadoshima[1], K. Akiyama[1], N. Mise[1], S. Migita[2], H. Ota[2], M. Ohno[1], T. Nabatame[1], T. Horikawa[2] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*

P3-23L TDS measurement for low-k porous silica films incorporated with ethylene groups
Y. Uchida, Y. Maruya, T. Katoh, Y. Ito and K. Ishida, *Teikyo Univ. of Sci. & Tech., Japan*

P4: Silicon-on-Insulator Technologies

P4-9L Degradation of Low-Frequency Noise in PD SOI MOSFETs after Hot-Carrier stress
K.M. Chen[1], H.H. Hu[2], G.W. Huang[1] and C.Y. Chang[2], *[1]National Nano Device Labs. and [2]National Chiao Tung Univ., Taiwan*

P4-10L Modeling Geometry-Dependent Floating-Body Effect using Body-Source Built-In Potential Lowering for Scaled SOI CMOS
P. Su and W. Lee, *National Chiao Tung Univ., Taiwan*

P6: Compound Semiconductor Materials and Devices

P6-5L Nitride-based light emitting diodes with nanostructured silicon contact layers
C.H. Kuo[1] and S.J. Chang[2], *[1]South Epitaxy Corp. and [2]National Cheng Kung Univ., Taiwan*

P6-6L Near-Ultraviolet InGaN LEDs Grown on Patterned Sapphire Substrates
D.S. Wuu[1], W.K. Wang[1], W.C. Shih[2], J.S. Fang[2], C.E. Lee[1], W.Y. Lin1 and R.H. Horng[1], *[1]National Chung Hsing Univ. and [2]National Huwei Univ. of Science and Technology, Taiwan*

P6-7L Improvement in Performance of AlGaN/GaN HFETs by Utilizing a Low-Temperature GaN Cap Layer
E. Waki[1], T. Deguchi[1], S. Ono[1], A. Nakagawa[1], H. Ishikawa[2] and T. Egawa[2], *[1]New Japan Radio Co., Ltd. and [2]Nagoya Institute of Technology, Japan*

P7: Optoelectronic Devices and Photonic Crystal Devices

P7-14L Optical Responsivity Enhanced InGaAs/InP Heterojunction Phototransistor Arrays
Y.C. Jo[1], S.J. Joe[2], H. Kim[1] and P. Choi[3], *[1]KETI, [2]KAIST and [3]Kyungpook National Univ., Korea*

P7-15L Feasibility Study on Self-Collimated Light-Focusing Device Using 2-D Photonic Crystal with a Parallelogram Lattice
Y. Ogawa, Y. Iida and Y. Omura, *Kansai Univ., Japan*

P7-16L The annealing temperature effects on the synthesis of n-TiO_2/dye/p-CuI solid state solar cells
M. Rusop, T. Shirata, T. Soga and T. Jimbo, *Nagoya Institute of Technology, Japan*

P8: Novel Devices, Physics and Fabrication

P8-10L Fluoride Resonant Tunneling Diodes on Si Substrates Improved by the Additional Thermal Oxidation Process
S. Watanabe, M. Maeda, T. Sugisaki and K. Tsutsui, *Tokyo Tech, Japan*

P8-11L Spectrum of plasma oscillations in a slot diode with a two-dimensional electron channel
A. Satou[1], I. Khmyrova[1], A. Chaplik[1,2] V. Ryzhii[1] and M. Shur[3], *[1]Univ. of Aizu, Japan, [2]Institute of Semiconductor Physics, Russia and [3]Rensselaer Polytechnic Institute, USA*

P8-12L Impact of Drain Induced Barrier Lowering on Read Scheme in Silicon Nanocrystal Memory with Two-Bitper-Cell Operation
S. Park[1, 2], H. Im[2], I. Kim[1] and T. Hiramoto[1], *[1]Univ. of Tokyo, Japan and [2]Univ. of Dongguk, Korea*

P9: Quantum Nanostructure Devices and Physics

P9-13L Diminished nonradiative recombination in near-surface pseudomorphic $Si_{1-x}Ge_x$/Si quantum wells
Y. Sugawara[1,2], Y. Kishimoto[2], Y. Akai[2] and S. Fukatsu[1,2], *[1]Japan Science and Technology Agency and [2]Univ. of Tokyo, Japan*

P9-14L Magnetic Force Microscope Using Carbon Nanotube Probes
T. Manago[1], H. Kuramochi[1,2], T. Uzumaki[1,3], M. Yasutake[1,2], A. Tanaka[1,3], H. Akinaga[1] and H. Yokoyama[1], *[1]National Institute of Advanced Industrial Science and Technology (AIST), [2]SII NanoTechnology and [3]Fujitsu Ltd., Japan*

P11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

P11-6L Enhancement of breakdown voltage in AlGaN/GaN HEMTs using AlN buffer layer thickness on 4-inch Silicon
S. Arulkumaran, T. Egawa and H. Ishikawa, *Nagoya Institute of Technology, Japan*

P11-7L Design and Fabrication of Packaged Wideband Transimpedance Amplifier by using InGaAs/InP HBT Technology
J.M. Lee, S.I. Kim, B.G. Min, C.W. Ju and K.H. Lee, *Electronics and Telecommunications Research Institute, Korea*

P13: Organic Semiconductor Devices and Materials

P13-12L Model of Electrodiffusion of Metals in Fullerene Thin Films
B.P. Kafle, I. Rubinstein and E.A. Katz, *Ben-Gurion Univ. of the Negev, Israel*

P13-13L Semi-Transparent Organic Photo Detectors Utilizing a Sputter Deposited Indium Tin Oxide for a Top Contact Electrode
T. Morimune, H. Kajii and Y. Ohmori, *Osaka Univ., Japan*

P13-14L The physical and micro structural properties of PECVD grown amorphous carbon films on the contribution to n-C:P/p-Si solar cells
M. Rusop, H. Ebisu, M. Adachi, T. Soga and T. Jimbo, *Nagoya Institute of Technology, Japan*

Friday, September 17

Oral Session

Room A

10:15 A-7-4L Effect of Strain on Static and Dynamic NBTI of pMOSFETs
H.N. Lin[1], H.C. Lin[2], T.Y. Huang[1], C.H. Ko[3], C.H. Ge[3], C.C. Lin[3] and C.C. Huang[2], *[1]National Chiao-Tung Univ., [2]National Nano Device Labs. and [3]Taiwan Semiconductor Manufacturing Company, Taiwan*

Room C

11:45 C-8-4L Double Gate SOI MOSFET - Considerations for Improved Cut-off Frequency
A. Kranti, T.M. Chung and J.P. Raskin, *Univ. catholique de Louvain, Belgium.*

Room F

11:45 F-8-5L Accumulated Carrier Density Dependence of Pentacene TFT Mobility Determined by Split C-V Technique
T. Yokoyama, T. Nishimura, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

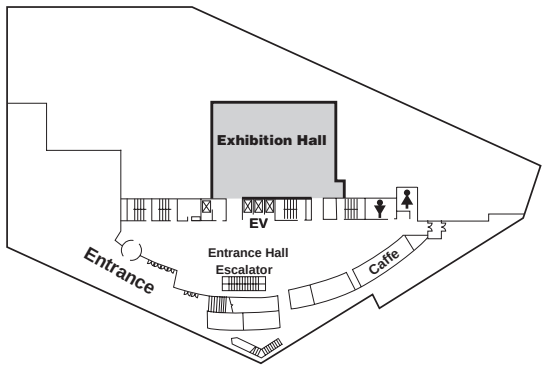
15:45 F-10-2L Low Temperature Solution Processed SiO_2 Insulator Thin Films for Organic FET
T. Kodzasa, M. Yoshida, S. Uemura, S. Hoshino and T. Kamata, *National Institute of Advanced Industrial Science and Technology, Japan*

UPDATED INFORMATION

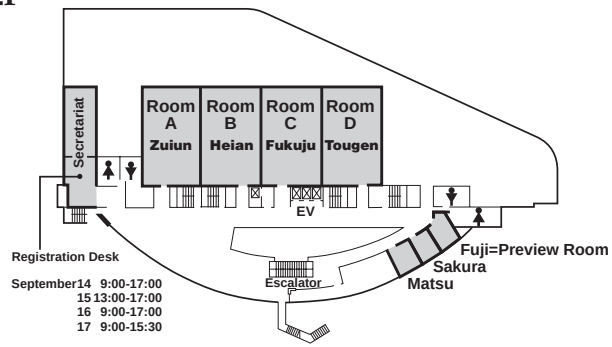
A-3-4 Phosphorescence Decay Time of Ir (ppy)$_3$ in Tetrahydrofuran at Magnetic Field
⇩
P-13-11 T. Tsuboi and N. Aljaloudi, *Kyoto Sangyo Univ., Japan*

Floor Map

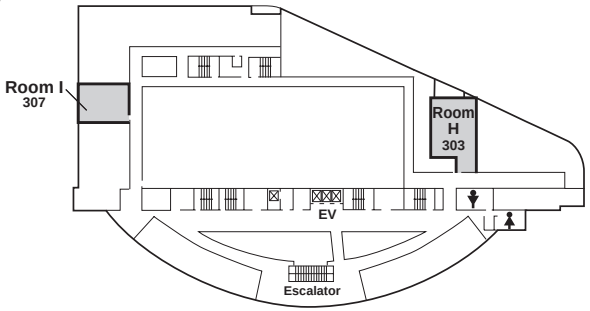
1F



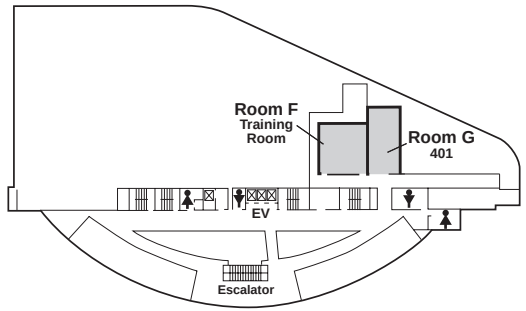
2F



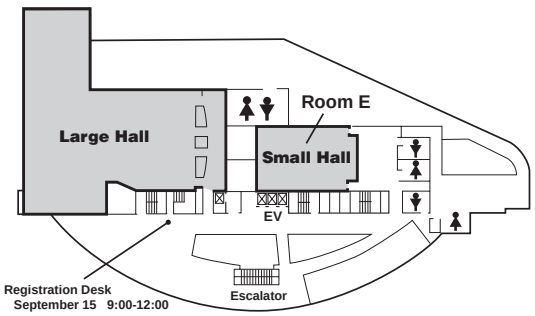
3F



4F



5F



SSDM 2004 Time Table

Wednesday, September 15

LARGE HALL

10:00-12:30 PL: Opening Session

Room A	Room B	Room C	Room D	Room E	Room F	Room H	Room I
14:00-16:00 **Area 2: Advanced Silicon Devices and Device Physics** A-1: Advanced Devices I	**14:00-15:50** **Area 3: Silicon Process/Materials Technologies** B-1: High-K Gate Dielectric I		**14:00-15:50** **Area 10: Non-Volatile Memory Technologies** D-1: Non-Volatile Memory Technologies I	**14:00-15:50** **Area 5: New Materials and Characterization for Silicon LSIs** E-1: Nano Materials & Characterization	**14:00-16:00** **Area 6: Compound Semiconductor Materials and Devices** F-1: Optical Devices	**14:00-16:00** **Area 8: Novel Devices, Physics and Fabrication** H-1: Nanoelectronics and Nanodevices	**14:00-15:50** **Area 1: Advanced Silicon Circuits and Systems** I-1: High Speed Digital
16:15-18:15 **Area 2: Advanced Silicon Devices and Device Physics** A-2: High-K Dielectrics/Metal Gate Stack	**16:15-18:15** **Area 3: Silicon Process/Materials Technologies** B-2: Interconnect			**16:15-18:05** **Area 5: New Materials and Characterization for Silicon LSIs** E-2: High-K Reliability	**16:15-18:15** **Area 6: Compound Semiconductor Materials and Devices** F-2: III-V Electronic Devices	**16:15-18:15** **Area 8: Novel Devices, Physics and Fabrication** H-2: Si Nanodevices	**16:15-17:45** **Area 1: Advanced Silicon Circuits and Systems** I-2: Low Power Analog
		18:30-20:30 Banquet					

Thursday, September 16

Room A	Room B	Room C	Room D	Room F	Room G	Room H	Room I
9:15-10:45 **Area 13: Organic Semiconductor Devices and Materials** A-3: Organic LED I	**9:15-10:45** **Area 3: Silicon Process/Materials Technologies** B-3: Silicide & Junction	**9:15-10:35** **Area 5: New Materials and Characterization for Silicon LSIs** C-3: Gate Dielectrics Characterization I	**9:15-10:45** **Area 10: Non-Volatile Memory Technologies** D-3: Non-Volatile Memory Technologies II	**9:15-10:45** **Area 12: System-Level Integration and Packaging Technologies** F-3: 3D&Interconnect	**9:15-11:00** **Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** G-3: High Speed and Photonic Devices and IC's	**9:15-10:45** **Area 8: Novel Devices, Physics and Fabrication** H-3: Novel Devices and Characterization	
11:00-12:30 **Area 13: Organic Semiconductor Devices and Materials** A-4: Organic LED II	**11:00-12:20** **Area 2: Advanced Silicon Devices and Device Physics** B-4: Advanced Memory Technology	**11:00-12:30** **Area 5: New Materials and Characterization for Silicon LSIs** C-4: Strained Si/SiGe/Ge Devices & Materials	**11:00-12:30** **Area 10: Non-Volatile Memory Technologies** D-4: Non-Volatile Memory Technologies III	**11:00-12:15** **Area 12: System-Level Integration and Packaging Technologies** F-4: Wafer Level Integration	**11:15-12:00** **Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** G-4: GaN Devices and their	**11:00-12:30** **Area 8: Novel Devices, Physics and Fabrication** H-4: Nanowires and Nanotubes	**11:00-12:15** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-4: N/MEMS for Bio-and Chemical Applications I
13:15-15:00 Poster Session (Exhibition Hall)							
15:15 -16:30 **Area 2: Advanced Silicon Devices and Device Physics** A-5: Novel Device and Sensors	**15:15-16:35** **Area 3: Silicon Process/Materials Technologies** B-5: Metal Gate Electrode	**15:15-16:35** **Area 4: Silicon-on-Insulator Technologies** C-5: SOI-Device Applications	**15:15-16:30** **Area 6: Compound Semiconductor Materials and Devices** D-5: GaN Electronic Devices I	**15:15-16:45** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** F-5: Photonic Crystal Fibers and Devices		**15:15-16:35** **Area 1: Advanced Silicon Circuits and Systems** H-5: Image Sensing and Processing	**15:15-16:30** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-5: N/MEMS for Bio-and Chemical Applications II
	17:00-18:20 **Area 3: Silicon Process/Materials Technologies** B-6: Advanced Process	**17:00-18:00** **Area 4: Silicon-on-Insulator Technologies** C-6: SOI-Device Characterization	**17:00-18:00** **Area 6: Compound Semiconductor Materials and Devices** D-6: GaN Electronic Devices II	**17:00-18:15** **Area 12: System-Level Integration and Packaging Technologies** F-6: System in Package		**17:00-18:00** **Area 1: Advanced Silicon Circuits and Systems** H-6: Memory Cicuits	**17:00-18:00** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-6: N/MEMS for Bio-and Chemical Applications III

18:30-20:30 Rump Session
Room A "Why don't you enjoy High-K Science?"
Room B "Challenges of Spintronics: from basic physics to nanoscale devices"

Friday, September 17

Room A	Room B	Room C	Room D	Room F	Room G	Room H	Room I
9:15-10:35 **Area 2: Advanced Silicon Devices and Device Physics** A-7: Advanced Gate Stack and DRAM	**9:15-10:15** **Area 3: Silicon Process/Materials Technologies** B-7: High-K Gate Dielectric II	**9:15-10:35** **Area 4: Silicon-on-Insulator Technologies** C-7: SOI-Strained Technology	**9:15-10:30** **Area 6: Compound Semiconductor Materials and Devices** D-7: GaN-Optical Devices	**9:15-10:30** **Area 13: Organic Semiconductor Devices and Materials** F-7: Molecular Electronics	**9:15-10:30** **Area 9: Quantum Nanostructure Devices and Physics** G-7: Fabrication and Characterization	**9:15-10:30** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-7: Quantum Effect Photonic Devices	
10:45-12:05 **Area 2: Advanced Silicon Devices and Device Physics** A-8: Advanced Devices II	**10:45-12:25** **Area 3: Silicon Process/Materials Technologies** B-8: High-K Gate Dielectric III	**10:45-12:05** **Area 4: Silicon-on-Insulator Technologies** C-8: SOI-Materials	**10:45-12:15** **Area 6: Compound Semiconductor Materials and Devices** D-8: GaN-Crystal Growth	**10:45-12:15** **Area 13: Organic Semiconductor Devices and Materials** F-8: Organic Electronics	**10:45-12:15** **Area 9: Quantum Nanostructure Devices and Physics** G-8: Quantum Devices and Circuits	**10:45-12:15** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-8: All-Optical Signal Processing	
13:45-15:05 **Area 2: Advanced Silicon Devices and Device Physics** A-9: Nanoscale Device Physics	**13:45-15:05** **Area 3: Silicon Process/Materials Technologies** B-9: DRAM	**13:45-15:05** **Area 5: New Materials and Characterization for Silicon LSIs** C-9: Gate Dielectrics Characterization II	**13:45-15:15** **Area 6: Compound Semiconductor Materials and Devices** D-9: Fe-Si	**13:45-15:15** **Area 13: Organic Semiconductor Devices and Materials** F-9: Organic FET I	**13:45-15:15** **Area 9: Quantum Nanostructure Devices and Physics** G-9: Control of Quantum State	**13:45-15:15** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-9: Semiconductor Lasers	
15:30-16:50 **Area 2: Advanced Silicon Devices and Device Physics** A-10: Analog Devices and Compact Modeling	**15:30-16:50** **Area 4: Silicon-on-Insulator Technologies** B-10: SOI-3D Structure	**15:30-16:30** **Area 5: New Materials and Characterization for Silicon LSIs** C-10: High-K Dielectrics	**15:30-16:45** **Area 6: Compound Semiconductor Materials and Devices** D-10: Wide-Gap Materials	**15:30-16:15** **Area 13: Organic Semiconductor Devices and Materials** F-10: Organic FET II	**15:30-16:45** **Area 9: Quantum Nanostructure Devices and Physics** G-10: Quantum Dots	**15:30-16:45** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-10: Optical Filters and Detectors	

SSDM 2004 Chairpersons List

	Large Hall
	PL: (10:00-12:30) K. Masu (Tokyo Tech) J. Sone (NEC)

	Room A	Room B	Room C	Room D	Room E	Room F	Room G	Room H	Room I
Wednesday,September 15	**A-1: (14:00-15:50)** K. Shibahara (Hiroshima Univ.) S. Inaba (Toshiba)	**B-1: (14:00-15:50)** M. Kubota (Matsushita Electric) F. Ohtsuka (SELETE)		**D-1: (14:00-15:50)** T. Nakamura (Rohm) Y. Shimada (Matsushita Electric)	**E-1: (14:00-15:50)** K. Kikuta (NEC) T. Kanayama (AIST)	**F-1: (14:00-16:00)** K. Ohtani (Tohoku Univ.) K. Kojima (Mitsubishi Electric)		**H-1: (14:00-16:00)** K. Ishibashi (RIKEN) J. Motohisa (Hokkaido Univ.)	**I-1: (14:00-15:50)** T. Kuroda (Keio Univ.) M. Takamiya (NEC)
	A-2: (16:15-18:15) Y. Momiyama (Fujitsu) C.C. Wu (TSMC)	**B-2: (16:15-18:15)** N. Kobayashi (SELETE) T. Nakamura (Fujitsu Labs.)			**E-2: (16:15-18:05)** J. Yugami (Renesas) M.Takayanagi (Toshiba)	**F-2: (16:15-18:15)** T. Takahashi (Fujitsu Labs.)		**H-2: (16:15-18:15)** M. Tabe (Shizuoka Univ.) D. K. Ferry (Arizona State Univ.)	**I-2: (16:15-17:45)** M. Takamiya (NEC) T. Kuroda (Keio Univ.)
Thursday, September 16	**A-3: (9:15-10:45)** M. Iwamoto (Tokyo Tech) H. Okada (Toyama Univ.)	**B-3: (9:15-10:45)** T. Noda (Matsushita Electric) S. Saito (NEC)	**C-3: (9:15-10:35)** H. Satake (ASET) R. Degraeve (IMEC)	**D-3: (9:15-10:45)** T. Nakanishi (Fujitsu Labs.) H. Takada (Mitsubishi Electric)		**F-3: (9:15-10:45)** K. Takahashi (ASET)	**G-3: (9:15-11:00)** N. Suematsu (Mitsubishi Electric) K. Oda (Hitachi)	**H-3: (9:15-10:45)** Y. Kuwahara (Osaka Univ.) Y. Miyamoto (Tokyo Tech)	
	A-4: (11:00-12:30) Y. Ohmori (Osaka Univ.) H. Usui (Tokyo Univ. of Agriculture and Technol.)	**B-4: (11:00-12:30)** S. Inaba (Toshiba) C.C. Wu (TSMC)	**C-4: (11:00-12:30)** J. Murota (Tohoku Univ.) A. Sakai (Nagoya Univ.)	**D-4: (11:00-12:30)** T. Kobayashi (Hitachi) K. Yoshikawa (Toshiba)		**F-4: (11:00-12:30)** T. Asano (Kyushu Inst. of Technol.) M. Kimura (Renesas)	**G-4: (11:15-12:30)** H. Miyamoto (NEC) K. Morizuka (Toshiba)	**H-4: (11:00-12:30)** K. Matsumoto (Osaka Univ.) Y. Homma (Tokyo Univ. Sci.)	**I-4: (11:00-12:15)** M. Kamahori (Hitachi) K. Shimoide (Asahi Kasei)
	A-5: (15:15-16:35) N. Sugii (Hitachi) H. Oda (Renesas)	**B-5: (15:15-16:35)** H. Kitajima (SELETE) K. Suguro (Toshiba)	**C-5: (15:15-16:35)** K. Inoh (Toshiba) M. Terauchi (Hiroshima City Univ.)	**D-5: (15:15-16:30)** H. Miyamoto (NEC) N. Maeda (NTT Photonics Labs.)		**F-5: (15:15-16:45)** H. Yamada (NEC) H. J. S. Dorren (Eindhoven Univ. of Technology)		**H-5: (15:15-16:35)** M. Fujishima (Univ. of Tokyo) M. Nagata (Kobe Univ.)	**I-5: (15:15-16:30)** H. Tabata (Osaka Univ.) T. Ichiki (Univ. of Tokyo)
		B-6: (17:00-18:20) M. Hori (Nagoya Univ.) T. Chikyo (NIMS)	**C-6: (17:00-18:15)** S. Okhonin (Innovative Silicon S.A.) Y. Kado (NTT)	**D-6: (17:00-18:00)** K. Kojima (Mitsubishi Electric)		**F-6: (17:00-18:15)** M. Aoyagi (AIST) H. Ezawa (Toshiba)		**H-6: (17:00-18:00)** Y. Kanno (Hitachi) M. Fujishima (Univ. of Tokyo)	**I-6: (17:00-18:00)** M. Sasaki (Tohoku Univ.) M. Sriyudthsak (Chulalongkorn Univ.)
Friday, September 17	**A-7: (9:15-10:30)** K. Takeuchi (NEC) Y. Momiyama (Fujitsu)	**B-7: (9:15-10:15)** Y. Tsunashima (Toshiba)	**C-7: (9:15-10:35)** O. Faynot (LETI) T. Iwamatsu (Renesas)	**D-7: (9:15-10:30)** M. Ikeda (Sony) K. Kojima (Mitsubishi Electric)		**F-7: (9:15-10:30)** M. Iwamoto (Tokyo Tech) H. Tada (Okazaki National Research Inst.)	**G-7: (9:15-10:30)** R. Noetzel (Eindhoven Univ. of Technol.) R. Knobel (Queen's Univ)	**H-7: (9:15-10:30)** H. Riechert (Infineon Technologies) N. Suzuki (Toshiba)	
	A-8: (10:45-12:15) N. Sugii (Hitachi) K. Kurimoto (Matsushita Electric)	**B-8: (10:45-12:25)** K. Eguchi (Toshiba) K.Torii (SELETE)	**C-8: (10:45-12:00)** C. Mazure (SOITEC) T. Nakai (Sumitomo Mitsubishi Silicon)	**D-8: (10:45-12:00)** T. Makimoto (NTT Basic Res. Labs.) T. Takahashi (Fujitsu Labs.)		**F-8: (10:45-12:15)** K. Kato (Niigata Univ.) A. Sugimura (Osaka Sangyo Univ.)	**G-8: (10:45-12:15)** P.V. Santos (Paul-Drude-Inst.) J. Motohisa (Hokkaido Univ.)	**H-8: (10:45-12:15)** S. Arahira (Oki Electric) T. Mizumoto (Tokyo Tech)	
	A-9: (13:45-15:15) M. Ogawa (Kobe Univ.) K. Kurimoto (Matsushita Electric)	**B-9: (13:45-15:05)** T. Kobayashi (Sony) I. Asano (Elpida)	**C-9: (13:45-15:05)** S. Miyazaki (Hiroshima Univ.) S. Takagi (Univ. of Tokyo)	**D-9: (13:45-15:15)** N. Kobayashi (Univ. of Electro-Communications) K. Ohtani (Tohoku Univ.)		**F-9: (13:45-15:15)** K. Kudo (Chiba Univ.) T. Someya (Univ. of Tokyo)	**G-9: (13:45-15:15)** W.T. Masselink (Humboldt Univ.) C. G. Smith (Cambridge Univ.)	**H-9: (13:45-15:15)** S. Matsuo (NTT Photonics Labs.) H. Shimizu (ATR International)	
	A-10: (15:30-16:30) H. Oda (Renesas) K. Takeuchi (NEC)	**B-10: (15:30-16:50)** A. Ogura (Meiji Univ.) H. Matsuhashi (Oki Electric)	**C-10: (15:30-16:30)** Y. Awano (Fujitsu Labs.) H. Watanabe (Osaka Univ.)	**D-10: (15:30-16:45)** Y. Horikoshi (Waseda Univ.) M. Ikeda (Sony)		**F-10: (15:30-16:15)** T. Kamata (AIST) T. Shimada (Univ. of Tokyo)	**G-10: (15:30-16:45)** D.L. Huffaker (Univ. of New Mexico) Y. Ohno (Tohoku Univ.)	**H-10: (15:30-16:45)** T. Nishimura (Mitsubishi Electric) S. Lee (Korea Inst. of Science and Technol.)	