SSDM 2003 Condensed Program

Tuesday, September 16

EMINENCE HALL

9:30 - 12:30 PL: Opening Session

Room A	Room B	Room C	Room D	Room E	Room F	Room G
14:00-15:50 **A-1: Advanced Silicon Devices and Device Physics** -Gate Stack Technologies- (5 papers)	**14:00-16:00** **B-1: Non-Volatile Memory Technologies** -Non-Volatile Memory I- (5 papers)	**14:00-15:50** **C-1: Silicon Process / Materials Technologies** -High-k Gate Dielectric I- (5 papers)	**14:00-16:00** **D-1: New Materials and Characterization** -Oxide Reliability and Surface Characterization- (6 papers)	**14:00-16:00** **E-1: Quantum Nanostructure Devices and Physics** -Fabrication and Micromechanics- (7 papers)	**14:00-16:00** **F-1: Compound Semiconductor Materials and Devices** -III-V and Nitride Electron Devices- (7 papers)	**14:00-15:50** **G-1: Advanced Silicon Circuits and Systems** -Advanced CMOS Circuits and Systems- (5 papers)
16:15-18:15 **A-2: Advanced Silicon Devices and Device Physics** -Advanced CMOS Technology I- (6 papers)	**16:15-17:35** **B-2: Non-Volatile Memory Technologies** -Non-Volatile Memory II- (4 papers)	**16:15-17:55** **C-2: Silicon Process / Materials Technologies** -High-k Gate Dielectric II- (5 papers)	**16:15-18:15** **D-2: New Materials and Characterization** -Low k and Silicide Characterization- (6 papers)	**16:15-18:00** **E-2: Quantum Nanostructure Devices and Physics** -Nanostructured Optical Devices- (6 papers)	**16:15-18:00** **F-2: Compound Semiconductor Materials and Devices** -Nitride Electron Devices- (6 papers)	**16:15-17:45** **G-2: Advanced Silicon Circuits and Systems** -Collaboration of Circuits and Devices- (4 papers)

18:30-20:30 Banquet, Eminence Hall

Wednesday, September 17

Room A	Room B	Room C	Room D	Room E	Room F	Room G
9:00-10:30 **A-3: Advanced Silicon Devices and Device Physics** -High-k Technology I- (4 papers)	**9:00-10:20** **B-3: Non-Volatile Memory Technologies** -Non-Volatile Memory III- (3 papers)	**9:00-10:30** **C-3: Silicon Process / Materials Technologies** -Memory Technology- (4 papers)	**9:00-10:30** **D-3: Silicon-on-Insulator Technologies** -SOI Novel Devices- (4 papers)	**9:00-10:15** **E-3: Quantum Nanostructure Devices and Physics** -Characterization and Nanoprobing- (5 papers)	**9:00-10:15** **F-3: Compound Semiconductor Materials and Devices** -Novel Compound Semiconductors Devices- (3 papers)	**9:00-10:30** **G-3: Advanced Silicon Circuits and Systems** -Circuit Technologies for Emerging Technologies- (4 papers)
10:45-12:00 **A-4: Optoelectronic Devices and Photonic Crystal Devices** -VCSELs and Visible Lasers- (4 papers)	**10:45-12:05** **B-4: Non-Volatile Memory Technologies** -Non-Volatile Memory IV- (4 papers)	**10:45-12:05** **C-4: Silicon Process / Materials Technologies** -DRAM- (4 papers)	**10:45-12:05** **D-4: Silicon-on-Insulator Technologies** -SOI Device Physics- (4 papers)	**10:45-12:15** **E-4: Quantum Nanostructure Devices and Physics** -Spin-related Phenomena- (5 papers)	**10:45-12:15** **F-4: Compound Semiconductor Materials and Devices** -Optical Devices- (5 papers)	**10:45-11:45** **G-4: System-Level Integration and Packaging Technologies** -System-Level Integration and Packaging Technologies I- (3 papers)
13:00-15:00 Poster Session (OHGI)						
15:15-16:45 **A-5: Optoelectronic Devices and Photonic Crystal Devices** -Optoelectronic Integrated Devices- (5 papers)	**15:15-16:30** **B-5: Organic Semiconductor Devices and Materials** -Preparation and Characterization- (5 papers)	**15:15-16:45** **C-5: Silicon Process / Materials Technologies** -Interconnect- (4 papers)	**15:15-16:45** **D-5: Silicon-on-Insulator Technologies** -Fin FET Technologies- (4 papers)	**15:15-16:30** **E-5: Quantum Nanostructure Devices and Physics** -Single Electron Transport- (4 papers)	**15:15-16:45** **F-5: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications** -Micro-Nano Electro Mechanical Devices for Bio-and Chemical Applications I- (5 papers)	**15:15-16:45** **G-5: System-Level Integration and Packaging Technologies** -System-Level Integration and Packaging Technologies II- (4 papers)
17:00-18:15 **A-6: Optoelectronic Devices and Photonic Crystal Devices** -Lasers for Optical Communication- (4 papers)	**17:00-17:40** **B-6: Non-Volatile Memory Technologies** -Non-Volatile Memory V- (2 papers)	**17:00-18:20** **C-6: Silicon Process / Materials Technologies** -Interconnect- (4 papers)	**17:00-18:30** **D-6: New Materials and Characterization** -Si/SiGe Devices and Materials- (4 papers)	**17:00-18:30** **E-6: Novel Devices, Physics, and Fabrication** -Nanoprocess and Nanodevices- (5 papers)	**17:00-18:00** **F-6: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications** -Micro-Nano Electro Mechanical Devices for Bio-and Chemical Applications II- (3 papers)	**17:00-18:15** **G-6: System-Level Integration and Packaging Technologies** -System-Level Integration and Packaging Technologies III- (4 papers)

18:45-20:45 Rump Session
Room A "Can channel material/structure engineering become a guiding principle for future CMOS device technology?"
Room B "What paradigm can nanoelectronic devices bring about?"

Thursday, September 18

Room A	Room B	Room C	Room D	Room E	Room F	Room G
9:00-10:30 **A-7: Advanced Silicon Devices and Device Physics** -High-k Technology II- (4 papers)	**9:00-10:20** **B-7: Silicon Process / Materials Technologies** -Metal Gate, Gate Oxde- (4 papers)	**9:15-10:30** **C-7: Organic Semiconductor Devices and Materials** -Organic Thin Film Transistor- (4 papers)	**9:20-10:30** **D-7: New Materials and Characterization** -Carbon Nanotube Devices and Materials- (3 papers)	**9:30-10:30** **E-7: Novel Devices, Physics, and Fabrication** -Novel Materials and Devices- (4 papers)	**9:00-10:30** **F-7: Optoelectronic Devices and Photonic Crystal Devices** -Photonic Crystal Devices I- (5 papers)	**9:00-10:30** **G-7: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** -III-V Devices & Circuits- (5 papers)
10:45-12:05 **A-8: Advanced Silicon Devices and Device Physics** -Advanced CMOS Technology II- (4 papers)	**10:45-12:05** **B-8: Silicon Process / Materials Technologies** -Si Process- (4 papers)	**10:45-12:00** **C-8: Organic Semiconductor Devices and Materials** -Organic Optics- (5 papers)	**10:45-11:25** **D-8: New Materials and Characterization** -High-k Dielectrics I- (2 papers)	**10:45-12:00** **E-8: Novel Devices, Physics, and Fabrication** -Carbon Nanotubess- (4 papers)	**10:45-11:45** **F-8: Optoelectronic Devices and Photonic Crystal Devices** -Photonic Crystal Devices II- (3 papers)	**10:45-11:45** **G-8: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** -SiGe Technologies- (3 papers)
13:30-14:50 **A-9: Advanced Silicon Devices and Device Physics** -Electron Mobility Characteristics- (4 papers)	**13:30-14:40** **B-9: Silicon-on-Insulator Technologies** -SOI Low Power Applications- (3 papers)	**13:30-14:45** **C-9: Organic Semiconductor Devices and Materials** -Molecular Devices and Materials- (4 papers)	**13:30-14:30** **D-9: New Materials and Characterization** -High-k Dielectrics II- (3 papers)	**13:30-14:45** **E-9: Novel Devices, Physics, and Fabrication** -Si Nanowire and Dots- (4 papers)	**13:30-14:45** **F-9: Optoelectronic Devices and Photonic Crystal Devices** -Ultrafast Photonic Devices- (4 papers)	**13:30-14:45** **G-9: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** -GaN Devices- (4 papers)
15:00-16:00 **A-10: Advanced Silicon Devices and Device Physics** -Poly-Si Device and Sensor- (3 papers)	**15:00-16:30** **B-10: Silicon-on-Insulator Technologies** -SOI CMOS Technologies- (4 papers)	**15:00-16:00** **C-10: Organic Semiconductor Devices and Materials** -Electroluminescent Devices and Materials- (4 papers)	**15:00-16:20** **D-10: New Materials and Characterization** -High-k DielectricsIII- (4 papers)	**15:00-16:15** **E-10: Novel Devices, Physics, and Fabrication** -Quantum Computing Devices- (4 papers)	**15:00-16:00** **F-10: Optoelectronic Devices and Photonic Crystal Devices** -New Photonic Materials- (4 papers)	**15:00-16:00** **G-10: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** -High Voltage Devices- (3 papers)

SSDM 2003 Advance Program
General Information

DATE
Conference: **September 16-18, 2003**
Short Course: **September 19, 2003 (in Japanese)**

LOCATION
Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel)
2-2-1 Nishi-Shinjuku, Shinjuku-Ku, Tokyo 160-8330
TEL +81-3-3344-0111 FAX +81-3-3345-8269
Keio Plaza Inter-Continental Tokyo is approximately 120 minutes by Airport Bus from New Tokyo International Airport (Narita), and only 5 minutes by walking from JR Shinjuku Station.
Web site: http://www.keioplaza.com/index.html

REGISTRATION
The registration desk will be open from September 15th to 19th. The registration hours are as follows:

September	15	17:00-19:00		MITAKE, 42F
	16	8:00-12:00		front of EMINENCE HALL, 5F
		13:00-17:00		front of TSUKUI, 42F
	17	8:00-15:30		"
	18	8:00-15:30		"
	19	8:00-13:30	(Short Course)	"

Pre-registration is accepted only through the conference website before September 1, 2003. After that date, registration can be made at the conference site. Early registration is recommended due to the expected large number of participants.

	Registration Fee		Short Courses in Japanese	Banquet
	On or before August 1	After August 1		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanying person(s)				¥4,000/person

1) The registration fee includes one copy of the abstract book, a CD-ROM and coffee breaks. However, it does not include the Banquet, and extra payment of 7,000 yen or 4,000 yen is required to attend the Banquet for regular participants and student participants, respectively.
2) Those who register as students are required to fax a copy of their current student ID to the secretariat at the time of registration, and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of online registration of individual information.
3) Registration is complete only with full payment.

Payment of the registration fee is to be made by one of the following methods. Please note that we do not accept personal checks.

1. Bank Transfer
A direct bank transfer can be made to the account below. A copy of the receipt for the bank remittance should be sent to the secretariat by fax. The registration ID must be written on the fax sheet. Please note that the bank service charge must be borne by the applicant.
- Name of Bank: Bank of Tokyo-Mitsubishi, Akasaka Branch
- Account Name: SSDM2003
- Account No: 1528425 (ordinary deposit)

2. Credit Card
Amex, VISA, MasterCard, Diners Club and JCB are acceptable.

Confirmation of Pre-Registration
The Secretariat will e-mail a confirmation to you after verifying payment in early September. Please print the confirmation slip out, bringing it with you to the conference and present it at the registration desk.

REGISTRATION CANCELLATION
Conference:
Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to the SSDM 2003 Secretariat. No cancellation will be accepted after August 19, 2003. Extended Abstracts will be sent to absent registrants after the Conference.

Short Course:
Cancellation fee of ¥2,000 will be deducted from the refund. Cancellations should be made in writing to the SSDM 2003 Secretariat. No cancellation will be accepted after August 19. A text will be sent to the absent registrants after the Conference.

BANQUET
Banquet will be held at “Eminence Hall” of the Keio Plaza Inter Continental Tokyo (5F) on September 16 from 18:30-20:30. Tickets (Regular ¥7,000 / Student ¥4,000) can be purchased at the registration desk.

LATE NEWS PAPERS

Late News Paper Deadline is July 25, 2003.

Late news papers describing important new developments may be submitted. A 2-page paper must be sent in the camera-ready format as required for the regular papers. The accepted papers will be included in the extended abstracts.
The abstract must be submitted through the conference Web site: http://www.intergroup.co.jp/ssdm.
Notice of acceptance will be e-mailed by the middle of August.

EXTENDED ABSTRACTS AND PUBLICATION
Authors of papers accepted for SSDM 2003 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics. The special issue will be published in April 2004. Please refer to the conference website for details.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS
Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by the automatic withdrawal of the paper by the conference committee.

AWARDS
"SSDM Awards" will be given to excellent papers presented in the previous conferences.

SSDM Award

For the paper, which made an outstanding contribution to the field of solid state devices and materials, among the papers presented prior to 1997.

SSDM Paper Award

For the best paper presented at the last conference.

SSDM Young Researcher Award

For a few excellent papers by young researchers presented at the last conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter.

VISA REQUIREMENT

All foreign participants must have valid passport. Participants from countries where a visa is required to enter Japan are recommended to apply at the nearest Japanese embassy in their countries as soon as possible.

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT) has been appointed as the official travel agent for the conference and will handle accommodations.

Kinki Nippon Tourist Co., Ltd.
Event, Convention and Congress Department
6F, Kyodo Bldg., 2-2 Kanda-Jinbocho, Chiyoda-ku, Tokyo 101-0051 Japan
Phone:+81-3-3263-5581, Fax:+81-3-3263-5961
E-mail:SSDM2003@knt-tokyo.gr.jp

HOTEL ACCOMMODATIONS

Hotel accommodations for the nights of September 15(in) - 19(out) are now available **through the conference website.** Early reservation is recommended due to the expected large number of participants.

#	Hotel Name	Single W/bath	Twin W/bath	Location	Grade
①	*Keio Plaza* Inter-Continental Tokyo	**¥19,100**	**¥25,400**	Shinjuku Station (walk 5 min)	Deluxe
②	*Hotel SunRouteTokyo*	**¥11,860**	**¥16,170**	Shinjuku Station (walk 3 min)	Superior
③	*Shinjuku Washington Hotel*	**¥12,700**	**¥15,750**	Shinjuku Station (walk 7 min)	Superior

All room rates include breakfast, service charge and consumption tax.

APPLICATION AND PAYMENT OF DEPOSIT

1. Participants wishing to make reservations for accommodations should submit your reservation form by the "Online Reservation button" at the conference website. Then your application form is transmitted to KNT. Reservation will close at August 15, 2003. Reservation should be proceeded on first come first served basis. Applications for hotel reservations should be accompanied by a deposit of 10,000 yen. Please pay for the balance at the hotel.

2. Payments must be made by either one of the following;
   a. Credit cards (Visa, MasterCard, American Express, JCB); Please fill in the Credit Card Authorization in the application form.
   b. Bank transfer; Please remit the deposit plus a handling charge to the following account.

Name of bank: **Sumitomo Mitsui Banking Corp., Chuo Branch**
Name of Account: **Kinki Nippon Tourist Co., Ltd.**
Account Number: **1855682**

NOTE: Personal checks are not acceptable. We would appreciate your kindly sending us a photocopy of the bank's receipt for your remittance.

CANCELLATION

In case of changes or cancellations, please inform KNT by FAX or E-mail. KNT accepts only written notification. The following cancellation fees apply according to the date of your notification.

5 to 2 days prior to the first night	¥1,000
1 day prior to the first night	50% of daily room charge
The first night or no notice given	100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

The temperature in Tokyo during the period of the conference ranges between 18 and 30 degrees centigrade.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

RUMP SESSIONS - September 17 (Wednesday) 18:45-20:45

Rump session 1 (Room A, FUJI, 42F)

"Can channel material/structure engineering become a guiding principle for future CMOS device technology?"

The simple device scaling rule has been facing to several physical and fundamental limitations, leading to severe trade-off relationships among device performance, short channel effects and power consumption. As one possible solution to avoid this difficulty, new channel structures different from conventional planar Si channel are currently stirring a strong interest. This channel engineering mainly includes two directions; one is new channel materials with high carrier mobility, such as strained-Si, SiGe and Ge, and the other is 3-dimensional channel structures to enhance gate control over channel potential, such as FinFET, double gate MOS, Gate-all-around (GAA) MOS and vertical MOS. However, a scenario for continuously improving the device characteristics under these many engineering options has not been clarified yet. Thus, it is a good timing to examine possibilities, realities and major roles of these non-classical MOSFETs for future technology nodes.

In this rump session, we would like to discuss following issues. (1) Can further and continuous improvements of CMOS characteristics be really achieved by channel material/structure engineering? (2) What is a guiding principle for CMOS device technologies in the future nodes, still smaller size, channel materials, channel geometrical structures or anything else? (3) What are critical issues in the competition between classical vs. non-classical CMOS?

Organizer	Panelists	
S. Takagi	T-J. King (UCB, USA)	FinFET, UTB SOI, Ge MOS
(Toshiba,	T. Skotnicki (STMicro, France)	SON, GAA MOS, Si/SiGeC MOS
MIRAI-ASET,	K. Rim (IBM, USA)	strained-Si/Strained-SOI CMOS
Japan)	K. Ishimaru (Toshiba, Japan)	Advanced CMOS, Bulk CMOS
	T. Takagi (Matsushita, Japan)	SiGe Analog Devices, SiGe/SiGeC HBT
	T. Sugii (Fujitsu, Japan)	From the viewpoint of ITRS

Rump session 2 (Room B, TAKAO, 42F)

" What paradigm can nanoelectronic devices bring about? "

Nanotechnology is expected to be a key technology in the 21st century bringing innovations for materials and devices. What kind of innovations are expected in the electronic devices by reducing the device feature sizes to nanometer-scale or even controlling molecular and atomic structures? Are the nanoelectronic devices positioned as a post-Si CMOS in the miniaturization limit, or will they co-exist with Si-CMOS devices by realizing new functions which are hardly provided solely by present Si devices? What paradigm can the nanoelectronic devices bring about in the future information society? From those standpoints, we would like to discuss future prospect of the nanoelectronic devices in the rump session, mainly by focusing on carbon nanotube devices, molecular/atomic and organic electronic devices, spin-electronic devices, and ultra small-scaled Si devices.

Moderators	Panelists	
J. Sone (NEC, Japan)	H.-S. P. Wong (IBM, USA)	Carbon nanotube electronics
Y. Wada (Waseda Univ., Japan)	Y. Awano (Fujitsu, Japan)	Carbon nanotube electronics
	K. Kudo (Chiba Univ., Japan)	Organic semiconductor devices
Organizer	M. Tanaka (Univ. of Tokyo, Japan)	Spin electronics
J. Sone (NEC, Japan)	T. Hiramoto (Univ. of Tokyo, Japan)	Nanostructured Si MOS

SHORT COURSES

Two short courses will be held on September 19 (Friday) for young engineers and students. All lectures are given in Japanese. Please refer to the attached information for details.

SSDM 2003 INSTRUCTION for SPEAKERS

<Oral Presentation>

Presentation Time

	Session Time	Presentation Time	Discussion
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of the presentation time, Third: End of the discussion time.

Audio-Visual Equipment

The meeting room will contain the following audiovisual equipment:

- Overhead projector
- LCD data projector (PC is not provided)
- Microphone
- Projection laser pointer

It is strongly recommended that you use the Overhead projector for your presentation.

Authors wishing to present their paper using LCD projector are requested to bring overhead transparencies preparing for an unforeseen accident.

<Poster Presentation>

Poster Sessions are scheduled as follows:

13:00-15:00 on Wednesday, September 17

Authors must remain in the vicinity of the bulletin board for the duration of the session to answer questions.

900mm(W) x 2,100mm(H) poster board, a sign indicating your paper number and push pins will be provided at the poster room, OHGI, 4F. Presenters should display, on their poster, the paper title, authors and affiliation.

Authors are requested to prepare their poster materials during:
9:00 to 12:00 of September 17.
Please put their poster materials off by:
17:00 on September 17.

Tuesday, September 16

EMINENCE HALL

PL: Opening Session (9:30 - 12:30)
Chairpersons: S. Kawamura, AIST and M. Koyanagi, Tohoku Univ.

9:30 PL-0
Welcome Address and Award Presentation
M. Nakamura, Hitachi

9:45 PL-1 (Plenary)
Research and Development Strategy for Creation of Corporate Value
T. Ikoma, Hitotsubashi Univ., Japan

10:30 PL-2 (Plenary)
Role and Strategy of IMEC as a European Player in a Globalized Research Era
G.J. Declerck, IMEC, Belgium

11:15 PL-3 (Plenary)
Progress and Perspective of Nanostructure Devices for Ubiquitous Information Network
Y. Arakawa, Univ. of Tokyo, Japan

12:30-14:00 Lunch

Room A

A-1: Advanced Silicon Devices and Device Physics
-Gate Stack Technologies-
(14:00-15:50)
Chairs: T. Mogami (NEC)
K. Shibahara (Hiroshima Univ.)

14:00 A-1-1 (Invited)
Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation
J. Kedzierski[1], E. Nowak[2], M. Ieong[2], T. Kanarski[2], and D. Boyd[2], [1]*SRDC, IBM,* [2]*Microelectronics Division, USA*

14:30 A-1-2
Influences of Gate-Poly Impurity Concentration on Inversion-Layer Mobility in MOSFETs with Ultrathin Gate Oxide Film
J. Koga[1], T. Ishihara[1] and S. Takagi[1], [1]*Toshiba Corp., Japan*

Room B

B-1: Non-Volatile Memory Technologies
-Non-Volatile Memory I-
(14:00-16:00)
Chairs: T. Nakamura (Rohm)
Y. Shimada (Matsushita Electric)

14:00 B-1-1 (Invited)
Current FeRAM Technology Developments and Scaling towards 3-D Capacitor Cells
D.J. Wouters[1], [1]*IMEC, Belgium*

14:30 B-1-2 (Invited)
32Mb Chain FeRAM -An Overview
D. Takashima[1] and T. Rohr[2], [1]*Toshiba Corp., and* [2]*Infineon Technologies Japan K.K., Japan*

Room C

C-1: Silicon Process / Materials Technologies
-High-k Gate Dielectric I-
(14:00-15:50)
Chais: Y. Tsunashima (Toshiba)
H. Kitajima (Selete)

14:00 C-1-1 (Invited)
Mobility in high-κdielectric based field effect transistors
L-A Ragnarsson[1], W. Tsai[2], A. Kerber[3], P.J. Chen[4], E. Cartier[5], L. Pantisano[1], S. De Gendt[1], and M. Heyns[1], [1]*IMEC, Belgium,* [2]*Intel Corp.,* [3]*Infineon,* [4]*Texas Instruments, USA, and* [5]*IBM*

14:30 C-1-2
Effect of the Film Composition of HfAlON Gate Dielectric on the Structural Transformation and the Electrical Properties through High-temperature Annealing
M. Koyama[1], Y. Kamimuta[1], M. Koike[1], M. Suzuki[1] and A. Nishiyama[1], [1]*Toshiba Corp., Japan*

Room D

D-1: New Materials and Characterization
-Oxide Reliability and Surface Characterization-
(14:00-16:00)
Chairs: H. Satake (Toshiba)
T. Maruizumi (Hitachi)

14:00 D-1-1
The Effect of Boron and Fluorine Incorporation in SiON Gate Insulator on NBTI
T. Sasaki[1], F. Ootsuka[1], H. Ozaki[1], M. Tomikawa[1], M. Yasuhira[1] and T. Arikado[1], [1]*SELETE, Japan*

14:20 D-1-2
New insights into dynamic negative bias temperature instabilities of pMOSFETs
S.S. Tan[1], T.P. Chen[1], C.H. Ang[2], W.Y. Teo[2] and L. Chan[2], [1]*Nanyang Technological Univ. of Singapore and* [2]*Chartered Semiconductor Manu. Ltd., Singapore*

Room E

E-1:Quantum Nanostructure Devices and Physics
-Fabrication and Micromechanics-
(14:00-16:00)
Chairs: Y. Hirayama (NTT)
J. Motohisa (Hokkaido Univ.)

14:00 E-1-1 (Invited)
Electronic and photonic devices via one-dimensional stacking of quantum structures
L. Samuelson[1], [1]*Lund Univ., Solid State Physics/the Nanometer Consortium*

14:30 E-1-2
Formation of 1μm-period GaAs Kagome Lattice Structure by Selective Area Metalorganic Vapor Phase Epitaxy
P. Mohan[1], J. Motohisa[1] and T. Fukui[1], [1]*Hokkaido Univ., Japan*

Room F

F-1:Compound Semiconductor Materials and Devices
-III-V and Nitride Electron Devices-(14:00-16:00)
Chairs: T. Mizutani (Nagoya Univ.)
M. Kuzuhara (FED)

14:00 F-1-1 (Invited)
Ultrahigh Performance InP HEMTs
A. Endoh[1], Y. Yamashita[1], K. Shinohara[2], K. Hikosaka[1], T. Matsui[2], S. Hiyamizu[2], and T. Mimura[1], [1]*Fujitsu Labs Ltd.,* [2]*Osaka Univ., Japan*

14:30 F-1-2
High f_T 30nm $In_{0.7}GaAs$ HEMT fabricated with SiO_2/SiN_x sidewall Process and BCB Planarization
D.-H. Kim[1], S.-J. Yeon[1], S.-S. Song[1] and K.-S. Seo[1], [1]*Seoul National Univ., Korea*

Room G

G-1:Advanced Silicon Circuits and Systems
-Advanced CMOS Circuits and Systems-(14:00-15:50)
Chairs: T. Kuroda (Keio Univ.)
M. Fujishima (Univ. of Tokyo)

14:00 G-1-1 (Invited)
Silicon Integration of UWB: Choices and Challenges
S.G. Narendra
[1]*Circuit Research - Intel Labs, USA*

14:30 G-1-2
Low-Power Real-Time Region-Growing Image-Segmentation in 0.35μm CMOS due to BAO-Scheme and Subdivided-Image Approach
T. Morimoto[1], Y. Harada[1], T. Koide[1] and H.J. Mattausch[1], [1]*Hiroshima Univ., Japan*

Room A

14:50 A-1-3
New Self-aligned Metal-gate MOSFETs Using Aluminum Substitution Technology
S. Nakamura[1], H. Shido[1], T. Kurahashi[1], S. Kishii[1], T. Nagata[1], B. Kumasaka[1], T. Usuki[1], S. Sato[1] and Y. Mishima[1], [1]*Fujitsu Labs Ltd., Japan*

15:10 A-1-4
Screening Effect on Remote Coulomb Scattering due to impurities in Polysilicon Gate of MOSFET
T. Ishihara[1], J. Koga[1], S. Takagi[1] and K. Matsuzawa[1], [1]*Toshiba Corporation, Japan*

15:30 A-1-5
Direct evaluation of an interfacial layer in high-*k* gate dielectrics by 1/f noise measurements
T. Ishikawa[1], S. Tsujikawa[1], S. Saito[1], D. Hisamoto[1] and S. Kimura[1], [1]*Hitachi, Ltd., Japan*

Room B

15:00 B-1-3
A proposal of new ferroelectric gate field effect transistor memory based on ferroelectric-insulator interface conduction
G. Hirooka[1], M. Noda[1] and M. Okuyama[1], [1]*Osaka Univ., Japan*

15:20 B-1-4
Long-Term Stabilization of Sense Signals in a Non-Destructive Readout FeRAM by Intentional Modification of the Polarization Hysteresis Curve for Low Voltage Applications
T. Yamada[1], Y. Kato[1], S. Koyama[1] and Y. Shimada[1], [1]*Matsushita Electric Industrial Co., Ltd., Japan*

15:40 B-1-5
A Low Dielectric Constant $Sr_2(Ta_{1-x},Nb_x)_2O_7$ Thin Film Controlling the Crystal Orientaion on IrO_2 Substrate for One Transistor Type Ferroelectric Memory Device
I. Takahashi[1], H. Sakurai[1], A. Yamada[2], T. Goto[1], M. Hirayama[1], A. Teramoto[1], S. Sugawa[1] and T. Ohmi[1], [1]*NICHe, Tohoku Univ. and* [2]*Tohoku Univ., Japan*

Room C

14:50 C-1-3
Projection of Mobility Degradation in $HfAlO_x/SiO_2$ nMOSFET towards the Reduction of Interfacial Oxide Thickness
N. Yasuda[1], H. Hisamatsu[1], H. Ota[2], K. Iwamoto[1], K. Tominaga[1], K. Yamamoto[1], W. Mizubayashi[2], N. Yamagishi[1], M. Ohno[1], S. Migita[2], Y. Morita[2], T. Horikawa[2], T. Nabatame[1] and T. Toriumi[2,3], [1]*MIRAI-ASET,* [2]*MIRAI-ASRC and* [3]*The Univ. of Tokyo, Japan*

15:10 C-1-4
Ultra-thin (EOT<1.0nm) Amorphous HfSiON Gate Insulator with High Hf Concentration for High-performance Logic Applications
M. Koike[1], T. Ino[1], M. Koyama[1], Y. Kamata[1], Y. Kamimuta[1], M. Suzuki[1], A. Takashima[1], Y. Mitani[1], A. Nishiyama[1] and Y. Tsunashima[1], [1]*Toshiba Corporation, Japan*

15:30 C-1-5
Hafnium Content Dependence of Bottom Interfacial Layer and Its Impact on $Hf_xAl_{1-x}O_y$ High-k nMOSCAPs and nMOSFETs Characteristics
Y. Tamura[1], Y. Sugiyama[1], M. Yamaguchi[1], H. Minakata[1], Y. Tanida[1], T. Sakoda[1], M. Nakamura[1] and Y. Nara[1], [1]*Fujitsu Labs Ltd., Japan*

Break

Room D

14:40 D-1-3
Neighboring effect in nitrogen-enhanced negative bias temperature instability
S.S. Tan[1], T.P. Chen[1], J.M. Soon[2], K.P. Loh[2], C.H. Ang[3], W.Y. Teo[3] and L. Chan[3], [1]*Nanyang Technological Univ. of Singapore,* [2]*National Univ. of Singapore and* [3]*Chartered Semiconductor Manu. Ltd., Singapore*

15:00 D-1-4
Conductive Atomic Force Microscopy Analysis for Local Electric Characteristic in Stressed SiO_2 Gate Films
Y. Watanabe[1], A. Seko[2], H. Kondo[2], A. Sakai[2], S. Zaima[2] and Y. Yasuda[2], [1]*Toyota Central R&D Labs., Inc.,* [2]*Nagoya Univ., Japan*

15:20 D-1-5
Measurement of extension structures in deep sub-micron MOSFETs by scanning capacitance microscopy based on frequency modulation control
Y. Naitou[1] and N. Ookubo[1], [1]*Silicon Systems Research Labs, NEC Corporation, Japan*

15:40 D-1-6
Valence-Mended Si(100) for Nanoelectronic Applications
M. Tao[1], W. P. Kirk[1], D. Udeshi[1], S. Agarwal[1], E. Maldonado[1] and N. Basit[1], [1]*Univ. of Texas at Arlington, USA*

Room E

14:45 E-1-3
Selective MBE Growth of GaAs Hexagonal Nano-wire Networks on (111)B Patterned Substrates
S. Yoshida[1], I. Tamai[1], T. Sato[1] and H. Hasegawa[1], [1]*Hokkaido Univ., Japan*

15:00 E-1-4
Migration-induced Ge Dot Formation
S. Kaechi[1], D. Kitayama[1] and Y. Suda[1], [1]*Tokyo Univ. of Agriculture & Technology, Japan*

15:15 E-1-5
Demonstration of MEMS-Controlled Electronic States in Single Quantum Dots
T. Nakaoka[1], T. Kakitsuka[2], T. Saito[1] and Y. Arakawa[1,2], [1]*RCAST, IIS, and CCR, Univ. of Tokyo and* [2]*NTT Photonics Labs, NTT Corporation, Japan*

15:30 E-1-6
Displacement Sensing using Quantum Mechanical Interference
H. Yamaguchi[1], S. Miyashita[2] and Y. Hirayama[1,3], [1]*NTT Basic Research Labs,* [2]*NTT Advanced Technology and* [3]*CREST-JST, Japan*

15:45 E-1-7
ZnO Metal-Insulator-Semiconductor Field-Effect-Transistor
J. Nishii[2], A. Ohtomo[1], T. Fukumura[1], K. Ohtani[2], F. Matsukura[2], Y. Ohno[2], H. Ohno[2] and M. Kawasaki[1], [1]*Tohoku Univ. and* [2]*RIEC, Tohoku Univ., Japan*

Room F

14:45 F-1-3
Observation of Thermal Reliability of BCB Passivated InAlAs/InGaAs HEMTs
M. Yoon[1], T. Kim[1], D. Kim[1] and K. Yang[1], [1]*KAIST, Korea*

15:00 F-1-4
High f_{max} 0.1 μm Γ-gate InGaAs/InAlAs/GaAs Metamorphic HEMT
B.H. Lee[1], B.O. Lim[1], M.R. Kim[1], S.D. Kim[1], J.K. Rhee[1] and H.S. Yoon[2], [1]*MINT and* [2]*Electronics and Telecommunications Research Inst., Korea*

15:15 F-1-5
Reduction of Turn-on Voltage in GaInNAs and InGaAs Base Double Heterojunction Bipolar Transistors
C.-H. Wu[1], Y.-K. Su[1], S.-C. Wei[1] and S.-J. Chang[1], [1]*National Cheng Kung Univ., Taiwan*

15:30 F-1-6
InP/InGaAs Tunneling Emitter Bipolar Transistor (TEBT)
C.-Y. Chen[1], H.-M. Chuang[1], S.-I. Fu[1], P.-H. Lai[1], Y.-Y. Tsai[1], C.-I. Kao[1] and W.-C. Liu[1], [1]*National Cheng-Kung Univ., Taiwan*

15:45 F-1-7
High-Quality Two-Dimensional Electron Gas at Large Scale GaN/AlGaN Wafer Interface Prepared by Mass Production MOCVD Systems
S. Yamada[1], T. Ohnishi[1], T. Kakegawa[1], M. Akabiri[1], T. Suzuki[1], H. Sugiura[2], F. Nakamura[2], E.Yamaguchi[2] and H. Kawai[2], [1]*CNMT, JAIST and* [2]*Powdec K.K., Japan*

Room G

14:50 G-1-3
Butterfly-Unit Based Programmable Computation Element Using Merged Module of Multiplication, Division and Square Root
L. Karnan[1], N. Miyamoto[1], K. Maruo[1], K. Kotani[1] and T. Ohmi[2], [1]*Tohoku Univ. and* [2]*NICHe, Tohoku Univ., Japan*

15:10 G-1-4
A Hierarchical 512-Kbit SRAM with 8 ports in 130nm CMOS
S. Fukae[1], N. Omori[1], T. Koide[1], H. J. Mattausch[1] and T. Hironaka[2], [1]*RCNS, Hiroshima Univ. and* [2]*Hiroshima City Univ., Japan*

15:30 G-1-5
Combined Data/Instruction Cache with Bank-Based Multi-Port Architecture
K. Johguchi[1], Z. Zhu[1], T. Hirakawa[2], T. Koide[1], T. Hironaka[2] and H.J. Mattausch[1], [1]*Hiroshima Univ. RCNS and* [2]*Hiroshima City Univ., Japan*

Break

Room A

A-2: Advanced Silicon Devices and Device Physics
-Advanced CMOS Technology I-(16:15-18:15)
Chairs: A. Hiroki (Kyoto Inst. of Technol.)
S. Inaba (Toshiba)

16:15 A-2-1
Enhancement of V_{th} Degradation under NBT Stress due to Hole Capturing
Y. Mitani[1], M. Nagamine[1], H. Satake[1] and A. Toriumi[2], *[1]Toshiba Corporation and [2]The Univ. of Tokyo, Japan*

16:35 A-2-2
New Mechanism for Negative-Bias-Temperature Instability and Its Impact on Scaling of pMOSFETs
D.-Y. Lee[1], H.-C. Lin[2], C.-C. Chen[3], C.-H. Chien[2], T.-Y. Huang[1], T. Wang[1], T.-L. Lee[3], S.-C. Chen[3] and M.-S. Liang[3], *[1]National Chiao-Tung Univ., [2]National Nano Device Labs and [3]Taiwan Semiconductor Manufacturing Company, Taiwan*

16:55 A-2-3
Origin of Enhanced Thermal Noise for 100nm-MOSFETs
S. Hosokawa[1], Y. Shiraga[1], H. Ueno[1], M. Miura-Mattausch[1], H. J. Mattausch[1], T. Ohguro[2], S. Kumashiro[2], M. Taguchi[2], H. Masuda[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]STARC, Japan*

17:15 A-2-4
Comparison of the Interconnect Capacitances for Various SRAM Cell Lyaouts To Achieve High Speed, Low Power SRAM Cells
Y. Tsukamoto[1], K. Nii[1], Y. Yamagami[2], T. Yoshizawa[1], S. Imaoka[3], T. Suzuki[2], A. Shibayama[2] and H. Makino[1], *[1]Renesas Technology Corporation, [2]Matsushita Electric Industrial Corporation and [3]Renesas Device Design Corporation, Japan*

Room B

B-2: Non-Volatile Memory Technologies
-Non-Volatile Memory II-(16:15-17:35)
Chairs: Y. Shimada (Matsushita Electric)
T. Nakamura (Rohm)

16:15 B-2-1
Novel Capacitor Structure Using Sidewall Spacer for Highly Reliable FRAM Device
H.H. Kim[1], J.H. Park[1], Y.J. Song[1], N.W. Jang[1], H.J. Joo[1], S.K. Kang[1], S.H. Joo[1], S.Y. Lee[1] and K. Kim[1], *[1]Samsung Electronics Co. Ltd., Korea*

16:35 B-2-2
High perfomance PZT capacitor using highly crystalline SRO bottom electrode for Mbit FeRAM devices
H. Itokawa[1], K. Natori[1], S. Yamazaki[1], G. Beitel[2] and K. Yamakawa[1], *[1]Toshiba Corp. and [2]Infineon Technologies Japan., Japan*

16:55 B-2-3
A novel chemical solution deposition method suitable for high-yield fabrication of 50 nm-thick $SrBi_2Ta_2O_9$ capacitors
Y. Kawashima[1] and H. Ishiwara[1], *[1]Tokyo Inst. of Technology, Japan*

17:15 B-2-4
Two-Mode Behavior in Time and Temperature Dependence of Imprint-Induced Charge Loss in Integrated $SrBi_2(Ta,Nb)_2O_9$ Capacitors
A. Noma[1], T. Mikawa[1], Y. Nagano[1], Y. Judai[1] and E. Fujii[1], *[1]Matsushita Electric Industrial Co., Ltd., Japan*

Room C

C-2: Silicon Process / Materials Technologies
-High-k Gate Dielectric II-(16:15-17:55)
Chairs: M. Kubota (Matsushita Electric)
J. Yugami (Renesas)

16:15 C-2-1
Flatband Voltage Shift Caused by Dopants Diffused from Poly-Si Gate Electrode in Poly-Si/HfSiO/SiO_2/Si
A. Kaneko[1], S. Inumiya[1], K. Sekine[1], M. Sato[1], Y. Kamimuta[1], K. Eguchi[1] and Y. Tsunashima[1], *[1]Toshiba Corporation, Japan*

16:35 C-2-2
Controlled Nitrogen Incorporation into $HfAlO_x$ by Layer-by-Layer Deposition and Annealing (LL-D&A) Process and Its Impact on Electrical Properties of MOSCAPs and nMOSFETs
K. Tominaga[1], K. Iwamoto[1], H. Hisamatsu[1], T. Yasuda[2], H. Ota[2], N. Yasuda[1], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC, AIST and [3]the Univ. of Tokyo, Japan*

16:55 C-2-3
Suppression of Silicidation in Poly-Si/ZrO_2/SiO_2/Si Structure by Helium Through Process
K. Muraoka[1], *[1]Advanced LSI Technology Lab, Toshiba Corporation, Japan*

17:15 C-2-4
Reliability characteristics of an HfO_2/SiO_2 stack gate dielectric annealed in a deuterium ambient
H. Park[1], H. Yang[1], H. Sim[1] and H. Hwang[1], *[1]Kwangju Inst. of Science and Technology, Korea*

Room D

D-2: New Materials and Characterization
-Low k and Silicide Characterization-(16:15-18:15)
Chairs: K. Kikuta (NEC)
S. Zaima (Nagoya Univ.)

16:15 D-2-1
Nondestructive Characterization of Pore Size Distributions in Porous Low-k Films by in-situ Spectroscopic Ellipsometry in Vapor Cell
C. Negoro[1], N. Hata[1,2] and T. Kikkawa[2,3], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST and [3]RCNS, Hiroshima Univ., Japan*

16:35 D-2-2
Accurate measurement of mechanical properties of nanoporous silica ultra-low-k films
Y. Seino[1], R. Ichikawa[2], H. Tanaka[3] and T. Kikkawa[4], *[1]MIRAI Project, ASRC, AIST, [2]ASRC, AIST, [3]MIRAI Project, ASET and [4]RCNS, Hiroshima Univ., Japan*

16:55 D-2-3
Mechanical Property and Skeletal Silicate Structure of Periodic Porous Silica Films
S. Takada[1], N. Hata[1,2], Y. Seino[1,2], K. Yamada[3], Y. Oku[3] and T. Kikkawa[2,4], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*

17:15 D-2-4
Determination of the Mechanical Properties of Thin Periodic Porous Silica Films by Laser-Generated Surface Acoustic Wave Technique
X. Xiao[1], N. Hata[2,1], K. Yamada[3], H. Tanaka[3] and T. Kikkawa[4,2], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*

Room E

E-2:Quantum Nanostructure Devices and Physics
-Nanostructured Optical Devices-(16:15-18:00)
Chairs: K. Hirakawa (Univ. of Tokyo)
L. Samuelson (Lund Univ.)

16:15 E-2-1 (Invited)
A Light Emitting Diode for Single Photons
A.J. Shields[1], Z. Yuan[1], M.B. Ward[1], R.M. Stevenson[1], B.E. Kardynal[1], P. See[1], C. Lobo[2], P. Atkinson[2] and D.A. Ritchie[2], *[1]Toshiba Research Europe Ltd., Cambridge Research Lab and [2]Cavendish Lab., Univ. of Cambridge, UK*

16:45 E-2-2
Coherent control of exiton in a single quantum dot using a high-resolution Michelson interferometer
T. Okada[1,2,3], K. Komori[2,3], K. Goshima[2,3], S. Yamauchi[2,3], T. Sugaya[2,3], O. Yamazaki[4] and T. Hattori[4], *[1]Tokai Univesity Junior College, [2]AIST, [3]CREST-JST, Japan and [4]Univ. of Tsukuba, Japan*

17:00 E-2-3
Voltage-controlled Emission Wavelength Switching in a Pseudomorphic $Si_{1-x}Ge_x$/Si Double Quantum Well
N. Yasuhara[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo and [2]PRESTO-JST, Japan*

17:15 E-2-4
A Solid-State Multicolor Light-Emitting Device Based on Ballistic Electron Excitations
Y. Nakajima[1], T. Uchida[1], A. Kojima[1], B. Gelloz[1] and N. Koshida[1], *[1]Tokyo Univ. of Agri. & Tech., Japan*

Room F

F-2:Compound Semiconductor Materials and Devices
-Nitride Electron Devices-(16:15-18:00)
Chairs: T. Kikkawa (Fujitsu Labs.)
N. Maeda (NTT)

16:15 F-2-1 (Invited)
MOVPE Growth of Wurtzite InN and its Characteristics
T. Matsuoka[1], H. Okamoto[2], M. Nakao[2], H. Harima[3], H. Takahata[4], H. Mitate[4], S. Mizuno[4], Y. Uchiyama[5], T. Makimoto[1], *[1]NTT Basic Research Labs, [2]NTT Photonics Labs, [3]Kyoto Inst. of Technology, [4]NTT Advanced Technology and [5]Meiji Univ., Japan*

16:45 F-2-2
Extrinsic Base Regrowth of p-InGaN for Npn-type GaN/InGaN Heterojunction Bipolar Transistor
T. Makimoto[1], K. Kumakura[1] and N. Kobayashi[2], *[1]NTT Basic Research Labs, NTT Corporation and [2]The Univ. of Electro-Communications, Japan*

17:00 F-2-3
Improvement of DC and RF characteristics of AlGaN/GaN HEMTs by thermally annealed Ni/Pt/Au Schottky gate
T. Nanjo[1], N. Miura[1], T. Oishi[1], M. Suita[1], Y. Abe[1], T. Ozeki[1], S. Nakatsuka[1], A. Inoue[1], T. Ishikawa[1] and Y. Matsuda[1], H. Ishikawa[2] and T. Egawa[2], *[1]Mitsubishi Electric Corporation and [2]Nagoya Inst. of Technology, Japan*

17:15 F-2-4
The improvement of DC performance in AlGaN/GaN HFET with isoelectronic Al doped channel
C.M. Jeon[1], J.-H. Lee[2], J.-H. Lee[2] and J.-L. Lee[1], *[1]POSTECH, and [2]Kyungpook National Univ., Korea*

Room G

G-2:Advanced Silicon Circuits and Systems
-Collaboration of Circuits and Devices-(16:15-17:45)
Chairs: M. Fujishima (Univ. of Tokyo)
T. Kuroda (Keio Univ.)

16:15 G-2-1 (Invited)
Performance of Deeply-Scaled, Power-Constrained Circuits
B. Nikolic[1], L. Chang[1], T.-J. King[1], *[1]Univ. of California, USA*

16:45 G-2-2
ESD Circuit Simulation Technology Using Protection Device Model with Generated-Hole-Dependent Base Resistance
Y. Tosaka[1], H. Anzai[1], K. Suzuki[1] and H. Oka[1], *[1]Fujitsu Labs Ltd., Japan*

17:05 G-2-3
A New Protection Circuit of IGBT (Insulated Gate Bipolar Transistor) for Short-Circuit Withstanding Capability
B.-C. Jeon[1], I.-H. Ji[1], M.-K. Han[1] and Y.-I. Choi[2], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

17:25 G-2-4
Dynamic Holding Voltage SCR (DHVSCR) Device for ESD Protection with high Latch-up Immunity
Z.-P. Chen[1] and M.-D. Ker[2], *[1]Industrial Technology Research Inst., Hsinchu, and [2]Inst. of Electronics, National Chiao-Tung Univ., Taiwan*

Room A

17:35 A-2-5
Eliminating Threshold Voltage Offset of PMOSFETs in High-Density DRAM
N. Takaura[1], R. Takemura[1], H. Matsuoka[1], R. Nagai[2], S. Yamada[2], H. Asakura[1] and S. Kimura[1], *[1]Hitachi, Ltd. and [2]Elpida Memory Inc., Japan*

17:55 A-2-6
Gate Engineering to prevent NMOS Dopant Channeling for Nano-Scale CMOSFET Technology
S.-H. Park[1] and H.-D. Lee[2], *[1]Hynix Semiconductor Inc. and [2]Chugiak National Univ., Korea*

Room B

Room C

17:35 C-2-5
Enhancement of dielectric constant due to expansion of lattice spacing in CeO_2 directly grown on Si (111)
D. Matsushita[1], Y. Nishikawa[1], N. Satou[2], M. Yoshiki[2], T. Shimizu[1], T. Yamaguchi[1], H. Satake[1] and N. Fukushima[1], *[1]Toshiba Corporation and [2]Toshiba Nanoanalysis Corporation, Japan*

18:30-20:30 Banquet (Eminence Hall)

Room D

17:35 D-2-5
HRTEM and EELS Analyses of Interfacial Nanostructures in Ti/$Si_{1-x}Ge_x$/Si(100)
J. Yamasaki[1], N. Tanaka[1], O. Nakatsuka[1], A. Sakai[2], S. Zaima[3] and Y. Yasuda[2], *[1]CIRSE, Nagoya Univ., [2]Nagoya Univ. and [3]CCRAST, Nagoya Univ., Japan*

17:55 D-2-6
Impact of NiSi Thermal Instability on Junction Shallowing Characterized with Damage-free n+/p Silicon Diodes
M. Tsuchiaki[1], K. Ohuchi[1] and C. Hongo[1], *[1]Toshiba Corporation, Japan*

Room E

17:30 E-2-5
High Brightness Si-based Quantum Dot Light Emitting Diode
M. Jo[1], N. Yasuhara[1], K. Kawamoto[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo and [2]PRESTO, JST, Japan*

17:45 E-2-6
Generation of Radiation Pressure in Thermally Induced Ultrasonic Emitter Based on Nanocrystalline Silicon
J. Hirota[1], H. Shinoda[2] and N. Koshida[1], *[1]Tokyo Univ. of A & T and [2]Univ. of Tokyo, Japan*

Room F

17:30 F-2-5
Drain Current DLTS of AlGaN/GaN MIS-HEMTs
T. Okino[1], M. Ochiai[1], Y. Ohno[1], S. Kisimoto[1], K. Maezawa[1] and T. Mizutani[1], *[1]Nagoya Univ., Japan*

17:45 F-2-6
Low damage, high selectivity $Ar/Cl_2/CH_4/O_2$ gate recess etching for AlGaN/GaN HEMT fabrication
W.-K. Wang[1], Y.-J. Li[1], C.-K. Lin[1], Y.-J. Chan[1], G.-T. Chen[1] and J.-I. Chyi[1], *[1]National Central Univ., Taiwan*

Room G

18:30-20:30 Banquet (Eminence Hall)

Wednesday, September 17

Room A

A-3: Advanced Silicon Devices and Device Physics
-High-k Technology I-
(9:00-10:30)
Chairs: M. Ogawa (Kobe Univ.)
T. Mogami (NEC)

9:00 A-3-1 (Invited)
Integration Issues of HfO_2-Al_2O_3 Laminate for Gate and Capacitor Dielectric
J.-H. Lee[1], [1]*Samsung Electronics Co., Ltd., Korea*

9:30 A-3-2
Influence of Carrier Velocity Related Parameters on the Propagation Delay Time of CMIS Inverters with High-k Gate Dielectrics
M. Ono[1] and A.Nishiyama[1], [1]*Toshiba Corporation, Japan*

9:50 A-3-3
A HfAlOx Gate Dielectric FET Technology Compatible with a Conventional Poly-Si Gate CMOS Process
H. Ohji[1], A. Mutoh[1], K. Torii[1], R. Mitsuhashi[1], A. Horiuchi[1], T. Maeda[1], H. Itoh[1], T. Kawahara[1], K. Hayashi[1], T. Sasaki[1], N. Kasai[1], H. Kitajima[1], M. Yasuhira[1], and T. Arikado[1], [1]*SELETE, Japan*

10:10 A-3-4
A Novel Approach for Determination of Tunneling Mass, m_{eff}-Conduction Band Offset Enegy, E_B Products for Advanced Gate Dielectrics
C.L. Hinkle[1], C. Fulton[1], R.J. Nemanich[1] and G. Lucovsky[1], [1]*North Carolina State Univ., USA*

Room B

B-3: Non-Volatile Memory Technologies
-Non-Volatile Memory III-
(9:00-10:20)
Chairs: K. Takasaki (Fujitsu Labs.)
H. Takada (Mitsubishi Electric)

9:00 B-3-1 (Invited)
Floating gate type nonvolatile memory reliability issues
G. Tempel[1], [1]*Infineon Technologies, Germany*

9:30 B-3-2 (Invited)
The Prospect of New Emerging Memories
H. Jeong[1] and K. Kim[1], [1]*Samsung Electronics, Korea*

10:00 B-3-3
Proposal of New Non-Volatile Memory with Magnetic Nano-Dots
T. Sakaguchi[1], M. Kobayashi[1], M. Takata[2], H. Choi[1], Y.G. Hong[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], [1]*Tohoku Univ. and* [2]*Asahi Glass Co.*

Room C

C-3: Silicon Process / Materials Technologies
-Memory Technology-
(9:00-10:30)
Chais: T. Kobayashi (Sony)
I. Asano (Elpida)

9:00 C-3-1 (Invited)
0.18 μm Embedded FRAM Fabrication Process and its Consistency with Conventional Logic LSI Process
Y. Horii and T. Eshita[1], [1]*Fujitsu Limited, Japan*

9:30 C-3-2
W-Polymetal Gate with Low W/Poly-Si Interface Resistance for High-Speed/High-Density Embedded Memory
T. Yamashita[1], Y. Nishida[1], K. Hayashi[1], T. Eimori[1], M. Inuishi[1] and Y. Ohji[1], [1]*Renesas Technology Corp., Japan*

9:50 C-3-3
Silicon Selective Epitaxial Growth for Self-Aligned Cell Contact Featuring High Performance Sub-100nm DRAM Cell Transistors
T. Kim[1], Y.P. Kim[1], B.C. Lee[1], S. Choi[1], U.I. Chung[1] and J.T. Moon[1], [1]*Samsung Electronics, Korea*

10:10 C-3-4
Optimum $TiSi_2$ Ohmic Contact Process for Sub-100nm Devices
H.S. Park[1], J.M. Lee[1], S.W. Lee[1], J.H. Park[1], K.J. Moon[1], S.B. Kang[1], G.H. Choi[1], U.I. Chung[1] and J.T. Moon[1], [1]*Samsung Electronics, Korea*

Break

Room D

D-3: Silicon-on-Insulator Technologies
-SOI Novel Devices-
(9:00-10:30)
Chairs: A. Ogura (NEC)
T. Nakai (SUMCO)

9:00 D-3-1 (Invited)
Strained Si MOSFETs on SiGe-on-Insulator (SGOI) for High Performance CMOS Technology
K. Rim[1], B.H. Lee[1], A. Mocuta[1], K. Jenkins[1], S. Bedell[1], H. Chen[1], D. Sadana[1], M. Gribelyuk[1], J. Ott[1], K. Chan[1], L. Shi[1], J. Chu[1], D. Boyd[1], P. Mooney[1], P. O'Neil[1], E. Leobandung[1], and J.J. Welser[1], [1]*SRDC, IBM, USA*

9:30 D-3-2
Fabrication of Ultra-Thin Strained Ge-on-Insulator Substrate by Ge-Condensation Technique
S. Nakaharai[1], T. Tezuka[1], N. Sugiyama[1], Y. Moriyama[1] and S. Takagi[1], [1]*MIRAI ASET, Japan*

9:50 D-3-3
Impact Ionization in Uniaxially Strained-Si MOSFET
N. Watanabe[1], Y. Maeda[1], M. Nishisaka[1] and T. Asano[1], [1]*CMS, Kyushu Inst. of Technology, Japan*

10:10 D-3-4
Quantum Confinement Effect of Ultrathin-SOI on double-gate-nMOSFETs
H. Watanabe[1], K. Uchida[1] and A. Kinoshita[1], [1]*Toshiba Corp., Japan*

Room E

E-3:Quantum Nanostructure Devices and Physics
-Characterization and Nanoprobing-
(9:00-10:15)
Chairs: H. Akinaga (AIST)
M. Sugawara (Univ. of Tokyo)

9:00 E-3-1
Optical characteristics of InAs/GaAs double quantum dots grown by MBE with Indium-Flush method
S. Yamauchi[1,2], K. Komori[1,2], T. Sugaya[1,2] and K. Goshima[1,2], [1]*AIST and* [2]*CREST-JST, Japan*

9:15 E-3-2
Molecular States of Coupled Zero-Dimensional Structures Imaged Using Low-Temperature Scanning Tunneling Spectroscopy
K. Kanisawa[1], S. Perraud[1,2], H. Yamaguchi[1] and Y. Hirayama[1,3], [1]*NTT Basic Research Labs,* [2]*ESPCI and* [3]*CREST-JST, Japan*

9:30 E-3-3
Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by AFM/Kelvin Probe Technique
Y. Darma[1], K. Takeuchi[1] and S. Miyazaki[1], [1]*Hiroshima Univ., Japan*

9:45 E-3-4
Magneto-luminescence of Interdiffused Self-Assembled Quantum Dots
S. Awirothananon[1,2], W. Sheng[1], A. Babinski[3], S. Studenikin[1], S. Raymond[1], P. Hawrylak[1], A. Sachrajda[1], M. Potemski[3], G. Ortner[4] and M. Bayer[4], [1]*National Research Council of Canada,* [2]*The Univ. of Ottawa, Canada,* [3]*MPI/FKF and CNRS, France and* [4]*Universitat Dortmund, Germany*

Room F

F-3:Compound Semiconductor Materials and Devices
-Novel Compound Semiconductors Devices-
(9:00-10:15)
Chairs: K. Akimoto (Tsukuba Univ.)
N. Kobayashi (The Univ. of Electro-Communications)

9:00 F-3-1 (Invited)
Optical and Electrical Control of Ferromagnetism in II-VI Quantum Wells
T. Dietl[1], [1]*Inst. of Physics, Polish Academy of Science, Poland*

9:30 F-3-2 (Invited)
Type-II InAs-based Quantum Cascade Lasers
K. Ohtani[1] and H. Ohno[1], [1]*RIEC, Tohoku Univ., Japan*

10:00 F-3-3
Fabrication of GaN/Alumina/GaN Structure to Reduce Dislocations in GaN
M. Hiroki[1], K. Kumakura[1], T. Makimoto[1], N. Kobayashi[2] and T. Kobayashi[1], [1]*NTT Corporation and* [2]*Univ. of Electro Communications, Japan*

Room G

G-3:Advanced Silicon Circuits and Systems
-Circuit Techniques for Emerging Technologies-
(9:00-10:30)
Chairs: K. Kotani (Tohoku Univ.)
M. Takamiya (NEC)

9:00 G-3-1 (Invited)
The challenge of analog mix-mode integrated circuit design for brain computer interface
Z. Wang[1], C. Zhang[1], and D. Li[1], [1]*Tsinghua Univ., P.R. China*

9:30 G-3-2
The Vision Chip with Electrical Fovea Motion
Y. Nakagawa[1], J. Deguchi[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], [1]*Tohoku Univ., Japan*

9:50 G-3-3
A Periodic Comparator Operating at 80GHz Based on Single-Flux-Quantum Technology with High Temperature Superconductor
H. Sugiyama[1,2], H. Wakana[2], S. Adachi[2], Y. Tarutani[2] and K. Tanabe[2], [1]*Toshiba Corporation and* [2]*Superconductivity Research Lab, Japan*

10:10 G-3-4
Ultra Small Random Number Generating Circuits With A Novel Noise Source Device
S. Yasuda[1], H. Satake[1], H. Nozaki[1], T. Tanamoto[1], R. Ohba[1], K. Uchida[1], A. Kinoshita[1] and S. Fujita[1], [1]*Toshiba Corporation, Japan*

Break

Break

Room A

A-4: Optoelectronic Devices and Photonic Crystal Devices
-VCSELs and Visible Lasers-
(10:45-12:00)
Chairs: T. Matsuo (NTT)
L.A. Coldren (Agility Communications)

10:45 A-4-1 (Invited)
1300nm-Range GaInNAsSb VCSELs
A. Kasukawa[1], H. Shimizu[1], C. Setiagung[1], M. Ariga[1], Y. Ikenaga[1], K. Kumada[1], T. Hama and N. Iwai[1], *[1]The Furukawa Electric Co., Ltd., Yokohama R&D Labs, Japan*

11:15 A-4-2
Improvement of High-Speed Oxide-Confined Vertical-Cavity Surface-Emitting Lasers
H.-C. Yu[1,2], S.-J. Chang[1], Y.-K. Su[1], C.-P. Sung[2], H.-P. Yang[2], C.-Y. Huang[2,3], Y.-W. Lin[2], J.-M. Wang[2], F.-I. Lai[4] and H.-C. Kuo[4], *[1]National Cheng Kung Univ., [2]Industrial Technology Research Inst., [3]National Tsing Hua Univ. and [4]National Chiao Tung Univ., Taiwan*

11:30 A-4-3
High-Power 200-mW 660-nm AlGaInP Laser Diodes with a Low Operating Current
R. Hiroyama[1], D. Inoue[1], S. Kameyama[1], A. Tajiri[1], M. Shono[1], M. Sawada[2] and A. Ibaraki[1], *[1]Sanyo electric Co., Ltd. and [2]Tottori Sanyo electric Co., Ltd., Japan*

Room B

B-4: Non-Volatile Memory Technologies
-Non-Volatile Memory IV-
(10:45-12:05)
Chairs: K. Yoshikawa (Toshiba)
T. Kobayashi (Hitachi)

10:45 B-4-1
A 0.18-μm Embedded MNOS-Type Non-volatile Memory for High-Frequency and Low-Voltage Operation
N. Matsuzaki[1], T. Ishimaru[1], Y. Okuyama[1], T. Mine[1], H. Kume[1], T. Hashimoto[2], Y. Kanamaru[2], T. Sakai[2], Y. Kawashima[2] and F. Ito[2], *[1]Hitachi, Ltd. and [2]Renesas Technology Corp., Japan*

11:05 B-4-2
70 nm SONOS Nonvolatile Memory Devices using FN Programming and Hot Hole Erase Method
S.D. Chae[1], C.J. Lee[2], J.H. Kim[1], S.K. Sung[2], J.S. Sim[2], M.K. Kim[1], S.W. Yoon[1], B.-G. Park[2], J.W. Lee and C.W. Kim[1], *[1]Samsung and [2]Seoul National Univ., Korea*

11:25 B-4-3
Excellent Electrical Characteristics of SONOS-type Flash Memory with High-k; Dielectric as Trapping Layer and Blocking Layer
M. Cho[1], S. Choi[1], H. Hwang[1] and J.W. Kim[2], *[1]Kwangju Inst. of Science and Technology and [2]Samsung Advanced Inst. of Technology, Korea*

Room C

C-4: Silicon Process / Materials Technologies
-DRAM-
(10:45-12:05)
Chais: M. Okuyama (Osaka Univ.)
K. Hieda (Toshiba)

10:45 C-4-1
Pt/BST/Pt Capacitor Technology for 0.15μm Embedded DRAM
Y. Tsunemine[1], T. Okudaira[1], K. Kashihara[1], A. Yutani[1], H. Shinkawata[1], M. K. Mazumder[1], M. Yoneda[1], Y. Okuno[2], A. Tsuzumitani[2] and Y. Mori[2], *[1]Mitsubishi Electric Corp. and [2]Matsushita Electronics Corp., Japan*

11:05 C-4-2
Low Resistive Contacts of TiN-Barrier and Ru-Electrode Using PCM Sputtering for MIM-Ta_2O_5 Capacitors in Giga-Bit DRAMs
Y. Nakamura[1], T. Kawagoe[1], H. Sakuma[1], H. Yamaguchi[1], I. Asano[1], M. Horikawa[1], K. Kuroki[1], K. Tanaka[1], Y. Ueda[1] and H. Goto[1], *[1]Elpida Memory, Inc., Japan*

11:25 C-4-3
A Noble SiON/AlO Structure at High-k/poly-Si Interface for Storage Capacitors of High Density DRAMs
O. Tonomura[1] and H. Miki[1], *[1]Hitachi, Ltd., Japan*

Room D

D-4: Silicon-on-Insulator Technologies
-SOI Device Physics-
(10:45-12:05)
Chairs: O. Nishio (Sharp)
T-J. King (UCB)

10:45 D-4-1
Variable Body Effect Factor FD SOI MOSFET for Ultra-Low Power VTCMOS Applications
T. Ohtou[1], T. Nagumo[1] and T. Hiramoto[1], *[1]Univ. of Tokyo, Japan*

11:05 D-4-2
Novel SOI MOSFET with Buried Back-Gate
H. Oh[1], H. Choi[1], T. Sakaguchi[1], J. C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ., Japan*

11:25 D-4-3
Modeling of Fully-depleted SOI Device Variation
H. Komatsubara[1], K. Kishiro[1], Y. Kawai[2], N. Miura[1] and K. Fukuda[1], *[1]Oki Electric Industry Co., Ltd. and [2]Miyagi Oki Electric Industry Co., Ltd., Japan*

Room E

10:00 E-3-5
Optical Time-of-Flight Study of Lateral Exciton Transport in a Strained $Si_{1-x}Ge_x$/Si Multiple Quantum Well
K. Sawada[1], N. Yasuhara[1] and S. Fukatsu[1,2], *[1]The Univ. of Tokyo, Graduate School of Arts and Sciences and [2]PRESTO, JST, Japan*

Break

E-4: Quantum Nanostructure Devices and Physics
-Spin-related Phenomena-
(10:45-12:15)
Chairs: A. Takeuchi (Waseda Univ.)
T. Dietl (Polish Academy of Science)

10:45 E-4-1 (Invited)
Control of ferromagnetic order in selectively p-doped GaMnAs-based heterostructures
M. Tanaka[1,2], and A. M. Nazmul[1,2], *[1]Univ. of Tokyo, Department of Electronic Engineering, [2]PRESTO-JST, Japan*

11:15 E-4-2
Effect of Internal Exchange Coupling on the Curie Temperature in $Ga_{1-x}Mn_xAs$ Trilayer Structures
S. Yuldashev[1], Y. Kim[1], N. Kim[1], H. Im[1], T. W. Kang[1], S. Lee[2], Y. Sasaki[3], X. Liu[3] and J. Furdyna[3], *[1]Dongguk Univ., Korea, [2]Korea Univ., Korea and [3]Univ. of Notre Dame, USA*

11:30 E-4-3
Magnetic Properties of Submicron-sized *p*-$In_{0.97}Mn_{0.03}As$ Ferromagnetic Semiconductor
Y. Sekine[1], J. Nitta[1,2], T. Koga[1,3], A. Oiwa[3,4], S. Yanagi[4], T. Slupinski[5] and H. Munekata[4], *[1]NTT [2]CREST [3]PRESTO-JST [4]Tokyo Inst. of Technology, Japan and [5]Warsaw Univesity, Poland*

Room F

F-4: Compound Semiconductor Materials and Devices
-Optical Devices-
(10:45-12:15)
Chaisr: T. Matsuoka (NTT)
M. Ikeda (Sony)

10:45 F-4-1 (Invited)
Developments of High Efficiency In GaN-Based Light-Emitting Diodes
J.-I. Chyi[1], C.-C. Pan[1], C.-M. Lee[1], W.-J. Hsu[1], and C.-S. Fang[1], *[1]National Central Univ., Taiwan*

11:15 F-4-2
InGaN-based horizontal cavity surface emitting laser diode with selectively grown cavity and outer micromirrors
T. Akasaka[1], T. Nishida[1], T. Makimoto[1] and N. Kobayashi[1], *[1]NTT Basic Research Labs, NTT Corporation, Japan*

11:30 F-4-3
Sub-mW Operation of 308 nm Deep UV LED using quaternary InAlGaN
H. Hirayama[1] and Y. Aoyagi[2], *[1]RIKEN and [2]Tokyo Inst. of Technology, Japan*

Room G

G-4: System-Level Integration and Packaging Technologies
-System-Level Integration and Packaging Technologies I-
(10:45-11:45)
Chairs: K. Fujimoto (Osaka Univ.)
M. Kada (Sharp)

10:45 G-4-1 (Invited)
3D System Integration by Chip-to-Wafer Stacking Technologies
P. Ramm[1], A. Klumpp[1], R. Merkel[1], J. Weber[1], R. Wieland[1], G. Elst[2] *[1]Fraunhofer Inst., Germany*

11:15 G-4-2
Micro Cu Bump Interconnection on 3D Chip Stacking Technology
K. Tanida[1], M. Umemoto[1], N. Tanaka[1], Y. Tomita[1] and K. Takahashi[1], *[1]ASET, Japan*

11:30 G-4-3
Copper Electrodeposition of High-Aspect-Ratio Vias for Three Dimensional Packaging
K. Kondo[1], T. Yonezawa[1], M. Tomisaka[2], H. Yonemura[2], M. Hoshino[2], Y. Taguchi[2] and K. Takahashi[2], *[1]Okayama Univ. and [2]ASET, Japan*

Room A	Room B	Room C
11:45 A-4-4 High power and high temperature operation of 660 nm AlGaInP laser diodes for DVD-R/RW Y. Yoshida, H. Nishiguchi, M. Sasaki, S. Abe, A. Ohno, K. Ono, M. Takemi, J. Horie, T. Yagi and E. Omura, [1]*Mitsubishi Electric Corporation, Japan*	**11:45 B-4-4** Data retention improvement of MONOS memories by using silicon-tetrachloride-based silicon nitride with ultra-low Si-H bond density K. Nomoto[1], G. Asayama[1] and T. Kobayashi[1], [1]*Sony Corporation , Japan*	**11:45 C-4-4** A Highly Reliable TiN/Al_2O_3/TiN MIM Technology for Embedded DRAMs L.-L. Chao[1], C.D. Wu[1], H.L. Lin[1], Y.L. Tu[1], K.Y. Lin[1], C.Y. Yu[1], C.Y. Chen[1], F.J. Shiu[1], C.T. Ho[1], C.S. Tsai[1], S.-G Wuu and C. Wang[1], [1]*Taiwan Semiconductor Manufacturing Company, Ltd, Taiwan*

Lunch

13:00-15:00 Poster Session (Ohgi)

Room D	Room E	Room F	Room G
11:45 D-4-4 Temperature Dependence of Threshold Voltage and Hot Carrier Degradation of Dynamic Threshold SOI-pMOSFET Y.-J. Lee[1], T.-S. Chao[1, 2], C.-Y. Huang[1], H.-C. Lin[2] and T.-Y. Huang[1], [1]*National Chiao Tung Univ., Taiwan and* [2]*National Nano Device Labs., Taiwan*	**11:45 E-4-4** Analysis and Control of Rashba Spin-Spliting in One-Dimensional Conductors at Narrow-Gap Single Heterojunctions T. Kakegawa[1], T. Kita[2], T. Sato[1], M. Akabori[1] and S. Yamada[1], [1]*CNMT, JAIST and* [2]*RIEC, Tohoku Univ., Japan*	**11:45 F-4-4** Low Temperature p-GaN rough layer on $In_{0.23}Ga_{0.77}N$/GaN MQW LEDs L.W. Wu[1], S.J. Chang[1], Y.K. Su[1], W.C. Lai[1,2] and J.K. Sheu[3], [1]*National Cheng Kung Univ.,* [2]*South Epitaxy Corporation and* [3]*National Central Univ., Taiwan*	
	12:00 E-4-5 Au/GaAs magnetoresistive-switch-effect devices fabricated by wet etching Z.G. Sun[1], M. Mizuguchi[1] and H. Akinaga[1], [1]*SYNAF, AIST, Japan*	**12:00 F-4-5** Improvement of AlGaInP MQW Light Emitting Diodes by Modification of Ohmic Contact Layer H.-C. Wang[1], Y.-K. Su[1], C.-L. Lin[1], S.-M. Chen[2] and W.-L. Li[2], [1]*Inst. of Microelectronics and Department of Electrical Engineering and* [2]*Epitech Technology Corporation, Taiwan*	

Lunch

13:00-15:00 Poster Session (Ohgi)

Room A

A-5: Optoelectronic Devices and Photonic Crystal Devices
-Optoelectronic Integrated Devices-
(15:15-16:45)
Chairs: T. Nishimura (Mitsubishi Electric)
S. Lee (KIST)

15:15 A-5-1 (Invited)
Monolithic PD-EAM Optical Gates for Ultrafast Signal Processing
S. Kodama[1], T. Yoshimatsu[1] and H. Ito[1], [1]*NTT Corporation, Japan*

15:45 A-5-2
InP-based OEIC Photoreceivers Using Shared Layer Integration Technology of Heterojunction Bipolar Transistors and Refracting-Facet Photodiodes
B. Lee[1], Y. Song[1] and K. Yang[1], [1]*KAIST, Korea*

16:00 A-5-3
Solid-State Optical Routing Device Utilizing Minority Carrier Drift
H. Tsukamoto[1], T.D. Boone[1] and J.M. Woodall[1], [1]*Yale Univ., USA*

16:15 A-5-4
Analysis of AlGaAs/GaAs Heterojunction Photodetector with a Two-Dimensional Channel Modulated by Gate Voltage
H. Song and H. Kim, *Korea Electronics Technology Inst., Korea*

Room B

B-5: Organic Semiconductor Devices and Materials
-Preparation and Characterization-
(15:15-16:30)
Chairs: F. Kaneko (Niigata Univ.)
O. Sugihara (Tohoku Univ.)

15:15 B-5-1
Controlling the Morphology of Nanostructured Poly(fluoreneethynylene) Film by a Simple Method
K. Tada[1] and M. Onoda[1], [1]*Himeji Inst. of Technol, Japan*

15:30 B-5-2
Anomalous Growth Temperature Dependence of the Surface Roughness of Pentacene Thin Films
M. Tejima[1], T. Komoda[1], K. Kita[1], K. Kyuno[1] and A. Toriumi[1], [1]*The Univ. of Tokyo, Japan*

15:45 B-5-3
Fabrication and Photoelectrochemical Properties of Polythiophene-Porphyrin Composite Films
T. Akiyama[1], K. Kakutani[1] and S. Yamada[1], [1]*Kyushu Univ., Japan*

16:00 B-5-4
High Resolution Pattern Recording on Photosensitive Urethane-Urea Copolymer Film Surface by Laser Irradiation through Photo-mask
Y. Che[1], O. Sugihara[1], N. Okamoto[1], M. Tomiki[1], M. Tsuchimori[2] and O. Watanabe[2], [1]*Shizuoka Univ. and* [2]*Toyota Central Research and Development Labs Inc., Japan*

Room C

C-5: Silicon Process / Materials Technologies
-Interconnect-
(15:15-16:45)
Chais: N. Kobayashi (Selete)
T. Nakamura (Fujitsu Labs.)

15:15 C-5-1 (Invited)
Stress Migration Phenomena of Cu interconnects
T. Oshima[1], K. Ishikawa[1], T. Saito[1], H. Aoki[1] and K. Hinode[1], [1]*Hitachi, Ltd., Japan*

15:45 C-5-2
Mechanical property control of Low-k Dielectrics for Diminishing CMP-related Defects in Cu-damascene Interconnects
K. Hijioka[1], F. Ito[1], M. Tagami[1], H. Ohtake[1], T. Takeuchi[1], S. Saitoh[1] and Y. Hayashi[1], [1]*NEC Corporation, Japan*

16:05 C-5-3
The Delamination Mechanism of Porous Low-k Film during the Cu-CMP Process
S. Kondo[1], T. Nasuno[1], S. Ogawa[1], S. Tokitou[1], B. U. Yoon[1], A. Namiki[2], Y. Sone[2], K. Misawa[1], T. Yoshie[1], K. Yoneda[1], M. Shimada[1], S. Sone[1], H.J. Shin[1], N. Ohashi[1], I. Matsumoto[1] and N. Kobayashi[1], [1]*SELETE and* [2]*Novellus Systems Japan, Inc., Japan*

16:25 C-5-4
In-situ Measurement of Friction Force during Cu Chemical Mechanical Polishing
H. Matsuo[1], A. Ishikawa[1] and T. Kikkawa[2,3], [1]*MIRAI-ASET,* [2]*MIRAI-ASRC, AIST and* [3]*RCNS, Hiroshima Univ., Japan*

Room D

D-5: Silicon-on-Insulator Technologies
-Fin FET Technologies-
(15:15-16:45)
Chairs: H. Matsuhashi (Oki Electric)
K. Rim (IBM)

15:15 D-5-1 (Invited)
FinFET Promise and Challenges
T.-J. King[1], [1]*Univ. of California, USA*

15:45 D-5-2
High-Aspect Ratio Gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation of Silicon Gate
A. Katakami[1], K. Kobayashi[2] and H. Sunami[2], [1]*Fujitsu Labs Limited and* [2]*Hiroshima Univ., Japan*

16:05 D-5-3
An Experimental Study of The Cross-Sectional Channel Shape Dependence of Short-Channel Effects in Fin-Type Double-Gate MOSFETs
Y. Liu[1], K. Ishii[1], M. Masahara[1], T. Tsutsumi[2], H. Takashima[1] and E. Suzuki[1], [1]*AIST and* [2]*Meiji Univ., Japan*

16:25 D-5-4
P-channel Vertical Double-Gate MOSFET Fabrication by Ion-Bombardment-Retarded Etching
M. Masahara[1], T. Matsukawa[1], S. Hosokawa[1], K. Ishii[1], Y. Liu[1], H. Tanoue[1], K. Sakamoto[1], H. Yamauchi[1], S. Kanemaru[1] and E. Suzuki[1], [1]*AIST, Japan*

Room E

E-5:Quantum Nanostructure Devices and Physics
-Single Electron Transport-
(15:15-16:30)
Chairs: Y. Ohno (Tohoku Univ.)
A. Shields (Toshiba Cambridge)

15:15 E-5-1 (Invited)
Nuclear spin dependent transport in quantum dots
K. Ono[1], and S. Tarucha[1,2,3], [1]*Univ. of Tokyo,* [2]*NTT Basic Research Labs,* [3]*ERATO-JST, Japan*

15:45 E-5-2
Single Electron Transport through Single InAs Quantum Dots Probed by Nanogap Electrodes
M. Jung[1] and K. Hirakawa[1,2], [1]*Univ. of Tokyo and* [2]*CREST-JST, Japan*

16:00 E-5-3
Investigation of Electron Transition Energy for Vertically Coupled InAs/GaAs Semiconductor Quantum Dots and Rings
Y. Li[1,2] and H.-M. Lu[3], [1]*National Nano Device Labs,* [2]*National Chiao Tung University and* [3]*Univ. of Illinois at Chicago, USA*

16:15 E-5-4
1-bit BDD full adder circuit using single electron transistors by selective area metalorganic vapor phase epitaxy
Y. Miyoshi[1], F. Nakajima[2], J. Motohisa[1] and T. Fukui[1], [1]*Hokkaido Univ. and* [2]*NTT, Japan*

Room F

F-5:Micro-Nano Electromechanical Devices for Bio- and Chemical Applications
-Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - I-
(15:15-16:45)
Chaisr: Y. Miyahara (NIMS)
M. Kamahori (Hitachi)

15:15 F-5-1 (Invited)
DNA Chips and Their Medical Applications
P. Fortina[1], L.J. Kricka[2], and S. Surrey[1], [1]*Thomas Jefferson Univ., USA* [2]*Hospital of the Univ. of Pennsylvania*

15:45 F-5-2
Bioluminometry by CMOS-based active pixel photodiode array with accurate background noise compensation
Y. Yazawa[1], M. Kamahori[1] and H. Kambara[1], [1]*Hitachi, Ltd., Japan*

16:00 F-5-3
Detection of DNA Molecules Using Insulated Gate Field Effect Transistor and Intercalator
T. Sakata[1], H. Otsuka[1] and Y. Miyahara[1], [1]*Biomaterials Research Center, National Inst. for Materials Science, Japan*

16:15 F-5-4
Electrostatic Immobilization of Biomolecules using Nano-Electrode Array
T. Yamamoto[1] and T. Fujii[1], [1]*The Univ. of Tokyo, Japan*

Room G

G-5:System-Level Integration and Packaging Technologies
-System-Level Integration and Packaging Technologies II-
(15:15-16:45)
Chairs: K. Takahashi (ASET.)
M. Kimura (Mitsubishi Electric)

15:15 G-5-1 (Invited)
Design, Manufacturing and Infrastructure for All-in-One SiP Solution
T. Fujitsu[1], [1]*J-SiP Walton, Japan*

15:45 G-5-2 (Invited)
System Packaging and Embedded WLP Technologies for Mobile Products
T. Wakabayashi[1], [1]*Casio, Japan*

16:15 G-5-3
Evaluation of Hot-Carrier Hardness and Thick-Film Formation with STP Technique for Seamless Integration Technology
N. Sato[1], N. Shimoyama[1], T. Kamei[2], K. Kudou[2], M. Yano[2], H. Ishii[1] and K. Machida[1], [1]*NTT Corporation and* [2]*NTT Advanced Technology Corporation, Japan*

16:30 G-5-4
New Process of Self-organized Interconnection in Packaging by Conductive Adhesive with Low Melting Point Filler
K. Yasuda[1], J.-M. Kim[1], M. Yasuda[1] and K. Fujimoto[1], [1]*Osaka Univ., Japan*

Room A

16:30 A-5-5
Enhancement of Magneto-Optic Effect in Magneto-Optic Waveguide with Low Refractive Index Undercladding Layer
Y. Shoji[1,2], H. Yokoi[1,2] and T. Mizumoto[1], *[1]Tokyo Inst. of Technology and [2]OITDA, Japan*

A-6: Optoelectronic Devices and Photonic Crystal Devices
-Lasers for Optical Communication-
(17:00-18:15)
Chairs: H. Shimizu (The Furukawa Electric)
M. Nielsen (Denmark Tech. Univ.)

17:00 A-6-1 (Invited)
Advances in Widely -Tunable Optical Transmitters
L.A. Coldren[1], *[1]Agility Communications and UC-Santa Barbara, USA*

17:30 A-6-2
40 GHz Actively Mode-Locked DBR Laser Diode Module with an Impedance Matching Circuit
S. Arahira[1] and Y. Ogawa[1], *[1]Oki Electric Industry Co., Ltd., Japan*

17:45 A-6-3
Very High Frequency Self-Pulsation and Stable Optical Injection Locking for Well-Difined Multi-Electrode DFB Lasers
S. Nishikawa[1,2], M. Gotoda[1,2], T. Nishimura[1,2], Y. Tokuda[1,2] and K. Matsumoto[1,2], *[1]Mitsubishi Electric Corporation and [2]OITDA, Japan*

Room B

16:15 B-5-5
Electrical Properties and Gas Response in Alternate Layer-by-Layer Films of Copper Phthalocyanine Dyes
K. Kato[1], N. Watanabe[1], S. Katagiri[1], K. Shinbo[1], F. Kaneko[1] and R.C. Advincula[2], *[1]Niigata Univ. and [2]Univ. of Houston, Japan*

B-6: Non-Volatile Memory Technologies
-Non-Volatile Memory V-
(17:00-17:40)
Chairs: K. Saito (NEC)
H. Takada (Mitsubishi Electric)

17:00 B-6-1
Hot Carrier Injection / Fowler Nordheim Erase Silicon Nanocrystal Memory Cell
Rajesh Rao[1], Robert Steimle[1], M. Sadd[1], C. Swift[1], R. Muralidhar[1], B. Hradsky[1], S. Straub[1], E. Prinz[1], J. Yater[1] and B. White[1], *[1]Motorola SPS, USA*

17:20 B-6-2
A New Investigation on Erase V_T Variation of NOR Flash fabricated with 90 nm Technology
T.Y. Kim[1], W.H. Lee[1], J.I. Han[1], S.E. Lee[1], H.G. Lee[1], S.Y. Kim[1], J.H. Park[1], M.K. Cho[1], Y.H. Song[1] and K. Kim[1], *[1]Samsung Electronics, Korea*

Room C

C-6: Silicon Process / Materials Technologies
-Interconnect-
(17:00-18:20)
Chais: S. Saito (NEC)
J. Koike (Tohoku Univ.)

17:00 C-6-1
High-modulus Porous MSQ Films for Cu/Low-k Integration (keff<2.7)
K. Misawa[1], S. Sone[1], H. Shin[1], K. Inukai[1], Y. Sudo[1], S. Kondo[1], B.U. Yoon[1], S. Tokitoh[1], K. Yoneda[1], T. Yoshie[1], N. Ohashi[1] and N. Kobayashi[1], *[1]SELETE, Japan*

17:20 C-6-2
Control of Pore Size and Porosity in Periodic Porous Silica Low-k Films
N. Hata[1,2], C. Negoro[2], K. Yamada[3] and T. Kikkawa[1,4], *[1]MIRAI-ASRC, AIST, [2]ASRC, AIST, [3]MIRAI-ASET and [4]RCNS, Hiroshima Univ., Japan*

17:40 C-6-3
Off-time Dependence of Pulsed DC Electromigration MTF of Cu Multilevel Interconnection
K. Oshima[1], T. Ishida[1], S. Miyazaki[1], T. Takahagi[1] and S. Shingubara[1], *[1]Hiroshima Univ., Japan*

Room D

D-6: New Materials and Characterization
-Si/SiGe Devices and Materials-
(17:00-18:30)
Chairs: J. Murota (Tohoku Univ.)
A. Sakai (Nagoya Univ.)

17:00 D-6-1 (Invited)
SiGe in Advanced CMOS Devices-an unique material equally helpful when present or absent
T. Skotnicki[1], *[1]STMicroelectronics, Crolled, France*

17:30 D-6-2
Structural Characterization of Strained Silicon Substrates by X-Ray Diffraction and Reflectivity
M. Erdtmann[1], T. Langdo[1], C. Vineis[1], H. Badawi[1] and M. Bulsara[1], *[1]AmberWave Systems Corp., USA*

17:50 D-6-3
Oxidation-Induced Damages on Germanium MIS Capacitors with HfO_2 Gate Dielectrics
K. Kita[1], M. Sasagawa[1], K. Tomida[1], K. Kyuno[1] and A. Toriumi[1], *[1]The Univ. of Tokyo, Japan*

Room E

E-6:Novel Devices, Physics, and Fabrication
-Nanoprocess and Nanodevices-
(17:00-18:30)
Chairs: M. Tabe (Sizuoka Univ.)
Y. Takahashi (NTT)

17:00 E-6-1 (Invited)
Nanoimprint Lithography–An Enabling Engine to Nanotechnology
S.Y. Chou[1], *[1]Princeton Univ., USA*

17:30 E-6-2
Photon-induced effect on single-charge-tunneling in a Si multidot Schottky FET
R. Nuryadi[1], H. Ikeda[1], Y. Ishikawa[1] and M. Tabe[1], *[1]Shizuoka Univ., Japan*

17:45 E-6-3
Room-Temperature Observation of Negative Differential Conductance Due to Large Quantum Level Spacing in Silicon Single-Electron Transistor
M. Saitoh[1] and T. Hiramoto[1], *[1]Univ. of Tokyo, Japan*

Room F

16:30 F-5-5
Microfluidic Devices Integrated with Parmalloy Micropatterns for Manipulating Magnetic Beads
N. Ichikawa[1], F. Omasu[2], Y. Nagasaki[3] and T. Ichiki[1,2], *[1]Toyo Univ., [2]PRESTO and [3]Tokyo Univ. of Science, Japan*

F-6:Micro-Nano Electromechanical Devices for Bio- and Chemical Applications
-Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - II-
(17:00-18:00)
Chairs: H. Tabata (Osaka Univ.)
K. Shimoide (Asahi Kasei)

17:00 F-6-1 (Invited)
Development of an integrated a-Si:H photodiode detector and its evaluation for chemical and biochemical microfluidic analysis
T. Kamei[1,3], B.M. Paegel[1], E.T. Lagally[1], A.M. Skelley[1], J.R. Scherer[1], R.A. Street[2], and R.A. Mathies[1], *[1]Univ. of California at Barkeley and [2]Palo Alto Research Center*

17:30 F-6-2
Resonant Cavity Thin Film Photodiode for Compact Displacement Sensor
M. Sasaki[1], F. Nakai, X. Mi, K. Hane, *[1]Tohoku Univ., Japan*

17:45 F-6-3
RF Propagation Characteristics and pH Measurement for in vivo Wireless Healthcare Chip
T. Yamada[1], H. Uesugi[1], K. Okada[1], K. Masu[1], H. Nakase[2], T. Kazuo[2], A. Oki[3] and Y. Horiike[3] *[1]Tokyo Inst. of Technology, [2]RIEC, Tohoku Univ. and [3]National Inst. for Materials Science, Japan*

Room G

G-6:System-Level Integration and Packaging Technologies
-System-Level Integration and Packaging Technologies III-
(17:00-18:15)
Chairs: M. Aoyagi (AIST)
H. Ezawa (Toshiba)

17:00 G-6-1 (Invited)
AC Coupled Interconnect for High-Density High-Bandwidth Packaging
P. Franzon[1], S. Mick[1], J. Wilson[1], L. Luo[1], K. Chandrasakhar[1], *[1]NC State Univ., USA*

17:30 G-6-2
Inter-chip Wireless Interconnection using Si Integrated Antenna
A.B.M. H.-U. Rashid[1], S. Watanabe[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*

17:45 G-6-3
Magnetic Near-Field Mappings over Fine Circuits by Fiber-Edge Magneto-Optic Probe
M. Iwanami[1], S. Hoshino[1], M. Kishi[2] and M. Tsuchiya[2], *[1]ASET and [2]Univ. of Tokyo, Japan*

Room A

18:00 A-6-4

Lasing-Wavelength-Change-Suppression 980 nm Pump Laser Diodes for Metro Applications

K. Kawasaki[1], K. Shigihara[1], H. Matsuoka[1], Y. Kunitsugu[1], T. Yagi[1], E. Omura[1] and Y. Mitsui[1], [1]*Mitsubishi Electric Corporation, Japan*

18:45-20:45
Rump Session A

"Can channel material/structure engineering become a guiding principle for future CMOS device technology?"

Room B

18:45-20:45
Rump Session B

"What paradigm can nanoelectronic devices bring about?"

Room C

18:00 C-6-4

CVD-Al/Flow-Al Technology for Filling Large Aspect Ratio Contact Holes

M. Sakamoto[1], T. Aoki[1], K. Masu[1], S.J. Lim[2], M. Hatanaka[2], M. Ishikawa[2] and Y. Furumura[3], [1]*Tokyo Inst. of Technology,* [2]*ULVAC Inc. and* [3]*Philbridge Inc., Japan*

Room D

18:10 D-6-4

Enhanced Metal-Induced Lateral Crystallization in Amorphous Ge/Si Layered Structure by Precursor Modulation

H. Kanno[1], A. Kenjo[1], T. Sadoh[1] and M. Miyao[1], [1]*Kyushu Univ., Japan*

Room E

18:00 E-6-4

Analytical SPICE Modeling of Realistic MOS-based Single-Electron Transistors –"MOSETs" with a Unique Distribution Function in the Coulomb Oscillation Region

K.R. Kim[1], K.-W. Song[1], G. Baek[1], H.H. Kim[1], J.I. Huh[1], J.D. Lee[1] and B.-G. Park[1], [1]*Seoul National Univ., Korea*

18:15 E-6-5

Analysis of Back-Gate Voltage Dependence of Threshold Voltage of Thin SOI MOSFET and Its Application to Si Single-Electron Transistor

S. Horiguchi[1], A. Fujiwara[1], H. Inokawa[1] and Y. Takahashi[1], [1]*NTT Basic Research Labs, Japan*

Room F

Room G

18:00 G-6-4

Variable RF Inductor on Si CMOS Chip

S. Gomi[1], Y. Yokoyama[1], H. Sugawara[1], H. Ito[1], K. Okada[1], H. Hoshino[2], H. Onodera[2] and K. Masu[1], [1]*Tokyo Inst. of Technology, and* [2]*Kyoto Univ., Japan*

POSTER SESSION (13:00-15:00, OHGI)

P1 Advanced Silicon Circuits and Systems
(6 Papers)

P1-1
Bank-Type Multiport Register File for Highly-Parallel Processors
T. Sueyoshi[1], H. Uchida[1], Y. Mitani[2], K. Hiramatsu[2], H.J. Mattausch[1], T. Koide[1] and T. Hironaka[2], *[1]Hiroshima Univ. and [2]Hiroshima City Univ., Japan*

P1-2
Three-Dimensionally Stacked Analog Retinal Prosthesis Chip
J. Deguchi[1], T. Watanabe[1], T. Nakamura[1], Y. Nakagawa[1], J.-C. Shim[1], H. Kurino[1] and M. Koyanagi[1], *[1]Tohoku Univ., Japan*

P1-3
Low-Voltage-Triggered PNP for ESD Protection in Mixed-Voltage I/O interface
M.-D. Ker[1], W.-J. Chang[1] and W.-Y. Lo[2], *[1]National Chiao-Tung Univ., and [2]Silicon Intergrated Systems (SiS) Corp., Taiwan*

P1-4
75-qubit Quantum Computing Emulator
M. Fujishima[1], K. Inai[1], T. Kitasho[1] and K. Hoh[1,2], *[1]The Univ. of Tokyo and [2]CREST-JST, Japan*

P1-5
Efficient Suppression of Substrate Noise Coupling in CMOS Technology
W.-K. Yeh[1], S.-M. Chen[2], C.-M. Lai[2] and Y.-K. Fang[2], *[1]National Univ. of Kaohsiung and [2]National Cheng-Kung Univ., Taiwan*

P1-6
All Digital One-chip Wireless Modem LSI with Acquisition Circuit
Y. Sakai[1], H. Nakase[1], Y. Isota[1] and K. Tsubouchi[1], *[1]Tohoku Univ., Research Inst. of Electorical Communication, Japan*

P2 Advanced Silicon Devices and Device Physics
(17 Papers)

P2-1
Efficient Improvement of Hot-Carrier-Induced Degradation for Sub-0.1μm CMOSFET
C.-M. Lai[1], C.-C. Hu[2], J.-C. Lin[3], S.-T. Pan[2] and W.-K. Yeh[4], *[1]Inst. of National Cheng Kung Univ., [2]Shu-Te Univ., [3]National Chiao-Tung Univ. and [4]National Univ. of Kaohsiung, Taiwan*

P2-2
Optimization of STI Stress and Active Geometry Configuration for Advanced CMOS Devices
T. Lin[1], Y. Gong[1], J.T. Tseng[1], L. Yu[1], T. Shen[1], D. Chen[1], T.P. Chen[1], C.L. Kuo[1], W.T. Shiau[1] and J.K. Chen[1], S.C. Chien and S.W.Sum, *[1]United Microelectronics Corporation, Taiwan*

P2-3
Modeling of Pocket Implant Effect on Drain Current Flicker Noise in High Performance Analog CMOS Devices
J.-W.Wu[1], J.C. Guo[2], K.-L. Chiu[1], C.-C. Cheng[1], W.Y. Lien[2], G.W. Huang[3] and T. Wang[1], *[1]National Chiao-Tung Univ., [2]Taiwan Semiconductor Manufacturing Company, and [3]National Nano Device Labs, Taiwan*

P2-4
Novel Substrate Engineering for High Performance CMOSFETs using Channeling Ion Implantation
M. Kitazawa[1], T. Yamashita[1], Y. Kawasaki[1], T. Kuroi[1], T. Eimori[1], M. Inuishi[1] and Y. Ohji[1], *[1]Renesas Technology Corp., Japan*

P2-5
A New Stable Extraction of Threshold Voltage Using Regularization Method
W.Y. Choi[1,2], B.Y. Choi[1,2], D.-S. Woo[1,2], M.W. Lee[1,2], J.D. Lee[1,2] and B.-G. Park[1,2], *[1]Inter-univ. Semiconductor Research Center (ISRC) and [2]Seoul National Univ., Korea*

P2-6
A New Approach to Gate Dielectric Integrity Based on Differences Between i)Strained and ii) Strain-Free Interfacial Regions: *Applications to Devices with Alternative High-k Dielectrics*
G. Lucovsky[1], J.C. Phillips[2] and P. Boolchand[3], *[1]North Carolina State Univ., [2]Rutgers Univ. and [3]Univ. of Cincinnati, USA*

P2-7
A Variable Channel-Size MOSFET with LDD Structure
N. Nakanose[1], Y. Arima[1], T. Asano[1], Y. Kosasayama[2], M. Ueno[2] and M. Kimata[2], *[1]Kyushu Inst. of Technology and [2]Mitsubishi Electric Corp., Japan*

P2-8
Novel ESD Protection Design for Nanoscale CMOS Integrated Circuits
M.-D. Ker[1] and T.-K. Tseng[2], *[1]National Chiao-Tung Univ., Taiwan and [2]Industrial Technology Research Inst., Taiwan, Taiwan*

P2-9
A New One-Transistor One-Bipolar (1T1B) Capacitor-Less DRAM Cell
J.-K. Park[1] and J. Woo[1], *[1]Univ. of California at Los Angeles, USA*

P2-10
On-current Modeling of poly-Si TFT
K.C. Moon[1], S.-H. Kang[1] and M.-K. Han[1], *[1]Seoul National Univ., Korea*

P2-11
Characterization and Modeling of High Q-Factor, High Resonant Frequency Spiral Inductors with 6 μm thick Top-Metal for RF-IC Applications
Y.-S. Lin[1], H.-W. Chiu[2], S.-H. Wu[1] and S.-S. Lu[2], *[1]National Chi-Nan Univ., [2]National Taiwan Univ., Taiwan*

P2-12
Design Issues for Sub-100nm Analog CMOS
M. Garg[1], S. Suryagandh[1] and J. Woo[1], *[1]Univ. of California Los Angeles, USA*

P2-13
Split Gate Engineering for RF/Analog Application In Sub 50 nm NMOSFET
J. Yuan[1] and J. Woo[1], *[1]Univ. of California, Los Angeles, USA*

P2-14
A Simple Wide-Band MIM Capacitor Model for RF Applications and the Effect of Substrate Grounded Shields
S.-S. Song[1], S.-W. Lee[1], J. Gil[1] and H. Shin[2], *[1]Korea Advanced Insititute of Science and Technology and [2]Seoul National Univ., Korea*

P2-15
Improvement on Turn-on Speed of Substrate-Triggered SCR Device by Using Dummy-Gate Structure for On-Chip ESD Protection
K.-C. Hsu[1] and M.-D. Ker[1], *[1]National Chiao-Tung Univ., Taiwan*

P2-16
A new Conductivity Modulated LDMOSFET employing Buried P Region and P+ Drain
J.-K. Oh[1], B.-C. Jeon[1], M.-K. Han[1] and Y.-I. Choi[2], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

P2-17
Trench IGBT for the Improved Short Circuit Capability by Employing the Curved Junction and Wide Cell Pitch
S.-S. Kim[1], M.-W. Ha[1], Y.-I. Choi[2] and M.-K. Han[1], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*

P3 Silicon Process / Materials Technologies
(19 Papers)

P3-1
Novel Storage-Node Contacts with Stacked PCM-Sp-TiN Barrier for MIM-Ru/Ta_2O_5/Ru Capacitors in Giga-Bit DRAMs
T. Kawagoe[1], Y. Nakamura[1], K. Kuroki[1], I. Asano[1], H. Goto[1] and N. Nakanishi[1], *[1]Elpida Memory, Inc., Japan*

P3-2
Very High Reliability of Ultrathin Silicon Nitride Gate Dielectric Film for sub-100nm Generation
M. Komura[1], M. Higuchi[1], W. Cheng[1], I. Ohshima[2], A. Teramoto[2], M. Hirayama[2], S. Sugawa[1] and T. Ohmi[2], *[1]Tohoku Univ. and [2]NICHe, Tohoku Univ., Japan*

P3-3
Excellent Contact-Hole Etching with NH_3 Added C_5F_8 Pulse-Modulated Plasma
M. Ooka[1] and S. Yokoyama[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-4
Electroless Copper Seed Activated by 1nm ICB-Pd Catalytic Layer for Fine Cu Interconnections
Z. Wang[1], O. Yaegashi[1], H. Sakaue[1], T. Takahagi[1] and S. Shingubara[1], *[1]Hiroshima Univ., Japan*

P3-5
Atomic Order Flattening of Hydrogen-Terminated Si(110) Substrate For Next Generation ULSI Devices
H. Akahori[1], K. Nii[1], A. Teramoto[1], S. Sugawa[2] and T. Ohmi[1], *[1]NICHe, Tohoku Univ. and [2]Tohoku Univ., Japan*

P3-6
An Integrated Gate Stack Process for Sub-90nm CMOS
S.J. Chang[1], S.Y. Wu[1], C.L. Chen[1], T.L. Lee[1], Y.M. Lin[1], Y.S. Tsai[1], H.D. Su[1], S.B. Chen[1], Y.S. Chen[1], M.S. Liang[1], Y.C. See[1] and Y.C. Sun[1], *[1]Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan*

P3-7
Precursors for chemical vapor deposition of NiSi
M. Ishikawa[1], T. Kada[1], H. Machida[1], Y. Ohshita[2] and A. Ogura[3], *[1]TRI Chemical Labs Inc., [2]Toyota Technological Inst. and [3]NEC Corp., Japan*

P3-8
MOCVD $HfAl_xO_y$ Gate Dielectrics Deposited Using Single Cocktail Liquid Source
M.S. Joo[1], B.J. Cho[1], C.C. Yeo[1], S.J. Whoang[2], S. Matthew[3], L.K. Bera[3], N. Balasubramanian[3] and D.-L. Kwong[4], *[1]SNDL, National Univ. of Singapore, [2]Jusung Engineering Co., Ltd., Korea, [3]Inst. of Microelectronics, Singapore and [4]The Univ. of Texas, Austin, Singapore*

P3-9
Tight-Binding Quantum Chemical Molecular Dynamics Simulation on Chemical Mechanical Polishing Process of Cu Surface
N. Isoda[1], K. Sasata[1], T. Yokosuka[1], A. Endou[1], M. Kubo[1], A. Imamura[2] and A. Miyamoto[1,3], *[1]Tohoku Univ., [2]Hiroshima Kokusai Gakuin Univ. and [3]NICHe, Tohoku Univ., Japan*

P3-10
A Novel Photosensitive Porous Low-k Interlayer Dielectric Film
S. Kuroki[1], T. Hirota[2] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ. and [2]TAZMO Co., Ltd., Japan*

P3-11
Increase of Crystallization Temperatures of Ultrathin Al_2O_3 Films Caused by Si Diffusion during Annealing
S. Migita[1], J.-W. Park[2], T. Yasuda[1], M. Nishizawa[1], R. Kuse[2], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-AIST, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*

P3-12
Neutral Beam Etching for Damage-free 50 nm Gate Electrode Patterning
S. Noda[1,2], H. Nishimori[2], T. Ida[3], T. Arikado[2], K. Ichiki[3] and S. Samukawa[1], *[1]Tohoku Univ. [2]Semiconductor Leading Edge Technologies, Inc., [3]Ebara Research Co., Ltd., Japan*

P3-13
Defect Generation in Gate Oxide by Selective Oxidation in Hydrogen-rich Wet Ambient
H.-J. Cho[1], K.-Y. Lim[1], S.-A. Jang[1], J.-H. Lee[1], J.-G. Oh[1], Y.-S. Kim[1], H.-S. Yang[1] and H.-C. Sohn[1], *[1]Hynix Semiconductor Inc., Korea*

P3-14
Improving Electrical Properties of CVD HfO_2 by Multi-Step Deposition and Annealing in a Gate Cluster Tool
C.C. Yeo[1], B.J. Cho[1], M.S. Joo[1], S.J. Whoang[2], D.-L. Kwong[3], L.K. Bera[4], S. Mathew[4] and N. Balasubramanian[4], *[1]National Univ. of Singapore, [2]Jusung Engineering Co., Ltd., [3]The Univ. of Texas at Austin and [4]Inst.s of Microelectronics, Singapore*

P3-15
Influence of Humidity on Electrical Characteristics of Porous Silica Films
S. Sakamoto[1], S. Kuroki[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-16
Chemical structure of N Atoms in the Transition Region of the SiO(N)/Si Interface -A New Spectroscopic Method with Hydrogenation Reaction in HF Acid-
N. Mizuta[1] and S. Watanabe[1], *[1]Fujitsu Labs Ltd, Japan*

P3-17
The sheet resistance instability in the sub-100 nm tungsten poly-metal wordline due to an *in-situ* NH_3 pre-annealing during the sealing nitride deposition
K.-Y. Lim[1], J.-H. Lee[1], H.-J. Cho[1], J.-G. Oh[1], B.-S. Hong[1], S.-A. Jang[1], Y.-S. Kim[1], H.-S. Yang[1] and H.-C. Sohn[1], *[1]Hynix Semiconductor Inc., Korea*

P3-18
Influence of interface layers and bottom electrode on $(Ba,Sr)TiO_3$ thin film leakage current
M. Yamato[1] and T. Kikkawa[1], *[1]RCNS, Hiroshima Univ., Japan*

P3-19
Interface Oxidation Mechanism in HfO_2/Silicon System with Post-Deposition Annealing
H. Shimizu[1], M. Sasagawa[1], K. Kita[1], K. Kyuno[1] and A. Toriumi[1], *[1]The Univ. of Tokyo, Japan*

P4
New Materials and Characterization
(18 Papers)

P4-1
Improving the Accuracy of Modified Shift-and-Ratio Channel Length Extraction Method Using Scanning Capacitance Microscopy
C.W. Eng[1,2], W.S. Lau[1], Y.Y. Jiang[3], D. Vigar[2], K.C. Tee[2], L. Chan[2], S.W.V. Lim[3] and A. Trigg[3], *[1]Nanyang Technological Univ. of Singapore, [2]Chartered Semiconductor Manufacturing Ltd and [3]Inst. of Microelectronics, Singapore*

P4-2
Influence of nitrogen profile on metal workfunction in Mo/SiO_2/Si MOS structure
M. Hino[1], T. Amada[1], N. Maeda[1] and K. Shibahara[1], *[1]RCNS, Hiroshima Univ., Japan*

P4-3
Compact Electrical Characterization of Nano-CMOS Transistor with 1.2nm Ultrathin Gate Dielectric
H.S. Kang[1], W.-Y. Quan[2], K.S. Kim[1], C.B. Oh[1], H.J. Ryu[1], C.K. Baek[2], B. Kim[2], Y.W. Kim[1], K.P. Suh[1], and D.M. Kim[2], *[1]Samsung Electronics, [2]Korea Inst. for Advanced Study, Korea*

P4-4
Cross-Hatch Related Oxidation and Reliability of Gate Oxide of Strained-Si/SiGe
M. Nishisaka[1] and T. Asano[1], *[1]Kyushu Inst. of Technology, Japan*

P4-5
Visible Light Irradiation Effects on Atomic-Scale Observations of Hydrogenated Amorphous Silicon Films by Scanning Tunneling Microscopy
K. Arima[1], H. Kakiuchi[1], M. Ikeda[1], K. Endo[2], M. Morita[1] and Y. Mori[2], *[1]Osaka Univ. and [2]Research Center for Ultra-Precision Science and Technology, Osaka Univ., Japan*

P4-6
Influence of structural variation of Ni silicide thin films on electrical property for contact materials
K. Okubo[1], Y. Tsuchiya[1], O. Nakatsuka[1], A. Sakai[1], S. Zaima[1] and Y. Yasuda[1], *[1]Nagoya Univ., Japan*

P4-7
Ultra-shallow Boron Profile Fitting Compensating for Surface Contamination by Utilizing Genetic Algorithms
M. Murakawa[1], K. Shibahara[2], Y. Oda[3], T. Higuchi[1] and K. Nishi[3], *[1]AIST, [2]Hiroshima Univ. and [3]SELETE, Japan*

P4-8
Nucleation-Control in Solid-Phase-Crystallization of a-Si/SiO_2 by Local Ge Insertion
I. Tsunoda[1], K. Nagatomo[1], A. Kenjo[1], T. Sadoh[1], S. Yamaguchi[2] and M. Miyao[1], *[1]Kyushu Univ. and [2]Hitachi, Japan*

P4-9
Atomic-scale Adsorbent Structure of Contaminant Metal on Si(100) Surface and its Effect on Thermal Oxidation
T. Onizawa[1,2], T. Narushima[1,3,4], K. Miki[1,3] and K. Yamabe[2], *[1]NRI, AIST, [2]Univ. of Tsukuba, [3]NML, NIMS and [4]SFI Trinity Nanoscience Lab, Trinity College Dublin, Japan*

P4-10
Effect of Vacuum Annealing on High-k Dy_2O_3 Thin Films Deposited on Si(100)
S. Ohmi[1], H. Yamamoto[1], J. Taguchi[1], K. Tsutsui[1] and H. Iwai[1], *[1]Tokyo Inst. of Technology, Japan*

P4-11
Formation of Strained β-$FeSi_2$(Ge) by Ge-Segregation Controlled Solid-Phase Growth of $[\text{Amorphous Si/FeSiGe}]_n$ Multi-Layered Structure
T. Sadoh[1], M. Owatari[1], A. Kenjo[1], T. Yoshitake[1], M. Itakura[1] and M. Miyao[1], *[1]Kyushu Univ., Japan*

P4-12
Electrical properties of crystalline γ-Al_2O_3 films using conductive-AFM and MISFETs with Aluminum gates
T. Okada[1], R. Ito[1], M. Shahjahan[1], K. Sawada[1] and M. Ishida[1], *[1]Toyohashi Univ. of Technology, Japan*

P4-13
Wet Etching Characteristics of both As-deposited and Annealed Al_2O_3 and $HfAlO_x$ Films
T. Nishimura[1], R. Kuse[2], K. Tominaga[2], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI project, ASRC, AIST, [2]MIRAI ASET and [3]The Univ. of Tokyo, Japan*

P4-14
Impact of Ti/TiN (Glue/Barrier Layer) Formation on Ultra-thin Gate Oxide Reliability (HCI and NBTI) for Deep Sub-micron CMOS Transistors
C. Liu[1], M.G. Chen[1], Y.R. Yang[1] and Y.T. Loh[1], *[1]UMC, Taiwan*

P4-15
Characterization and Comparison of Strained $Si_{1-y}C_y$ MOSFET Grown by Gas Source MBE and Hot Wire Cell Method
T. Watahiki[1], K. Abe[2], A. Yamada[2] and M. Konagai[1], *[1]Tokyo Inst. of Technology, [2]Shinshu Univ., Japan*

P4-16
Effect of Nitrogen Annealing on the Electrical Properties of Ultrathin Crystalline γ-Al_2O_3 High-κ Dielectric Films Deposited on Si(111) Substrates
M. Shahjahan[1], T. Okada[1], K. Sawada[1] and M. Ishida[1], *[1]Toyohashi Univ. of Technology, Japan*

P4-17
Electrical properties and conduction mechanism of ZrO_2 films on $Si_{1-y}C_y$
G.K. Dalapati[1], S.K. Samanta[2], S. Chatterjee[3], P.K. Bose[4], S. Varma[5], S. Patil[6] and C.K. Maiti[7], *[1]IIT Kharagpur, [2]Jadavpur Univ., [3]Inst. of Physics, Bhubaneswar, India*

P4-18
Failure Mechanism of Nano-crystalline VN barrier in Cu/VN/SiO_2/Si system
T. Itoi[2], O. Yanada[3], K. Satoh[4], B.M. Takeyama[1] and A. Noya[1], *[1]Kitami Inst. of Technology, [2]Chiba Univ., [3]SEC Ltd. and [4]Hitachi Kokusai Electric Inc., Japan*

P5
Compound Semiconductor Materials and Devices
(12 Papers)

P5-1
Metal-Semiconductor-Metal UV Photodetector Based on AlGaN/GaN Heterostructure
H. Jiang[1], T. Egawa[1], H. Ishikawa[1], Y. Dou[1], C. Shao[1] and T. Jimbo[1], *[1]Nagoya Inst. of Technology, Japan*

P5-2
Low Frequency Noise Caused by Substrate Current in AlGaAs/InGaAs HEMTs
M. Wada[1], S. Nishiyama[1], T. Nakamoto[1] and K. Higuchi[1], *[1]Hiroshima Univ., Japan*

P5-3
Electro Static Discharge effects on AlGaN/GaN HEMTs on sapphire substrates
S.-C. Lee[1], J.-C. Her[1], K.-S. Seo[1] and M.-K. Han[1], *[1]Seoul National Univ., Korea*

P5-4
Study of InGaP/InGaAs Double Doped Channel Heterostructure Field-effect Transistor (DDCHFET)
H.-M. Chuang[1], C.-Y. Chen[1], P.-H. Lai[1], S.-I. Fu[1], Y.-Y. Tsai[1], C.-I. Kao[1] and W.-C. Liu[1], *[1]Inst. of Microelectronics, National Cheng-Kung Univ., Taiwan*

P5-5
Nitride-based blue LEDs with GaN/SiN double buffer layers
C.-H. Kuo[1], S.-J. Chang[1], Y.-K. Su[1], C.-K. Wang[1], L.-W. Wu[1], J.-K. Sheu[2] and J.-M. Tsai[3], *[1]National Cheng Kung Univ., [2]National Central Univ. and [3]South Epitaxy Corporation, Taiwan*

P5-6
Thermal Annealing Effect in GaInNAs Thin Films Estimated by X-ray Absorption Fine Structure Spectroscopy
K. Uno[1], M. Yamada[1], T. Takizawa[2] and I. Tanaka[1], *[1]Fac. Systems Eng., Wakayama Univ. and [2]Matsushita Elec. Co., Ltd., Japan*

P5-7
A Double-Barrier-Emitter Triangular Barrier Optoelectronic Switch
J.-Y. Chen[1], D.-F. Guo[2], K.-M. Lee[1], H.-M. Chuang[1], C.-Y. Chen[1] and W.-C. Liu[1], *[1]National Cheng-Kung Univ. and [2]Chinese Air Force Academy, Taiwan*

P5-8
GaAs-MISFETs with nm-Thin Gate Insulating Films Formed by Oxi-Nitridation Process
M. Takebe[1], N.C. Paul[1], K. Nakamura[1], K. Iiyama[1] and S. Takamiya[1], *[1]Kanazawa Univ., Japan*

P5-9
Characterization of Threading Dislocation in Si-doped GaN Films by High Spatial Resolution Cathodoluminescence Spectroscopy
R. Sugie[1], M. Yoshikawa[1] and H. Harima[2], *[1]Toray Research Center Inc. and [2]Kyoto Inst. of Technology, Japan*

P5-10
Characterization of AlInAsSb/GaInAsSb Multiple Quantum Wells Grown by MOVPE
Y.-K. Su[1], C.-H. Wu[1] and J.-R. Chang[2], *[1]Inst. of Microelectronics, National Cheng Kung Univ., [2]Epistar Corporation, Taiwan*

P5-11
Growth Temperature Dependence of Nitrogen Incorporation in GaNAs Grown by Chemical Beam Epitaxy
Y. Sun[1], M. Yamamori[1], T. Egawa[1] and H. Ishikawa[1], *[1]Nagoya Inst. of Technology, Japan*

P5-12
Al-doped ZnO Intermediate Layer for AlGaN/GaN HEMT Ohmic Contact
K. Nishizono[1], M. Okada[1], M. Kamei[1], D. Kikuta[1], J.-P. Ao[1], K. Tominaga[1] and Y. Ohno[1], *[1]The Univ. of Tokushima, Japan*

P6
Optoelectronic Devices and Photonic Crystal Devices
(14 Papers)

P6-1
Investigation of Nonreciprocal Phase Shift Characteristics for Integrated Optical Waveguide Isolators Utilizing Magnetic Photonic Crystals
J.S. Yang[1], G. Lee[1], T.H. Lee[1], Y.-I. Kim[1], M.-C. Park[1], Y.T. Byun[1], D.H. Woo[1], S. Lee[1], S.H. Song[2] and S.H. Kim[1], *[1]Korea Inst. of Science and Technology and [2]Hanyang Univ., Korea*

P6-2
Magnetooptic Spatial Light Modulator with One-Step Pattern Growth on Ion-Milled Substrates by Liquid-Phase Epitaxy
J.-H. Park[1,3], J.-K. Cho[2], K. Nishimura[1], H. Uchida[1] and M. Inoue[1,4], *[1]Toyohashi Univ. of Technology, Japan, [2]Gyeongsang National Univ., Korea, [3]ASTF and [4]CREST-JST, Japan*

P6-3
Optical Properties of Acrylate-Based Negative-Type Photoresist and Fabrication of Optical Waveguides
P. Gutafik[1], O. Sugihara[2] and N. Okamoto[1], *[1]Shizuoka Univ. and [2]Tohoku Univ., Japan*

P6-4
Optical Tuning of Defect-Induced Pass-Band in Photonic Crystal Waveguide
M. Tsuji[1], Y. Iida[1] and Y. Omura[1], *[1]Kansai Univ., Japan*

P6-5
Numerical Analysis of Waveguides in Three-Dimensional Photonic Crystal with Finite Thickness
Y. Watanabe[1], N. Yamamoto[1,2] and K. Komori[1], *[1]AIST and [2]CREST, JST, Japan*

P6-6
Fabrication of Wide Area Two-Dimensional Photonic Crystal Using Holographic Lithography
J.I. Moon[1], S.H. Kim[1], S.H. Park[1] and Y.T. Lee[1], *[1]Kwangju Inst. of Science Technology, Korea*

P6-7
A Study of Magnetostriction and Its Application to Silicon-on-Insulator Waveguides
P.S. Chan[1] and H.K. Tsang[1], *[1]The Chinese Univ. of Hong Kong., China*

P6-8
Blue Luminescence of Porous Alumina Membranes Prepared by Anodic Oxidation
T. Echizenya[1], K. Takase[1], Y. Takahashi[1], Y.Takano[1] and K. Sekizawa[1], *[1]Nihon Univ., Japan*

P6-9
AlGaAs/InGaAs DFB Laser by One Time Selective MOCVD Growth on a Grating Substrate
Y. Takasuka[1,2], K. Yonei[2], H. Yamauchi[1] and M. Ogura[1], *[1]AIST and [2]Shibaura Inst. of Technology, Japan*

P6-10
InGaN/GaN Light Emitting Diodes with a Lateral Current Blocking Structure
W.-B. Chen[1], Y.-K. Su[1], C.-L. Lin[1], H.-C. Wang[1] and S.-M. Chen[2], *[1]National Cheng Kung Univ., and [2]Epitech Technology Corporation, Taiwan*

P6-11
Characteristics of P-I-i-I-N GaAs/$Al_{0.35}Ga_{0.65}As$ Phase Modulator and MultiMode Interference Used in the TE/TM Mode Splitter
S.-P. Kim[1,2], J.-M. Son[1,2], S.-S. Lee[1], S. Lee[2], D.-H. Woo[2] and S.-H. Kim[2], *[1]Hanyang Univ. and [2]Korea Inst. of Science and Technology, Korea*

P6-12
Surface Plasmon Resonance and Emission Light Properties of Polystyrene Sphere Thin Films
K. Shinbo[1], S. Miyabayashi[1], K. Yoshizawa[1], H. Shirasawa[1], K. Kato[1] and F. Kaneko[1], *[1]Niigata Univ., Japan*

P6-13
Enhanced Frequency Response Associated with Negative Photoconductance in an InGaAs/InAlAs Avalanche Photodetector
G. Kim[1], I.G. Kim[1], J.H. Baek[1] and O.K. Kwon[1], *[1]Electronics & Telecommunication Research Inst., Korea*

P6-14
The Characteristic of InGaN/GaN Multiple-Quantum-Well Metal-Insulater-Semiconductor Photodiodes Using SiO_2 Fabricated by Photochemical Vapor Deposition
P.C. Chang[1], C.H. Chen[2], S.J. Chang[1], Y.K. Su[1], P.C. Chen[1], Y.D. Jhou[1], H. Hung[1], S.L. Wu[2], and K.C. Huang[2], *[1]National Cheng Kung Univ. and [2]Cheng Shiu Inst. of Technology, Taiwan*

P7
Novel Devices, Physics, and Fabrication
(8 Papers)

P7-1
Novel comb-type differential pressure sensor with silicon beams embedded in a silicone rubber membrane
C.T. Seo[1] and J.H. Lee[1],
[1]Kyungpook National Univ., Korea

P7-2
Periodic Coulomb oscillation in highly doped Si single-electron transistor
T. Kitade[1], K. Ohkura[1] and A. Nakajima[1], *[1]RCNS, Hiroshima Univ., Japan*

P7-3
Active Pixel Sensor Using an SOI MOSFET Photodetector with a Quantum Wire
J.-H. Park[1], S.-H. Seo[1], I.-S. Wang[1], J.-H. Kim[1], J.-K. Shin[1], P. Choi[1], Y.-C. Jo[2] and H. Kim[2], *[1]Kyungpook National Univ. and [2]Korea Electronics Technology Inst., Korea*

P7-4
Side Gating Phenomenon in GaAs Quantum Wire Transistors
R. Jia[1], S. Kasai[1] and H. Hasegawa[1], *[1]RCIQE, Hokkaido Univ., Japan*

P7-5
Observation of current modulation in SAM-FET fabricated by an air-bridge structure
K. Sasao[1], Y. Azuma[1], N. Kaneda[1], E. Hase[1], Y. Miyamoto[1] and Y. Majima[1], *[1]Tokyo Inst. of Technology, Japan*

P7-6
Generation of Local Magnetic Field by Nano Electro-Magnets
H.K. Kim[1,2], S.H. Hong[1], B.C. Kim[1], J.S. Hwang[2], S.W. Hwang[1,2] and D. Ahn[2], *[1]Korea Univ. and [2]Univ. of Seoul, Korea*

P7-7
Atomic-scale Smoothing and Structural Analysis of $LiNbO_3$ Surface
A. Saito[1,2], H. Matsumoto[1], S. Ohnisi[1], M. Akai-Kasaya[1], Y. Kuwahara[1,2] and M. Aono[1,3], *[1]Osaka Univ., [2]RIKEN and [3]National Inst. for Materials Science, Japan*

P7-8
Electron Transport in Molecular Enamel Wires
Rodion Belosludov[1], Amir Farajian[1], Hiroshi Mizuseki[1], Kyoko Ichinoseki[1] and Yoshiyuki Kawazoe[1], *[1]Tohoku University, Japan*

P8
Quantum Nanostructure Devices and Physics
(10 Papers)

P8-1
Spin depolarization via tunneling effects in asymmetric double quantum dot structure
H. Sasakura[1], S. Adachi[1], S. Muto[1], H. Song[2], T. Miyazawa[2] and T. Usuki[2], *[1]Hokkaido Univ. and CREST, JST and [2]Fujitsu Labs Ltd., Japan*

P8-2
Mechanical Properties of Nanometer-sized Cu Contacts
T. Kizuka[1], M. Mori[1], S. Fujisawa[2] and A. Yabe[2], *[1]Univ. of Tsukuba, [2]AIST, Japan*

P8-3
A Study on Doping Density in InAs/GaAs Quantum Dot Infrared Photodetector
U.H. Lee[1], Y.H. Kang[1], J.H. Oum[1], S.-J. Lee[2], M. Kim[2], S.K. Noh[2], Y.D. Jang[3], D. Lee[3] and S. Hong[1], *[1]Korea Advanced Inst. of Science and Technology, [2]Korea Research Inst. of Standards and Science and [3]Chungnam National Univ., Korea*

P8-4
Enhanced Optical Properties of High Density $(>10^{11}/cm^2)$ InAs/AlAs Quantum Dots by Using Hydrogen Passivation
S.-K. Park[1], J. Tatebayashi[1], Y.J. Park[2] and Y. Arakawa[1], *[1]RCAST and IIS, Univ. of Tokyo, Japan and [2]Korea Inst. of Science and Technology, Korea*

P8-5
Controlling the optical properties of self-assembled InAs quantum dots by various annealing treatments
J.-J. Yoon[1], S.-I. Jung[1], H. Choi[1], J.W. Lee[1], G.S. Cho[1], M.H. Jeon[1], J.-Y. Leem[1], D.Y. Lee[2], J.S. Kim[3], J.S. Son[4], S.I. Ban[1], J.I. Lee[5] and J.S. Kim[6], *[1]InJe Univ., [2]Yeungnam Univ., [3]Nanomaterials Lab., [4]Kyungwoon Univ., [5]Materials Evaluation Center and [6]Basic Res. Lab., ETRI, Korea*

P8-6
Control of GaSb/GaAs Quantum Nanostructures by Molecular Beam Epitaxy
T. Nakai[1], S. Iwasaki[1] and K. Yamaguchi[1], *[1]The Univ. of Electro-Communications, Japan*

P8-7
Formation of Ge Quantum dots by Selective Oxidation of SiGe alloys for Single-Electron Devices
P.-W. Li[1], W.-M. Liao[1], S.W. Lin[1], P.S. Chen[1] and M.J. Tsai[1], *[1]National Central Univ. Taiwan*

P8-8
Investigation of Ultrafast Carrier Dynamics in Quantum Wire by Terahertz Spectroscopy
I. Morohashi[1,2], K. Komori[1,2], T. Hidaka[3], G.-R. Wang[1], M. Ogura[1] and M. Watanabe[1], *[1]National Inst. of Advanced Industrial Science and Technology, [2]CREST, JST and [3]Shonan Inst. of Technology, Japan*

P8-9
Influence of deep-level concentrations on strong red photoluminescence from nano-porous silicon formed on Fe-contaminated silicon substrate
D.-Y. Lee[1], J.-W. Park[1], S.-S. Choi[1], D.-H. Kim[1], I.-H. Bae[1], J.-Y. Leem[2], J.-S. Kim[3], S.-K. Kang[4], J.-S. Son[5] and I.-S. Kim[5], *[1]Yeungnam Univ., [2]Inje Univ., [3]National Inst. for Materials Science, [4]Kyunghee Univ. and [5]Kyungwoon Univ., Korea*

P8-10
Identification of valence-band ordering in ZnO by using four-wave mixing
S. Adachi[1], S. Muto[1], K. Hazu[2], T. Sota[2], K. Suzuki[2] and S. Chichibu[3], *[1]Hokkaido Univ., [2]Waseda Univ. and [3]Univ. of Tsukuba, Japan*

P9
Silicon-on-Insulator Technologies
(8 Papers)

P9-1
SOI SRAM / DRAM Cells for 0.5 Volt Operation
M. Terauchi[1], *[1]Hiroshima City Univ., Japan*

P9-2
Complete Surface-Potential-Based SOI-MOSFET Model for Circuit Simulation
D. Kitamaru[1], Y. Uetsuji[1] and M. Miura-Mattausch[1], *[1]Hiroshima Univ., Japan*

P9-3
Complementary Operation of Schottky Source/Drain SOI MOSFET with Shallow Doped Extension
S. Matsumoto[1], M. Nishisaka[1] and T. Asano[1], *[1]Kyushu Inst. of Technology, Japan*

P9-4
A Workable Use of Floating-Body SOS MOSFET as a Transconductance Mixer
S. Lam[1], A.C.-K. Chan[1], W.-K. Lee[1], P.K.T. Mok[1], P.K. Ko[1] and M. Chan[1], *[1]Hong Kong Univ. of Science & Technology, Hong Kong*

P9-5
Thereshold Voltage Control on the Body-Tied FinFET (OMEGA MOSFET)
H.J. Jo[1], T.-S. Park[2], J.D. Choe[1], S.Y. Han[1], J.H. Jeong[1], M.C. Chae[1], D.G. Park[1], K. Kim[1], E. Yoon[2] and J.-H. Lee[3], *[1]Samsung Electronics Co., Ltd, [2]Seoul National Univ. and [3]Kyungpook National Univ., Korea*

P9-6
High Performance Buried Gate Surrounding Gate Transistor (BG-SGT) for Future Three-Dimensional Devices
M. Iwai[1], Y. Yamamoto[1], R. Nishi[1], H. Sakuraba[1], T. Endoh[1] and F. Masuoka[1], *[1]RIEC, Tohoku Univ., Japan*

P9-7
Thermal conductivity of high-integrity nanometer buried oxides by SIMOX
Y. Dong[1], X. Wang[1], J. Chen[1], M. Chen[1,2], X. Wang[1,2], P. He[3], L. Tian[3] and Z. Li[3], *[1]Shanghai Inst. of Microsystem and Information Technology, Chinese Academy of Sciences, [2]Shanghai Simgui Technology Co., Ltd. and [3]Inst. of Microelectronics, Tsinghua Univ., China*

P9-8
Low frequency noise in partially-depleted SOI MOSFETs operating from linear region to saturation region at various temperatures
K.-M. Chen[1], H.-H. Hu[2], G.-W. Huang[1], S.-Y. Huang[2], A.S. Peng[1], W.-K. Yeh[3] and C.-Y. Chang[2], *[1]Natioanl Nano Device Labs, [2]Natioanl Chiao Tung Univ. and [3]National Univ. of Kaohsiung, Taiwan*

P10
Non-Volatile Memory Technologies
(9 Papers)

P10-1
Improvement of Data Retention in Floating Gate Flash EEPROM's with P-Doped Floating Gate
B.C. Wu[1], H.W. Tsai[1], S.S. Chung[1], C.J. Lin[2], D.S. Kuo[3], and M.S. Liang[2], *[1]National Chiao Tung Univ., [2]Tsmc, Science-based Industrial Park, Hsinchu, Taiwan and [3]Nexflash Inc., San Jose, USA*

P10-2
New Three Dimensional High Density S-SGT Flash Memory Architecture using Self-Aligned Interconnection Fabricating Technology without Photo Lithography Process for Tera Bits and Beyond
H. Sakuraba[1], K. Kinoshita[2], T. Tanigami[2], T. Yokoyama[1], S. Horii[1], M. Saitoh[2], K. Sakiyama[2], T. Endoh[1] and F. Masuoka[1], *[1]RIEC, Tohoku Univ. and [2]Sharp Corporation, Japan*

P10-3
The Impact of Technology Parameters and Scaling on the Programming Performance and Drain Disturb in CHISEL Flash EEPROMs
D. Nair[1], N. Mohapatra[1], S. Mahapatra[1] and S. Shukuri[2], *[1]Indian Inst. of Technology, India and [2]Hitachi Ltd., Japan*

P10-4
Key technologies of First 'Chain' -32M bit Ferroelectric RAM
T. Ozaki[1], N. Nagel[2], Y. Kumura[1], J. Lian[2], A. Hilliger[2], T. Tsuchiya[1], R. Bruchhaus, H. Kanaya[1], H. Koyama, U. Wellhausen, O. Hidaka, S. Shuto, S. Germhardt, Y. Shimojo, B.K. Moon, H. Itokawa, U. Egger, H. Zhuang, K. Tomioka, M. Fukushima, K. Yamakawa, D. Takashima, I. Kunishima[1], Y. Oowaki[1] and G. Beitel[2], *[1]Smiconductor Company, Toshiba Corporation and [2]Infineon Technologies Japan K.K., Japan*

P10-5
High performance Pt/$SrBi_2Ta_2O_9$/Hfo_2/Si structure for 1T ferroelectric random access memory
D.-Y. Wang[1], C.-H. Chien[2], M.-J. Yang[2], P. Lehnen[3], C.-C. Leu[2], S.-H. Chuang[2], T.-Y. Huang[1] and C.Y. Chang[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs and [3]AIXTRON AG, Germany*

P10-6
Improvement in Read Endurance of Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode
D.K. Tran[1] and S. Horita[1], *[1]JAIST, Japan*

P10-7
A Novel Sensing Circuit for High Speed Synchronous MRAM
H. Kim[1], S. Lee[1], S. Lee[1], H. Shin[1] and D. Kim[2], *[1]Ewha Womans Univ. and [2]Kookmin Univ., Korea*

P10-8
Electrical Characterization Sub-micron MTJ Cells Using SPM
S. Park[1], J. Heo[1], I. Chung[1] and T. Kim[2], *[1]SungKyunKwan Univ. and [2]Samsung Advanced Inst. of Technology, Korea*

P10-9
Highly Anisotropic and Corrosion-less PtMn Etching using Negative Ions in Pulse-Time-Modulated Chlorine Plasma
S. Kumagai[1], T. Shiraiwa[2] and S. Samukawa[1], *[1]Tohoku University and [2]Micro Systems Network Company, Sony Corporation, Japan*

P11
SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
(4 Papers)

P11-1
Balanced-type Peak Power Injection Amplifierfor Simultaneous High Efficiency and Large Saturation Power
K. Iyomasa[1], M. Nakayama[1], K. Horiguchi[1], Y. Ikeda[1] and Y. Sakai[1], *[1]Mitsubishi Electric Corporation, Japan*

P11-2
Indium Content Dependence of Electron Velocity and Impact Ionization in InAlAs/InGaAs Metamorphic HEMTs
H. Ono[1], S. Taniguchi[1] and T. Suzuki[2], *[1]Sony Corporation and [2]AIST, Japan*

P11-3
Two-Step Electrode Self-Aligned Process of InP-based RTDs for Highly Integrated RTD/HEMT Circuits
T. Ohki[1], N. Okamoto[1], T. Takahashi[1], K. Makiyama[1], K. Imanishi[1] and N. Hara[1], *[1]Fujitsu Labs Ltd., Japan*

P11-4
The fabrication of enhancement-mode metamorphic InAlAs/InGaAs HEMT by Pt Schottky metal diffusion
C.-K. Lin[1], J.-C. Wu[1], W.-K. Wang[1], H.-C. Chiu[1] and Y.-J. Chan[1], [1]*National Central Univ., Taiwan*

P12 System-Level Integration and Packaging Technologies (3 Papers)

P12-1
Effect of High Resistivity Si Substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects
S. Watanabe[1], A.B.M. Harun-ur Rashid[1] and T. Kikkawa[1], [1]*RCNS, Hiroshima Univ., Japan*

P12-2
Stacked π–type Equivalent Circuit Analysis of Ferromagnetic RF Integrated Inductor
M. Yamaguchi[1], S. Ikeda[1], S. Bae[1], S. Tanabe[2], K. Sugawara[2] and A. Konrad[3], [1]*Tohoku Univ.,* [2]*Mitsubishi Electric Co., Japan and* [3]*Univ. of Toronto, Canada*

P12-3
A Study of ESD Protection under Pad Design for Copper-Low K VLSI Circuits
J.-W. Lee[1], A. Chao[3], Y. Li[1,2] and H. Tang[3], [1]*National Nano Device Labs,* [2]*National Chiao Tung Univ. and* [3]*United Microelectronics Corporation, Taiwan*

P13 Organic Semiconductor Devices and Materials (6 Papers)

P13-1
Characterization of hydrogen treated Pentacene OTFT
S.-C. Suen [1], W.-T. Whang[2] and J.-Y. Yang[1], [1]*National Nano Device Labs and* [2]*Inst. of Materials Science and Engineering, National Chiao-Tung Univ., Taiwan*

P13-2
Thickness Dependent Device Operation of Sublimed Molecular Field-Effect Transistors
S. Hoshino[1], M. Yoshida[1], S. Uemura[1], T. Kodzasa[1], T. Kamata[1] and K. Yase[1], [1]*AIST, Japan*

P13-3
A Study on Morphology and Electrical Properties of Dendrimer Complex with Pt Ions
K.-H. Jung[1], H.-K. Shin [1], C. Kim[1] and Y.-S. Kwon[1], [1]*Dong-A Univ., Korea*

P13-4
High Resolution Periodical Structure Fabricated by Laser Machining in Photosensitive Polymers
S. Shibata[1], O. Sugihara[2], N. Okamoto[3] and T. Kaino[2], [1]*Shizuoka Univ.,* [2]*Tohoku Univ. and* [3]*Shizuoka Univ., NEDO, Japan*

P13-5
Fabrication of a Photoelectrochemical Cell Using a Self-Assembled Monolayer of Tris(2.2'-bipyridine)ruthenium(II)-Viologen Linked Thiol on Multistructured Gold Nanoparticles
N. Terasaki[1], K. Otsuka[2], T. Akiyama[2] and S. Yamada[2], [1]*AIST and* [2]*Kyushu Univ., Japan*

P13-6
Electrochemical Studies on a Self-Assembled Viologen Monolayer using Quartz Crystal Microbalance
J.-Y. Ock[1], H.-K. Shin[1], D.-J. Qian[2], J. Miyake[2] and Y.-S. Kwon[1], [1]*Dong-A Univ., Korea and* [2]*Tissue Engineering Research Center, AIST, Japan*

P14 Micro-Nano Electromechanical Devices for Bio- and Chemical Applications (4 Papers)

P14-1
Incident Angle Effect on Deep MEMS Structure in Resist Spray Coating Technique
V.K. Singh[1], M. Sasaki[1] and K. Hane[1], [1]*Tohoku Univ., Japan*

P14-2
A High Resolution Hemoglobin Measurement Cell Integrated with Signal Processing Circuit
T. Noda[1], T. Hidekuni[1], M. Ashiki[1], H. Ebi[2], K. Sawada[1] and M. Ishida[1], [1]*Toyohashi Univ. of Technology and* [2]*HORIBA Ltd., Japan*

P14-3
Vertically Buckled Bridges for Three-Dimensional SOI-MEMS
M. Sasaki[1], D. Briand[2], W. Noell[2] and N. de Rooij[2], [1]*Tohoku Univ. and* [2]*Univ. of Neuchatel, Japan*

P14-4
An Investigation on The Mechanism of EHD Phenomena in High Intensity and Asymmetric Electric Field
S. Suzuki[1], T. Nakasone[1] and K. Ishikawa[1], [1]*SEIKEI Univ., Japan*

Thursday, September 18

Room A

A-7: Advanced Silicon Devices and Device Physics
-High-k Technology II-
(9:00-10:30)
Chairs: K. Shibahara (Hiroshima Univ.)
M. Ogawa (Kobe Univ.)

9:00 A-7-1 (Invited)
High-k/Oxynitride Gate Dilectric-Searching for Serendipitous Materials-
M. Hiratani[1], S. Saito[1], Y. Shimamoto[1], S. Tsujikawa[1], Y. Matsui[1], O. Tonomura[1], K. Torii[1], J. Yugami[1], and S. Kimura[1], *[1]Hitachi, Ltd., Japan*

9:30 A-7-2
Effect of Coulomb Scattering on Stress-Induced Mobility Degradation in nMOSFETs with $HfAlO_x/SiO_2$ Dielectrics
W. Mizubayashi[1], N. Yasuda[2], H. Hisamatsu[2], H. Ota[1], K. Tominaga[2], K. Iwamoto[2], K. Yamamoto[2], T. Horikawa[1], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]The Univ. of Tokyo, Japan*

9:50 A-7-3
Influence of Dielectric Constant Distribution in Stacked Gate Dielectrics on Electron Mobility in Inversion Layers
M. Ono[1], T. Ishihara[1] and A. Nishiyama[1], *[1]Toshiba Corporation, Japan*

Room B

B-7: Silicon Process / Materials Technologies
-Metal Gate, Gate Oxide-
(9:00-10:20)
Chairs: T. Arikado (Selete)
K. Suguro (Toshiba)

9:00 B-7-1
Low Tinv (≤1.8 nm) Metal-Gated MOSFETs on SiO_2 Based Gate Dielectrics for High Performance Logic Applications
V. Ku[1], R. Amos[1], A. Steegen[1], C. Cabral, Jr.[1], V. Narayanan[1], P. Jamison[1], P. Nguyen[1], Y. Li[1], M. Gribelyuk[1], Y. Wang[1], J. Cai[1], A. Callegari[1], F. McFeely[1], F. Jamin[1], K. Wong[1], E, Wu[1], A. Chou[1], D. Boyd[1], H. Ng[1], M. Ieong[1], C. Wann[1], R. Jammy[1] and W. Haensch[1], V. Ku[1], R. Amos[1], C. Cabral, Jr[1], V. Narayanan[1], P. Jamison[1], P. Nguyen[1], Y. Li[1], M. Gribelyk[1], Y. Wang[1], J. Cai[1], A.Callegari[1], F. McFeely[1], F. Jamin[1], K. Wong[1], E. Wu[1], A. Chou[1], D. Boyd[1], H. Ng[1], M. Ieong[1], C. Wann[1], R. Jammy[1], and W. Haensch[1], *[1]IBM, USA*

9:20 B-7-2
New Dual Metal Gate by Using WSix for nMOS and Pt-alloyed WSix for pMOS
K. Matsuo[1], O. Arisumi[1] and S. Kyoichi[1], *[1]Toshiba Corporation, Japan*

9:40 B-7-3
Highly Selective Etching of Ta/TaNx Metal Electrode to Si_3N_4 Gate Dielectric Employing $SiCl_4$-NF_3 Gas Mixture Plasma
H. Shimada[1] and K. Maruyama[1], *[1]SEIKO EPSON Corp., Japan*

Room C

C-7: Organic Semiconductor Devices and Materials
-Organic Thin Film Transistor-
(9:15-10:30)
Chais: T. Kamata (AIST)
S. Shiratori (Keio Univ.)

9:15 C-7-1 (Invited)
Towards Printed Organic Electronics: Semiconductor Materials Design for Plastic Transistors
B.S. Ong[1], *[1]Xerox Research Centre of Canada, Canada*

9:45 C-7-2
Self-Alignment Organic Field-Effect Transistor using Back-Side Exposure Method
T. Hyodo[1], F. Morita[1], S. Naka[1], H. Okada[1] and H. Onnagawa[1] *[1]Toyama Univ., Japan*

10:00 C-7-3
A Water-Soluble Photolithography Process and the Application to OTFT Fabrication
C.K. Song[1] and K.H. Kim[1], *[1]DONG-A University, Korea*

Room D

D-7: New Materials and Characterization
-Carbon Nanotube Devices and Materials-
(9:20-10:30)
Chairs: Y. Awano (Fujitsu Labs.)
Y. Ochiai (NEC)

9:20 D-7-1
Characteristics of a Carbon Nanotube FET Analyzed as a Ballistic Nanowire FET
Y. Kimura[1], T. Shimizu[1] and K. Natori[1,2], *[1]Univ. of Tsukuba and [2]CREST-JST, Japan*

9:40 D-7-2 (Invited)
Performance Estimation and Benchmarking for Carbon Nanotube FETs and Nanodiode Arrays
H.-S.P. Wong[1], G.S. Ditlow[1], P.M. Solomon[1], X. Wang[2], *[1]IBM Research, T.J. Watson Research Center, [2]IBM Microelectronics, SRDC*

10:10 D-7-3
Ultra-low Energy Nitrogen-ion Irradiation for Improvement of Carbon Nanotube Channel Single Electron Transistor
T. Kamimura[1,4], K. Yamamoto[2] and K. Matsumoto[3,4], *[1]Univ. of Tsukuba, [2]AIST, [3]Osaka Univ. and [4]CREST/JST, Japan*

Room E

E-7:Novel Devices, Physics, and Fabrication
-Novel Materials and Devices-
(9:30-10:30)
Chairs: Y. Kuwahara (Osaka Univ.)
H. Yamaguchi (NTT)

9:30 E-7-1
Solid-electrolyte nanometer switch
T. Sakamoto[1,2], H. Sunamura[1,2], H. Kawaura[1,2], T. Hasegawa[2,3], T. Nakayama[2,3] and M. Aono[2,3], *[1]Fundamental Research Labs., NEC Corp., [2]SORST, JST and [3]NIMS, Japan*

9:45 E-7-2
Piezoresistive Nanomechanical Cantilever based on InAs/AlGaSb Heterostructure
L.F. Houlet[1], H. Yamaguchi[1], S. Miyashita[2] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs, [2]NTT-AT and [3]CREST-JST, Japan*

10:00 E-7-3
InP hot electron transistors modulated by gate electrodes sandwiching emitter mesa
K. Takeuchi[1], H. Maeda[1], R. Nakagawa[1], Y. Miyamoto[1,2] and K. Furuya[1,2], *[1]Tokyo Inst. of Technology and [2]CREST-JST, Japan*

Room F

F-7:Optoelectronic Devices and Photonic Crystal Devices
-Photonic Crystal Devices I-
(9:00-10:30)
Chaisr: N. Yokouchi (Furukawa Electric)
T. Baba (Yokohama National Univ.)

9:00 F-7-1 (Invited)
3D Photonic Crystal as a Novel Dielectric Material
S. Kawakami[1], T. Kawashima[2], T. Sato[1,2], T. Aoyama[2], W. Ishikawa[2], Y. Ohtera[1], H. Ohkubo[1], Kenta Miura[1], and Y. Honma[2] *[1]Tohoku Univ., NICHe, [2]Photonic Lattice Inc., Japan*

9:30 F-7-2
Coupled Waveguide Devices Based on Autocloned Photonic Crystals
M. Shirane[1], A. Gomyo[1], K. Miura[2], Y. Ohtera[2], H. Yamada[1] and S. Kawakami[2], *[1]NEC Corporation and [2]Tohoku Univ., Japan*

9:45 F-7-3
Reflection Characteristics of Coupled Defect Waveguides in Photonic Crystals
T. Katsuyama[1,2], K. Hosomi[1,2], T. Fukamachi[1,2] and Y. Arakawa[1], *[1]The Univ. of Tokyo, [2]Hitachi Ltd., Japan*

Room G

G-7:SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
-III-V Devices & Circuits-
(9:00-10:30)
Chairs: Y. Tateno (Fujitsu Quantum Devices Limited)
Yi-J. Chan (Natl. Central Univ.)

9:00 G-7-1
Over 65% Efficiency 300MHz Bandwidth C-Band Internally-Matched GaAs FET
H. Ohtsuka[1], K. Mori[1], H. Yukawa[1], H. Minamide[1], Y. Kittaka[1], T. Tsunoda[1], S. Ogura[1] and T. Takagi[1], *[1]Mitsubishi Electric Corporation, Japan*

9:15 G-7-2
High-Performance InP HBTs with a Composite Collector
K. Kurishima[1], M. Ida[1], K. Ishii[1] and N. Watanabe[1], *[1]NTT Photonics Labs, Japan*

9:30 G-7-3
A High Reliability and High Gain InP-HEMT with Composite Channel Structure
S. Kurachi[1], Y. Nonaka[1] and J. Nikaido[1], *[1]Fujitsu Quantum Devices Limited, Japan*

Room A

10:10 A-7-4
Characterization of Soft Breakdown Effects for Post-deposition NH_3 Plasma Treated HfO_2 Gate Dielectrics
J.-C. Wang[1], D.-C. Shie[1], T.-F. Lei[1] and C.-L. Lee[1], [1]*National Chiao Tung Univ., Taiwan*

Room B

10:00 B-7-4
High Quality Silicon Nitride Film Formed by Microwave-Excited Plasma Enhanced Chemical Vapor Depositon with Dual Gas Shower Head
H. Tanaka[1], C. Zhong[2], Y. Hayakawa[2], M. Hirayama[2], A. Teramoto[2], S. Sugawa[1] and T. Ohmi[2], [1]*Tohoku Univ. and* [2]*NICHe, Tohoku Univ., Japan*

Room C

10:15 C-7-4
Time-of-flight measurement for lateral carrier transport in organic thin films
M. Kitamura[1], T. Imada[1], S. Kako[1] and Y. Arakawa[1], [1]*Univ. of Tokyo, Japan*

Room D

Room E

10:15 E-7-4
Single-Electron Transistors with Large-Enegry Binary States in a GaN Quantum Dot
K. Kawasaki[1,2], Y. Kitaichi[1], M. Takeuchi[2] and Y. Aoyagi[1,2], [1]*Tokyo Inst. of Technology and* [2]*CREST-JST, Japan*

Room F

10:00 F-7-4
Enhancement of Cavity-Q in a Quasi-Three Dimensional Photonic Crystal Microcavity
M. Ito[1], S. Iwamoto[1] and Y. Arakawa[1], [1]*Univ. of Tokyo, Japan*

10:15 F-7-5
Proposal of a Novel Ring Waveguide Device of 2D Photonic Crystal Slab - The Transmittance Simulated by FDTD Analysis -
K. Furuya[1,2], N. Yamamoto[1], Y. Watanabe[1] and K. Komori[1,2], [1]*AIST, and* [2]*CREST-JST, Japan*

Room G

9:45 G-7-4
75-GHz Optical Clock Divide-by-Two OEIC using InP HEMTs and Uni-Traveling-Carrier Photodiode
K. Sano[1], K. Murata[1], H. Matsuzaki[1], H. Kitabayashi[1], T. Akeyoshi[1], H. Ito[1], T. Enoki[1] and H. Sugahara[1], [1]*NTT Photonics Labs, Japan*

10:00 G-7-5 (Invited)
High-Speed III-VHEMT and HBT Devices and Circuits for ETDM Transmission beyond 80 Gbit/s
R. Quay[1], M. Schlechtweg[1], A. Leuther[1], M. Lang[1], U. Nowotny[1], O. Kappeler[1], W. Benz[1], M. Ludwig[1], M. Leich[1], R. Driad[1], W. Bronner[1], and G. Weimann[1]
[1]*Fraunhofer Institut fur Angewandte Festkorperphysik*

Break

Break

A-8: Advanced Silicon Devices and Device Physics
-Advanced CMOS Technology II-
(10:45-12:05)
Chairs: T. Eimori (Renesas)
K. Goto (Fujitsu Labs.)

B-8: Silicon Process / Materials Technologies
-Si Process-(10:45-12:05)
Chairs: M. Hori (Nagoya Univ.)
T. Horikawa (MIRAI-ASRC)

C-8: Organic Semiconductor Devices and Materials
-Organic Optics-
(10:45-12:00)
Chais: K. Kudo (Chiba Univ.)
C. Adachi (Chitose Inst. of Sci & Technol.)

D-8: New Materials and Characterization
-High-k Dielectrics I-
(10:45-11:25)
Chairs: S. Miyazaki (Hiroshima Univ.)
K. Torii (Selete)

E-8:Novel Devices, Physics, and Fabrication
-Carbon Nanotubes-
(10:45-12:00)
Chairs: Y. Homma (NTT)
F. Nihei (NEC)

F-8:Optoelectronic Devices and Photonic Crystal Devices
-Photonic Crystal Devices II-
(10:45-11:45)
Chaisr: H. Yamada (NEC)
T. Katsuyama (Univ. of Tokyo)

G-8:SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
-SiGe Technologies-
(10:45-11:45)
Chairs: K. Washio (Hitachi)
N. Suematsu (Mitsubishi Electric)

10:45 A-8-1
Schottky Barrier Height Reduction and Drive Current Improvement in Metal Source/Drain MOSFET with Strained-Si Channel
A. Yagishita[1], T.-J. King[2] and J. Bokor[2], [1]*Toshiba Corporation and* [2]*Univ. of California at Berkeley, USA*

10:45 B-8-1
Ni-salicided Poly-Si/poly-SiGe Layered Gate Technology for 65nm-node CMOSFETs
A. Muto[1], H. Ohji[1], T. Maeda[1] and K. Torii[1], [1]*SELETE, Japan*

10:45 C-8-1
Electric Field Induced Second Harmonic Generation from Vacuum Evaporated Metal-Phthalocyanine Film/Metal Electrode Interface
C.-Q. Li[1], T. Manaka[1] and M. Iwamoto[1], [1]*Tokyo Inst. of Technology, Japan*

10:45 D-8-1
Thermal Instability of Poly-Si Gate Al_2O_3MOSFETs
W. Kim[1], T. Kawahara[1], H. Itoh[1], A. Horiuchi[1], A. Muto[1], T. Maeda[1], R. Mitsuhashi[1], K. Torii[1] and H. Kitajima[1], [1]*SELETE, Japan*

10:45 E-8-1 (Invited)
Carbon Nanotube SPM Probe Fabricated by NanoEngineering
S. Akita[1], and Y. Nakayama[1,2], [1]*Osaka Pref. Univ.,* [2]*Osaka Univ., Japan*

10:45 F-8-1 (Invited)
Semiconductor Photonic Crystal Devices
T. Baba[1], [1]*Yokohama National Univ., Japan*

10:45 G-8-1 (Invited)
High-Performance, Low-Cost SiGe:C BiCMOS Technology
B. Tillack[1], D. Knoll[1], B. Heinemann[1], K.-E. Ehwald[1], H. Rucker[1], R. Barth[1], J. Bauer[1], K. Blum[1], D. Bolze[1], J. Borngraber[1], J. Drews[1], G. Fischer[1], A. Fox[1], F. Fuernhammer[1], O. Fursenko[1], T. Grabolla[1], U. Haak[1], W. Hoppner[1], K. Kopke[1], D. Kruger[1], B. Kuck[1], R. Kurps[1], M. Marschmeyer[1], H. H. Richter[1], D. Schmidt[1], P. Schley[1], R. Scholz[1], W. Winkler[1], D. Wolansky[1], H.-E. Wulf[1], Y. Yamamoto[1] and P. Zaumseil[1], [1]*IHP*

Room A

11:05 A-8-2
Experimental Evidence of Gate-Induced Schottky Barrier Height Lowering Due to Image Force in Gated Schottky Diodes
A. Kinoshita[1], K. Uchida[1] and J. Koga[1], [1]*Advanced LSI Technology Lab., Toshiba Corp., Japan*

11:25 A-8-3
Intelligent BSIM4 Model Parameter Extraction for Sub-100 nm MOSFETs era
Y. Li[1,2] and Y.-Y. Cho[2], [1]*National Nano Device Labs, Taiwan and* [2]*National Chiao Tung Univ., Taiwan*

11:45 A-8-4
0.13μm Low-K/Cu Logic CMOS Based Technology for High Performance Analog Devices
J.-C. Guo[1], W.Y. Lien[2], T.L. Tsai[2], S.M. Chen[2], C.M. Wu[2], Y.C. Sun[2] and P. Yang[2], [1]*National Chiao Tung Univ. and* [2]*Taiwan Semiconductor Manufacturing Corp., Taiwan*,

Room B

11:05 B-8-2
Pre-amorphization and co-implantation suitability for advanced PMOS devices integration
R. Surdeanu[1], B. Pawlak[1], R. Lindsay[2], M. van Dal[1], G. Doornbos[1], C. Dachs[1], Y. Ponomarev[1], J.J. Loo[1], K. Henson[2], M. Verheijen[3], M. Kaiser[3], X. Pages[4], M. Jurczak[2] and P. Stolk[1], [1]*Philips Research Leuven,* [2]*IMEC,* [3]*Philips Research Labs and* [4]*ASM International, Eindhoven, Belgium*

11:25 B-8-3
Kinetics of Boron Activation by Flash Lamp Annealing
K. Yamashita[1], M. Noguchi[1], H. Nishimori[1], T. Ida[1], M. Yoshioka[2], T. Kusuda[3], T. Arikado[1] and K. Okumura[4], [1]*SELETE,* [2]*Ushio Inc,* [3]*Dainippon Screen MFG. Co. Ltd. and* [4]*Univ. of Tokyo, Japan*

11:45 B-8-4
High-Speed Damage-Free Contact Hole Etching using Dual Shower Head Microwave-Excited High-Density Plasma Equipment
T. Goto[1], H. Yamauchi[1], T. Kato[1], A. Teramoto[1], M. Hirayama[1], S. Sugawa[2] and T. Ohmi[1], [1]*Tohoku Univ. and* [2]*NICHe, Tohoku Univ., Japan*

Room C

11:00 C-8-2
Conversion Between Three And Two Dimensional Optical Waves In Attenuated Total Reflection Kretschmann Configuration With Nanostructured Langmuir-Blodgett Films
F. Kaneko[1], K. Wakui[1], H. Hatakeyama[1], S. Toyoshima[1], K. Shinbo[1], K. Kato[1], T. Kawakami[1], Y. Ohdaira[1] and T. Wakamatsu[2], [1]*Niigata Univ. and* [2]*Ibaraki National College of Tech., Japan*

11:15 C-8-3
Low-birefringent slab waveguide fabricated with hot-embossing for sol-gel derived phenyl-methyl silsesquioxane films
K. Hasui[1,2], M. Tomiki[1] and N. Okamoto[1], [1]*Shizuoka Univ.,* [2]*Corning Japan K.K, Japan*

11:30 C-8-4
Waterproof Anti-reflection films fabricated by layer-by-layer adsorption process
S. Fujita[1] and S. Shiratori[1], [1]*Keio Univ., Japan*

11:45 C-8-5
Optical Waveguide Characterization of Some Pyroelectric Polymer Thin Films
G.K. Tiwari[1], H.V. Tiwary, [1]*Ravishankar Shukla Univ., India*

Lunch

Room D

11:05 D-8-2
W/HfO_2 gate stacks with Tinv~1.2nm and low charge trapping
A. Callegari[1], P. Jamison[1], B.H. Lee[2], D. Neumayer[1], V. Narayanan[1], S. Zafar[1], E. Gousev[1], C.D. Emic[1], D. Lacey[1], M. Gribelyuk[2], C. Cabral[1], A. Steegen[2], V. Ku[2], R. Amos[2], Y. Li[2], P. Nguyen[2], F.Mc. Feely[1], G. Singco[1], J. Cai[1], S-H Ku[2], Y.Y. Wang[2], C. Wajda[3], D. O'Meara[3], H. Shinriki[3], and T. Takahashi[3], [1]*IBM, SRDC,* [2]*IBM T. J. Watson Research Center, and* [3]*Tokyo Electron America*

Room E

11:15 E-8-2
Top-Gate Carbon-Nanotube Field-Effect Transistors with Very High Intrinsic Transconductance
F. Nihey[1,3], H. Hongo[1,3], Y. Ochiai[1,3], M. Yudasaka[1,2] and S. Iijima[1,2,4,5], [1]*NEC Corporation,* [2]*JST,* [3]*Japan Fine Caramics Center,* [4]*AIST and* [5]*Meijo Univ., Japan*

11:30 E-8-3
Fabrication of Two-Dimensional Carbon Nanostructures Using Radio-Frequency Plasma-Enhanced Chemical Vapor Deposition
M. Hiramatsu[1], K. Shiji[1], H. Amano[1], Y. Ando[1] and M. Hori[2], [1]*Meijo Univ. and* [2]*Nagoya Univ., Japan*

11:45 E-8-4
Control of Electrical Property in Multi-Wall Carbon Nanotube using Electrical Breakdown
N. Aoki[1], K. Miyamoto[1], N. Oguri[1], T. Sasaki[1], K. Ishibashi[2] and Y. Ochiai[1], [1]*Chiba Univ.,* [2]*RIKEN, Japan*

Room F

11:15 F-8-2
Ultraviolet Second Harmonic Generation and Sum-Frequency Mixing in Nonlinear-Optical Polymer Photonic-Crystal Waveguides
S. Inoue[1], K. Kajikawa[1] and Y. Aoyagi[1], [1]*Tokyo Inst. of Technology, Japan*

11:30 F-8-3
Enhanced Light Extraction Efficiency of GaN-Based Blue LED Using Extended-Pitch Surface Photonic Crystal
K. Orita, S. Tamura, T. Takizawa, T. Ueda, M. Yuri, S. Takigawa and D. Ueda, *Matsushita Electric Industrial Co., Ltd, Japan*

Room G

11:15 G-8-2
Base Current Control in Low V_{BE} Operated SiGeC Heterojunction Bipolar Transistors Using SiGe-cap Structure and High Carbon Content Base
T. Saitoh[1], T. Kawashima[1], Y. Kanzawa[1], J. S. Iwanaga[1], K. Idota[1], T. Takagi[1], T. Ohnishi[1], K. Yuki[1], T. Sano[1] and S. Sawada[1], [1]*Matsushita Electric Industrial Co., Ltd., Japan*

11:30 G-8-3
A Low Power SiGe Micromixer for 2.4/5.2/5.7 GHz Multi-band WLAN Applications
C.-Y. Wang[1], H.-W. Chiu[1], H.-C. Chen[1], S.-S. Lu[1] and C.-C. Meng[1], [1]*National Taiwan Univeristy, Taiwan*

Lunch

Room A

A-9: Advanced Silicon Devices and Device Physics
-Electron Mobility Characteristics-
(13:30-14:50)
Chairs: S. Inaba (Toshiba)
N. Sugii (Hitachi)

13:30 A-9-1
Re-Examination on the Universality of Si-MOS Inversion Layer Mobility
H. Irie[1], K. Kita[1], K. Kyuno[1], S. Takagi[2], K. Takasaki[2], M. Kubota[2], S. Saito[2], S. Nishikawa[2] and A. Toriumi[1], *[1]The Univ. of Tokyo and [2]STARC, Japan*

13:50 A-9-2
Channel direction impact of (110) surface Si substrate on performance improvement in sub-100 nm MOSFETs
H. Nakamura[1], T. Ezaki[1], T. Iwamoto[1], M. Togo[1], N. Ikarashi[1], M. Hane[1] and T. Yamamoto[1], *[1]NEC Corporation, Japan*

14:10 A-9-3
Characterization of Plasma Nitridation Impact on Lateral Extension Profile in 50nm N-MOSFET by Scanning Tunneling Microscopy
H. Fukutome[1], T. Saiki[2], M. Hori[2], T. Tanaka[2], R. Nakamura[2] and H. Arimoto[2], *[1]Fujitsu Labs Ltd. and [2]Fujitsu Limited, Japan*

14:30 A-9-4
High Performance Strained Si/SiGe N-channel MOSFETs: Impact of Alloy Composition and Layer Architecture
S. Olsen[1], L. Driscoll[1], K. Kwa[1], S. Chattopadhyay[1] and A. O'Neill[1], *[1]Univ. of Newcastle, UK*

Room B

B-9: Silicon-on-Insulator Technologies
-SOI Low Power Applications-(13:30-14:40)
Chairs: K. Ino (Toshiba)
T. Ipposhi (Renesas)

13:30 B-9-1 (Invited)
Ultralow-power CMOS/SOI Circuit Technology for Ubiquitous Communications
Y. Kado[1], Y. Matsuya[1], S. Mutoh[1], J. Terada[1], H. Morisawa[1], Y. Sato[1], T. Douseki[1] and H. Kyuragi[1], *[1]NTT Microsystem Integration Labs, Japan*

14:00 B-9-2
On the Performance Advantage of undoped ultra thin-film FD-SOI MOSFETs
H. Matsuhashi[1], T. Okamura[1], T. Douseki[2], N. Miura[1], T. Chiba[1] and S. Baba[1], *[1]OKI Electric Industry co., Ltd., and [2]NTT Microsystem Integration Labs, Japan*

14:20 B-9-3
A 0.5-V Noise-Shaping A/D Converter Using Low-Threshold FD-SOI Transistors
Y. Matsuya[1] and T. Douseki[1], *[1]NTT Microsystem Integration Labs, Japan*

Room C

C-9: Organic Semiconductor Devices and Materials
-Molecular Devices and Materials-
(13:30-14:45)
Chais: M. Iwamoto (Tokyo Inst. of Technol.)
A. Sugimura (Osaka Sangyo Univ.)

13:30 C-9-1 (Invited)
Potential Profile and Opto-Electronic Properties at Nano Interface of Conducting Polymer and Metals
K. Kaneto[1] and W. Takashima[1], *[1]Kyushu Inst. of Technology, Japan*

14:00 C-9-2
Effects of different materials use for internal floating electrode on the photovoltaic properties of tandem type organic solar cell
K. Triyana[1], T. Yasuda[1], K. Fujita[1] and T. Tsutsui[1], *[1]Kyushu Univ., Japan*

14:15 C-9-3
Photoinduced Gate Operation and Temperature Dependence in the Coulomb staircase of Organic Single Electron Tunneling Junctions
Y. Noguchi[1], T. Manaka[1] and M. Iwamoto[1], *[1]Tokyo Inst. of Technology, Japan*

14:30 C-9-4
Thin film transistors with oriented cupper phthalocyanine micro-crystals fabricated by physical vapor deposition under DC electric field
M. Sakai[1], M. Iizuka[1], M. Nakamura[1] and K. Kudo[1], *[1]Chiba Univ., Japan*

Break

Room D

D-9: New Materials and Characterization
-High-k Dielectrics II-
(13:30-14:30)
Chairs: T. Nabatame (ASET)
Y. Sugita (Fujitsu)

13:30 D-9-1
Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Transition Metal-Rare Earth Oxides
G. Lucovsky[1], Y. Zhang[1], J.L. Whitten[1], D.G. Schlom[2] and J.L. Freeouf[3], *[1]North Carolina State Univ., [2]Pennsylvania State Univ. and [3]Oregon Graduate Inst., USA*

13:50 D-9-2
Chemical Structures of HfO$_2$/Si Interfacial Transition Layer
H. Nohira[1], Y. Takata[2], K. Kobayashi[3], M.B. Seman[1], S. Joumori[4], K. Nakajima[4], M. Suzuki[4], K. Kimura[4], Y. Sugita[5], O. Nakatsuka[6], A. Sakai[6], S. Zaima[6], T. Ishikawa[2], S. Shin[2] and T. Hattori[1], *[1]Musashi Inst. of Technology, [2]RIKEN, [3]JASRI, [4]Kyoto Univ., [5]Fujitsu Ltd. and [6]Nagoya Univ., Japan*

14:10 D-9-3
Pulsed-source MOCVD HfO$_2$ ultrathin film growth optimized by *in situ* ellipsometry monitoring
Y. Tsuchiya[1], M. Endoh[1] and S. Oda[1], *[1]Tokyo Inst. of Technology, Japan*

Room E

E-9:Novel Devices, Physics, and Fabrication
-Si Nanowire and Dots-
(13:30-14:30)
Chairs: Y. Miyamoto (Tokyo Inst. of Technol.)
S. Miyazaki (Hiroshima Univ.)

13:30 E-9-1
Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs
M. Ikeda[1], Y. Shimizu[1], T. Shibaguchi[1], H. Murakami[1] and S. Miyazaki[1], *[1]Hiroshima Univ., Japan*

13:45 E-9-2
Hybrid Silicon Nanocrystal Silicon Nitride Memory
R. Steimle[1], R. Rao[1], B. Hradsky[1], R. Muralidhar[1], M. Sadd[1], M. Ramon[1], S. Straub[1], S. Bagchi[1], X.-D. Wang[1], J. Hooker[1] and B. White[1], *[1]Motorola SPS, USA*

14:00 E-9-3
Monte-Carlo Simulation of Single-Electron Nanocrystal Memories
J.S. Sim[1], J. Kong[1], J.D. Lee[1] and B.-G. Park[1], *[1]Seoul National Univ., Korea*

14:15 E-9-4
Growth of Si Nanowire Using Metal-Induced Lateral Crystallization
K. Makihira[1] and T. Asano[1], *[1]Kyushu Inst. of Technology, Japan*

Room F

F-9:Optoelectronic Devices and Photonic Crystal Devices
-Ultrafast Photonic Devices-
(13:30-14:45)
Chairs: N. Suzuki (Toshiba)
S. Arahira (Oki Electric)

13:30 F-9-1 (Invited)
SOA-Based Functional Devices for Future Optical Networks
M. L. Nielsen[1], J. D. Buron[1], M. Nord[1], and M. N. Petersen[1], *[1]Research Center COM, Technical Univ. of Denmark, Denmark*

14:00 F-9-2
100-Gbit/s Full-Rate Operation of PD-EAM Optical Gate for Retiming Function
T. Yoshimatsu, S. Kodama, K. Yoshino and H. Ito, *NTT Photonics Labs, NTT Corporation, Japan*

14:15 F-9-3
Semiconductor Dispersion Compensators Based on Asymmetric Coupled Waveguides
Y. Lee[1], T. Shiota[1], A. Takei[1], T. Taniguchi[1] and H. Uchiyama[1], *[1]Central Research Lab, Hitachi, Ltd., Japan*

14:30 F-9-4
Linear and Nonlinear Femtosecond Pulse Propagation through a Quantum Nano-Structure Optical Waveguide Observed with XFROG Spectroscopy
N. Tsurumachi[1,2], N. Watanabe[3], K. Hikosaka[1,2], X.-L. Wang[1,2], K. Komori[1,2], T. Hattori[3] and M. Ogura[1,2], *[1]AIST, [2]CREST-JST and [3]Univ. of Tsukuba, Japan*

Room G

G-9:SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
-GaN Devices-
(13:30-14:45)
Chairs: M. Kuzuhara (NEC)
Y. Ohno (Tokushima Univ.)

13:30 G-9-1 (Invited)
GaN-based microwave power devices: A survey on the activities in Europe
J. Würfl[1], *[1]Ferdinand-Braun-Institut fur Hochstfrequenztechnik, Germany*

14:00 G-9-2
Gate Direction of AlGaN/GaN MODFET's with Low Temperature Coefficient of Threshold Voltage
H. Ishida[1], T. Murata[1], T. Matsuno[1], Y. Ikeda[1], Y. Hirose[1], Y. Uemoto[1] and T. Tanaka[1], *[1]Matsushita Electric Industrial Co., Ltd., Japan*

14:15 G-9-3
AlGaN/GaN Power HEMT Using Advanced Ohmic Structure with Recessed Ohmic Technique
M. Kanamura[1], T. Kikkawa[1], N. Adachi[2], T. Kimura[1], S. Yokokawa[2], M. Nagahara[2], N. Hara[1] and K. Joshin[1], *[1]Fujitsu Labs Ltd. and [2]Fujitsu Quantum Devices Ltd., Japan*

14:30 G-9-4
AlGaN/GaN/graded-AlGaN Double-Heterostructure HEMTs
Y. Zhou[1], R. Chu[1], K.J. Chen[1] and K.M. Lau[1], *[1]Hong Kong Univ. of Science and Technology, Hong Kong*

Break

Room A

A-10: Advanced Silicon Devices and Device Physics
-Poly-Si Device and Sensor-
(15:00-16:00)
Chairs: N. Sugii (Hitachi)
T. Eimori (Renesas)

15:00 A-10-1
High Performance Poly-Si Device with Thin Gate Oxide Film Grown by Plasma Oxidation Technology
F. Imaizumi[1], T. Hayashi[1], K. Ishii[2], A. Teramoto[1], M. Hirayama[1], S. Sugawa[2] and T. Ohmi[1], *[1]NICHe, Tohoku Univ. and [2]Tohoku Univ., Japan*

15:20 A-10-2
A Novel High Performance Power MOSFET with Split Well and Split Poly Structure
F.-T. Chien[1], K.-W. Tu[2], S.-T. Su[3], C.-L. Cheng[3], J.-H. Dung[3], C.-Y. Kung[2] and Y.-C. Huang[2], *[1]Feng Chia Univ., [2]Chung Hsing Univ. and [3]R&D Dept., Chino-Excel Technology Corp., Taiwan*

15:40 A-10-3
Optimization of The Ultra-Low Dark Current CMOS Image Sensor Cell Using n+ Ring Reset
P.-H. Huang[1] and Y.-C. King[1], *[1]STAR, National Tsing-Hua Univ., Taiwan*

Room B

B-10: Silicon-on-Insulator Technologies
-SOI CMOS Technologies-
(15:00-16:30)
Chairs: Y. Kado (NTT)
M. Terauchi (Hiroshima City Univ.)

15:00 B-10-1 (Invited)
Quality Comparison of Commercial Silicon-on-Insulator Wafers by Photoluminescence
M. Tajima[1], *[1]Inst. of Space and Astronautical Science*

15:30 B-10-2
Low-Noise and High-Frequency 0.10μm body-tied SOI-CMOS Technology with High-Resistivity Substrate for Low-Power 10Gbps Network LSI
T. Iwamatsu[1], M. Tujiuchi[1], Y. Hirano[1], T. Matsumoto[1], H. Takashino[1], T. Ikeda[1], T. Yoshimura[2], D. Chen[2], T. Oka[2], H. Kondoh[2], T. Ipposhi[1], S. Maegawa[1], Y. Inoue[1], M. Inuishi[1] and Y. Ohji[1], *[1]Renesas Technology Corp and [2]Mitsubishi Electric Corporation, Japan*

15:50 B-10-3
Fully Depleted SOI CMOS Device with Raised Source/Drain for 90nm Embedded SRAM Technology
M.-H. Oh[1], C.-H. Park[1], H. S. Kang[1], C.-B. Oh[1], Y.-W. Kim[1] and K.-P. Suh[1], *[1]Samsung Electronics, Korea*

16:10 B-10-4
Body Contact Structure using Elevated Field Insulator for Ultra-Thin Film SOI-MOSFETs
S. Yamagami[1], R. Koh[1], H. Wakabayashi[1], J.-W. Lee[1], Y. Saito[2], A. Ogura[1], M. Narihiro[1], K. Arai[2], H. Takemura[1], Y. Ochiai[1], K. Takeuchi[1] and T. Mogami[1], *[1]Silicon Systems Research Labs, NEC Corporation and [2]R&D Technical Support Center, NEC Corporation, Japan*

Room C

C-10: Organic Semiconductor Devices and Materials
-Electroluminescent Devices and Materials-
(15:00-16:00)
Chais: Y. Ohmori (Osaka Univ.)
K. Kaneto (Kyushu Inst. of Technol.)

15:00 C-10-1
Analysis of a charged bio molecular particle passing through semi conductive ion channel on biological membrane
H. Hirayama[1], *[1]Asahikawa medical college, Japan*

15:15 C-10-2
Fabrication and Characteristics of Increased Efficiency of Layered Polymeric Electroluminescent Diodes
Y. Hino[1], M. Yamazaki[1], H. Kajii[1] and Y. Ohmori[1], *[1]Osaka Univ, CRCast, Japan*

15:30 C-10-3
Passivation of organic light emitting diodes with plasma polymerized p-xylene thin films deposited by PECVD
S. Sohn[1], S. Kho[1] and D. Cho[1], *[1]Sungkyunkwan Univ., Physics, Korea*

15:45 C-10-4
High efficiency fluorescent organic light emitting devices utilizing a phosphorescent sensitizer
S. Liu[1], *[1]Jilin Univ., China*

Room D

D-10: New Materials and Characterization
-High-k Dielectrics III-
(15:00-16:20)
Chairs: M. Hiratani (Hitachi)
H. Watanabe (NEC)

15:00 D-10-1
Molecular Dynamic Simulation on the Crystallization of HfO_2, Hf-aluminate, and Hf-silicate
Y. Kosaka[1], T. Yamasaki[1] and C. Kaneta[1], *[1]Fujitsu Labs Limited[1], Japan*

15:20 D-10-2
Theoretical Analysis of Oxygen Diffusion in monoclinic HfO_2
M. Ikeda[1], G. Kresse[2], T. Nabatame[1] and A. Toriumi[3,4], *[1]MIRAI ASET, [2]Universitaet Wien, [3]MIRAI AIST and [4]Univ. of Tokyo, Japan*

15:40 D-10-3
Etching yields of HfO_2 under Ar^+ and CF_X^+ (X = 1, 2, 3) ion beam irradiation
K. Karahashi[1], N. Yamagishi[1], T. Horikawa[2] and A.Toriumi[2,3], *[1]MIRAI ASET, [2]MIRAI ASRC, AIST and [3]Univ. of Tokyo, Japan*

16:00 D-10-4
Selective Dry Etching of HfO_2 in CF_4, Cl_2 and HBr Based Chemistry
T. Maeda[1], H. Ito[1], R. Mitsuhashi[1], A. Horiuchi[1], T. Kawahara[1], A. Muto[1], T. Sasaki[1], K. Torii[1] and H. Kitajima[1], *[1]Semiconductor Leading Edge Technologies, Inc., Japan*

Room E

E-10:Novel Devices, Physics, and Fabrication
-Quantum Computing Devices-
(15:00-16:15)
Chairs: K. Ishibashi (RIKEN)
Y. Pashkin (NEC)

15:00 E-10-1 (Invited)
Quantum Oscillations in Two Coupled Charge Qubits
Y. Pashkin[1], T. Yamamoto[1,2], O. Astafiev[1], Y. Nakamura[1,2], D. Averin[3], and J.-S. Tsai[1,2], *[1]RIKEN, [2]NEC Corporation, [3]State Univ. of New York, USA*

15:30 E-10-2
Measurement of Two-Qubit States detected by Quantum Point Contacts
T. Tanamoto[1] and H. Xuedong[2], *[1]Toshiba Corporation and [2]Univ. at Buffalo, SUNY, USA, Japan*

15:45 E-10-3
Coherent control in inhomogeneously broadened quantum dots ensemble and its coherent transient phenomena
N. Tsurumachi[1,2], K. Komori[1,2] and T. Hattori[3], *[1]AIST, [2]CREST-JST and [3]Inst. of Applied Physics, Univ. of Tsukuba, Japan*

16:00 E-10-4
Observation of the spin-related even-odd effect in single-wall carbon nanotube quantum dots
H. Maki[1], M. Suzuki[1], Y. Ishiwata[1] and K. Ishibashi[1], *[1]RIKEN, Japan*

Room F

F-10:Optoelectronic Devices and Photonic Crystal Devices
-New Photonic Materials-
(15:00-16:00)
Chaisr: O. Wada (Kobe Univ.)
T. Mizumoto (Tokyo Inst. of Technol.)

15:00 F-10-1
Intersubband Transition Based on a Novel II-VI Quantum Well Structure for Ultrafast All-optical Switching
R. Akimoto[1], B. Li[1], F. Sasaki[1] and T. Hasama[1], *[1]AIST, Photonics Research Inst., Japan*

15:15 F-10-2
Control of $In_xGa_{1-x}As$ Cappling Layer Induced Optical Polarization in Edge-Emitting Photoluminescence of InAs Quantum Dots
J. Pachamuthu[1], H. Tanaka[1], T. Kita[1], O. Wada[1], H. Ebe[2], M. Sugawara[2], J. Tatebayashi[2], Y. Arakawa[2], Y. Nakata[3] and T. Akiyama[3], *[1]Kobe Univ., [2]Research Centre for Advanced Science and Technology, Univ.of Tokyo and [3]Fujitsu Labs Ltd., Japan*

15:30 F-10-3
High Performance Electroluminescence from Nanocrystalline Si with Carbon Buffer
B. Gelloz[1] and N. Koshida[1], *[1]Tokyo Univ. Agr.&Tech., Japan*

15:45 F-10-4
Optical Component Coupling Using Self-Written Waveguides
N. Hirose[1] and O. Ibaragi[1], *[1]ASET, Japan*

Room G

G-10:SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
-High Voltage Devices-
(15:00-16:00)
Chairs: K. Morizuka (Toshiba)
T. Enoki (NTT)

15:00 G-10-1 (Invited)
Development of AlGaN/GaN power HFET for the application of an inverter circuit
S. Yoshida[1], *[1]Yokohama R&D Labs, The Furukawa Electric Co., Ltd., Japan*

15:30 G-10-2
Si/SiGe Heterojunction Collector for Low Loss Operation of Carrier Stored Trench-Gate Bipolar Transistor
T. Kudoh[1] and T. Asano[1], *[1]Center for Microelectronic Systems, Kyushu Inst. of Technology, Japan*

15:45 G-10-3
Design and Demonstration of High Breakdown Voltage GaN-HEMT using Field Plate Structure for Power Electronics Applications
W. Saito[1], Y. Takada[2], M. Kuraguchi[2], K. Tsuda[2], I. Omura[1] and T. Ogura[1], *[1]Toshiba Corporation, Semiconductor Company and [2]Toshiba Corporation, Research & Development Center, Japan*

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[7] Novel Devices, Physics, and Fabrication
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[9] Silicon-on-Insulator Technologies
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[10] Non-Volatile Memory Technologies

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H. Takada (Mitsubishi Electric)
K. Yoshikawa (Toshiba)

[11] SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

Chair: T. Enoki (NTT)

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[12] System-Level Integration and Packaging Technologies

Chair: K. Takahashi (ASET)

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T. Suga (Univ. of Tokyo)
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[13] Organic Semiconductor Devices and Materials

Chair: M. Iwamoto (Tokyo Inst. of Technol.)

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H. Tada (Okazaki Natl. Reserch Inst.)

[14] Micro-Nano Electromechanical Devices for Bio-and Chemical Applications

Chair: Y. Miyahara (NIMS)

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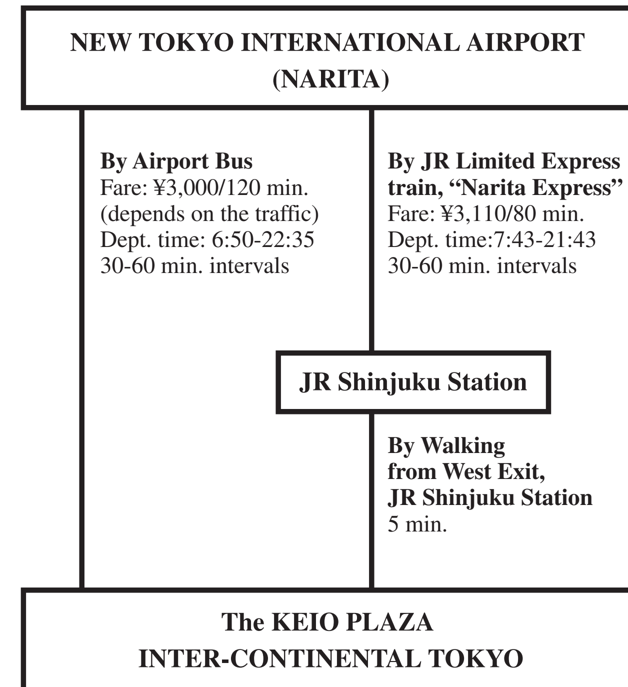
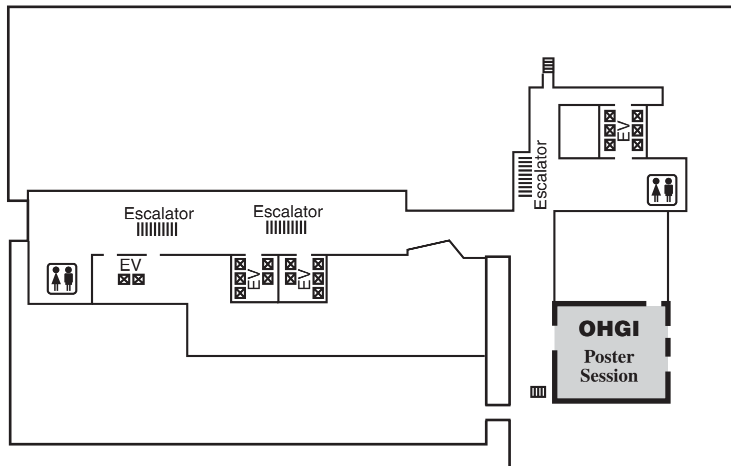


Poster Room

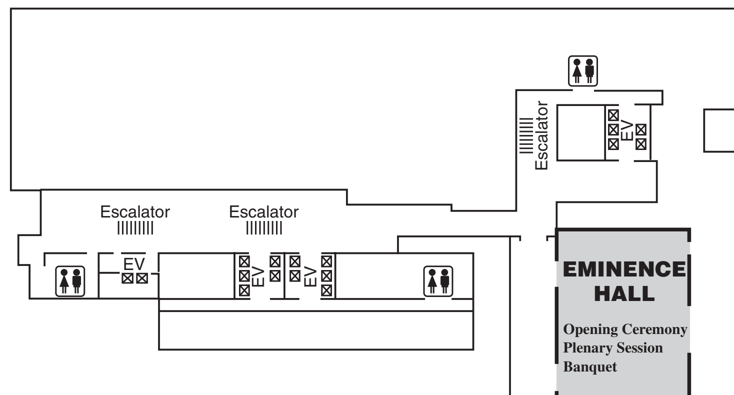
4F



Eminence Hall

5F

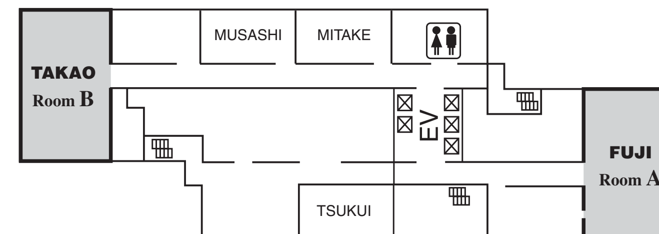
Opening Ceremony
Plenary Session
Banquet



SSDM 2003 Floor Map, Keio Plaza Inter-Continental Tokyo

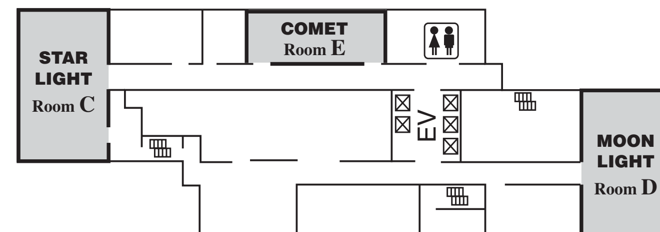
Conference Room A, B

42F



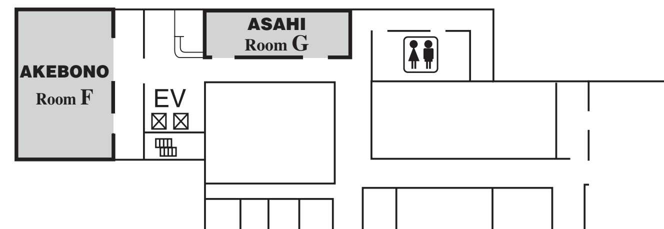
Conference Room C, D, E

43F



Conference Room F, G

47F



Access to the Keio Plaza Inter-Continental Tokyo from Shinjuku Station

徒歩 [On Foot]

●上記地図参照　●See the map

新宿（西口）・Shinjuku Sta. (West Exit) —5分・5min.→ 京王プラザホテル・Keio Plaza Inter-Continental Tokyo

地下鉄 [Subway]

●都営大江戸線170円　●Oedo Line 170 YEN

新宿・Shinjuku Sta. —2分・2min.→ 都庁前・Tocho-Mae Sta.　A-1番出口から徒歩1分・Exit #A-1,1min.walk

タクシー [Taxi]

●約700円　●Approx. 700 YEN

新宿（西口）Shinjuku Sta. (West Exit) —7分・7min.→ 京王プラザホテル Keio Plaza Inter-Continental Tokyo